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Voids in SMT Solder Joints – Trends in Automotive Electronics

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Abstract
Voiding in SMT (surface-mount technology) solder joints has been a topic of intensive discussions particularly since the introduction of lead-free technology. This is also reflected by various IPC guidance documents, as IPC-7093 (Design and Assembly Process Implementation for Bottom Termination Components) and IPC-7095 (Design and Assembly Process Implementation for BGAs), which contain some information on typical voiding levels and the impact of voiding on assembly reliability. In terms of quantitative requirements and limits for acceptability of voiding, values are provided only for ball-grid arrays in current versions of J-STD001, IPC-A610 and IEC 61191-2. However, recent discussions during standardization-related meetings as well as the vast amount of papers dedicated to voiding reveal a need for a more extensive coverage of voiding in standards. This is particularly true in automotive electronics, where customer specifications already often contain requirements for voiding in SMT solder joints. This fact obviously calls for a more extended coverage of voiding in the automotive addenda for J-STD-001 and IPC-A610 in the future. To accomplish this, two challenges have to be addressed: (i) a common understanding of the impact of voiding on assembly reliability between different stakeholders in the supply chain has to be established. The design for reliability of electronic assemblies has to cover all aspects, ranging from solder-joint lifetime to other aspects as electrochemical reliability. Any material and process optimization should thus be oriented towards the goal of an overall assembly-reliability improvement rather than focusing exclusively on the reduction of voiding. Adopting too tight limits on voiding may even impede the implementation of solutions for overall reliability improvements, as has been shown for some cases. Moreover, the notion of voiding does not generally make sense for all types/geometries of solder joints: For flat, laterally extended solder joints, e.g. at exposed pad soldering areas, solder coverage is a more appropriate measure for thermal transfer than void percentage. (ii) typical X-ray inspection systems used nowadays in automotive mass production do not generally satisfy tight requirements on gage repeatability and reproducibility (gage R&R), i.e. such systems do not qualify as measurement systems for voiding. This can be understood considering that their primary purpose is the detection of soldering defects like bridging, wetting failures etc. For introduction of void level requirements, a certain level of X-ray reproducibility would be required. This paper will provide an overview of current activities in standardization related to the above-discussed challenges.

Introduction
The formation of voids in solder joints has been investigated in earlier publications and will not be treated extensively in this paper (see, for example, [1] [2] [3] and references therein). A common understanding is that a certain average void level, depending on the component's geometry, and a process inherent void level scattering occurs for current state-of-the-art soldering technologies.
Concerning the effects of voiding in solder joints of surface-mount technology (SMT) components on assembly function and reliability no such clear general agreement exists, and it has been a controversially discussed topic over the past years. The main concern related to voiding is that it may have a negative impact on solder-joint reliability under thermomechanical and dynamic mechanical (e.g. vibration) load and on the thermal and electrical performance of solder joints. Whereas the effects of voiding on the thermal and electrical performance of solder joints can be assessed rather straightforwardly based on numerical or even analytical calculations, the impact of voiding on solder-joint reliability is more difficult to assess and less clear. In this context, a very thorough distinction of different types of voids is mandatory: In total, (at least) five different types of voids in solder joints can be distinguished (see [4]), but as only macro-(process-)voids and design-induced voids can be easily observed with standard X-ray imaging, much attention has been focused on these types of voids. Numerous studies have been devoted to the reliability impact of such macro voids, but an unambiguous confirmation of a reliability concern has to our best knowledge, not been obtained, unless untypical, excessive voiding levels generated deliberately in studies (and not in mass production) are taken into consideration. Yet, suppliers of solder pastes have embarked on developing solder pastes and flux systems optimized for low voiding, marketing these as if this feature would be a competitive advantage, which is yet unproven.
In the light of the existence of various types of voids and the lack of conclusive evidence for negative impacts of macro and design-induced voids it comes as no surprise that voiding is practically not covered by existing standards for requirements

and acceptability of electronic assemblies as J-STD-001G [5], IPC-A-610G [6] and IEC 61191-2 [7]. Except for area-array components, these standards do not impose restrictions on the acceptable voiding levels of electronic assemblies. However, discussions in standardization organizations are ongoing if a more extensive discussion of voiding in standards would be required.

At present, this discussion is in full blast in automotive electronics, as this branch of the electronics industry is mostly employing lead-free alloys in SMT soldering, for which voiding is more prominent compared to leaded alloys. Moreover, very high reliability requirements are imposed on such electronics, thus reliability concerns related to voiding may drive various stakeholders in the automotive electronics supply chain to impose unsubstantiated and even too tight limits on voiding. It is therefore desirable to arrive at a common understanding regarding acceptable voiding levels, which get endorsed by all stakeholders throughout the automotive electronics supply chain. This work, outlining consensus found within a working group of the German Electrotechnical Commission (DKE – Deutsche Kommission Elektrotechnik) among various stakeholders in the automotive electronics supply chain, may be used as a starting point among other stakeholders concerned.

An important aspect that also needs to be taken into consideration in any standardization activity is the lack of robust measurement systems for voiding in mass production satisfying common gage repeatability and reproducibility (Gage R&R) requirements. Voiding is characterized typically by automated X-ray inspection (AXI) systems operating in two-dimensional (2D-AXI) or three-dimensional (3D-AXI) imaging modes. For such systems, neither references samples nor round-robin investigations are available according to our best knowledge. This aspect is also addressed within this work (see section ‘Determination of voiding levels in solder joints’).

Types of voids

There are various sources of voids in SMT solder joints, which lead to voids of different sizes and at different locations. The different types are summarized in Table 1 (see [4]).

Table 1 – Types of voids with indication of root cause, occurrence in automotive electronic assemblies, detectability, effect on thermomechanical reliability, thermal and electrical function and overall assessment (based on [4]).

Type of voids	Origin / root cause	Occurrence in automotive el. assemblies	Detectability with in-line automated X-ray inspection	Reliability influence thermo-mechanical	Influence thermal / electrical function	Overall assessment
Macrovoids (type I): typically between 50 and a few 100 µm) in dia-meter, sometimes referred to as 'process' voids	Generated by the outgassing of flux volatiles	Common	Good detectability	No proven reliability impact unless excessive voiding occurs	No impact unless excessive voiding occurs	Common in electronic assemblies, not a concern unless excessive voiding occurs
Design-induced voids (type II) typically between 50 and a few 100 µm) in dia-meter	Generated by gasses entrapped within the microvia, i.e. air, water vapor, flux volatiles	Common for via-in-pad land design	Good detectability	No proven reliability impact unless excessive voiding occurs	No impact unless excessive voiding occurs	Common in electronic assemblies, not a concern unless excessive voiding occurs
Skrinkage voids (type III): Elongated, voids with rough, `dendritic` edges emanating from the surface of the solder joint	Caused by the reduction in solder volume when the solder is in the process of solidification from liquid to solid, related to solidification sequence of lead-free alloys	Common	Poor detectability due to limited size	No impact	No impact	Common in lead-free electronic assemblies, not a concern.
Planar micro-voids (champagne voids, type IV): small (< 25 µm) voids at solder-to-land or solder-to-component termination interface	Not unequivocally determined; likely due to anomalies in surface-finish application	Limited: immersion Ag finishes, less frequently observed on ENIG and OSP, also observed at solder-to-component termination interface	Poor detectability due to small size	Can negatively impact reliability in case of high area coverage (perforation)	Low impact	Generally not a concern for automotive electronic assemblies
IMC micro-voids (type V): Sub-micron voids located between the IMC and the Cu land; also known as Kirkendall voids	Growth occurs at elevated temperatures; commonly accepted root-cause: Organic impurities incorporated in the Cu during electroplating.	Limited: Not commonly observed, even though extensive destructive analysis is commonly employed in reliability testing of automotive electronics	Very poor detectability due to very small size	Can negatively impact reliability	Low impact	Generally not a concern for automotive electronic assemblies
Pinhole micro-void (type VI)s: Micron-sized voids within the IMC, between IMC and the PCB Cu land or (rarely) close to IMC in the solder	Generated by unstable plating process at board supplier	Limited: Not commonly observed, even though extensive destructive analysis is commonly employed	Very poor detectability due to very small size	Can negatively impact reliability	Low impact	Generally not a concern for automotive electronic assemblies

Finding consensus in the supply chain on acceptable voiding levels – the case of automotive electronics

This work outlines consensus on acceptable voiding levels found within a working group of the German Electrotechnical Commission (DKE – Deutsche Kommission Elektrotechnik) among various stakeholders in the automotive electronics supply chain. This working group DKE AK682.0.7 'Assembly and Interconnect Technology in Automotive Electronic Assemblies' started its work roughly two years ago and features a very broad coverage of the entire supply chain in automotive electronics (see Table 2). Even though the group is focusing on automotive electronic assemblies, the approach is quite general and may also be helpful in other industries. The main findings have already been harmonized with Technical

Committee TC 91 'Electronics Assembly Technology' of the International Electrotechnical Commission (IEC) and an IEC Technical Report is under preparation.

Table 2 – Coverage of the supply chain of automotive electronics in the working group DKE AK682.0.7.

Chair: U. Welzel (Robert Bosch)		Vice-chair: U. Pape (VW)	
OEM	**Tier 1 & EMS**	**Tier n**	**others**
Audi, BMW, VW	Aptiv, Brose, Continental, Delphi, Hella, Kostal, Robert Bosch, Valeo, Zollner	Goepel, Heraeus, Indium, Infineon, Murata, Osram, Rehm Thermal Systems, TechnoLab, Viscom, Vishay, XRay-Lab, Carl Zeiss, Zestron	Diehl Aerospace, Fraunhofer ENAS & IZM, Hensoldt, Trainalytics, Universities Dresden, Freiburg, Rostock

The following aspects were taken into consideration in the discussion:

(i) Considering typical components, printed boards, assembly materials and processes, which voiding levels do typically occur in SMT assemblies?
(ii) Which environmental loads (e.g. mechanical, thermomechanical) are imposed on assemblies and what is the impact of voids on solder-joint reliability under these loads?
(iii) Which performance characteristics of solder joints (e.g. thermal transfer) are important and what is the impact of voids on these characteristics?
(iv) Which void or solder coverage percentages should be defined as limits trying to find a reasonable compromise between function and reliability concerns and feasibility/processability.

Obviously, a 'one-size-fits-all' approach to voiding in solder joints cannot be appropriate: A threshold for acceptability for area-array components of 30 % voiding, as an example, can certainly not generally apply to solder joints at exposed pads. For this reason, it is required to arrive at a 'component Pareto', indicating which types of solder joints are to be addressed with which priority. In the first approach, the following components where considered:

- **Area-array components** like BGA and LGA,
- **Bottom-termination components** involving a lead-frame construction, as quad-flat no lead packages, dual-flat no lead packages etc.,
- **Thermal planes of components** with gull-wing solder joints as quad-flat packages, transistors with thermal planes,
- **Chip components**.

When voiding levels of solder joints are analyzed it turns out that typically a rather wider scatter of voiding levels occurs, even for the same joints (i.e. joints at the same layout positions) investigated on a set of PCBAs of a certain type. This can be understood as follows: Online X-ray analysis during reflow processes has shown that void formation during reflow is a quite dynamic process. Voids are generated, grow and, upon reaching a certain critical size where the voids touch the outer surface of a solder joint, escape from the solder joint. A few seconds later new voids are forming, often at the same location from flux residues not visible in X-ray inspection. This process can be observed by online X-ray analysis. Thus, the void level in a solder joint during the melting phase of a reflow process may look like an irregular saw-tooth cycle [3]. For this reason, too tight thresholds should be avoided, as it may not be possible to comply with these limits in high volume production, where the entire scatter of void distributions is expected to occur.

Influence of voids on solder joint performance Most voiding concerns concentrate on issues related to the mechanical and thermomechanical reliability performance and the thermal and electrical function of solder joints. In the following, the discussion will be focused on voids of type I and II (cf. Table 1). Even though the reliability impact of other types of voids may be more pronounced in case of high occurrence, those are normally rare in automotive electronic assemblies.

Mechanical reliability. The mechanical reliability concerns vibration drop or shock loads. The influence of voids on mechanical solder joint reliability under such loads is not investigated very deeply, which already hints at the very limited relevance of voiding in this context. Based on long-term field experience, mechanical loads are not generally expected to result in void-related failures. For chip components at least up to 1206 size and also multi-pin components there is no negative effect of voiding seen since these components are not critical concerning mechanical loads. Some potential risks can be conceived for the following two groups of components:

- Heavy components (electrolytic capacitors, SMD coils, chokes, shunts …) with small pin count (<4). For such components, voids could be relevant for shock/drop reliability due to high shear force load during a mechanical impact.
- Area-array components with low standoff and high number of solder joints like LGA modules > 2 x 2 cm and castellation modules. For such components, bending-induced failures could occur with voids playing a relevant role.

Due to limited experience and knowledge about void influence on drop, shock and vibration performance deeper investigations are recommended only in case of exceptionally high requirements concerning mechanical loads, exceeding typical field loads in automotive electronics.

Thermomechanical reliability. Since voiding affects the solder-joint geometry and microstructure and can interact with crack propagation, it can have an impact on thermomechanical solder joint reliability. For most types of solder joints preferred crack paths during temperature cycling of boards can be identified. Especially if voids are positioned within these critical paths the stability against cracking can be reduced as specific types of voids may accelerate the crack propagation and weaken the solder joint stability. On the other hand, voids can increase the flexibility of solder joints and improve reliability at least locally for certain solder-joint geometries, e.g. for BGA solder joints. The overall effect on solder-joint reliability is difficult to assess, especially for components with multiple solder joints like BGAs. For such components also interactions between the solder joints have to be taken into account. For example, voids in one solder joint may increase flexibility of this joint, but may also transfer stress partially to neighboring solder joints. Since voiding effect on thermomechanical reliability is difficult to assess only by theoretical simulations, some experimental evaluations have been done and reported in literature.

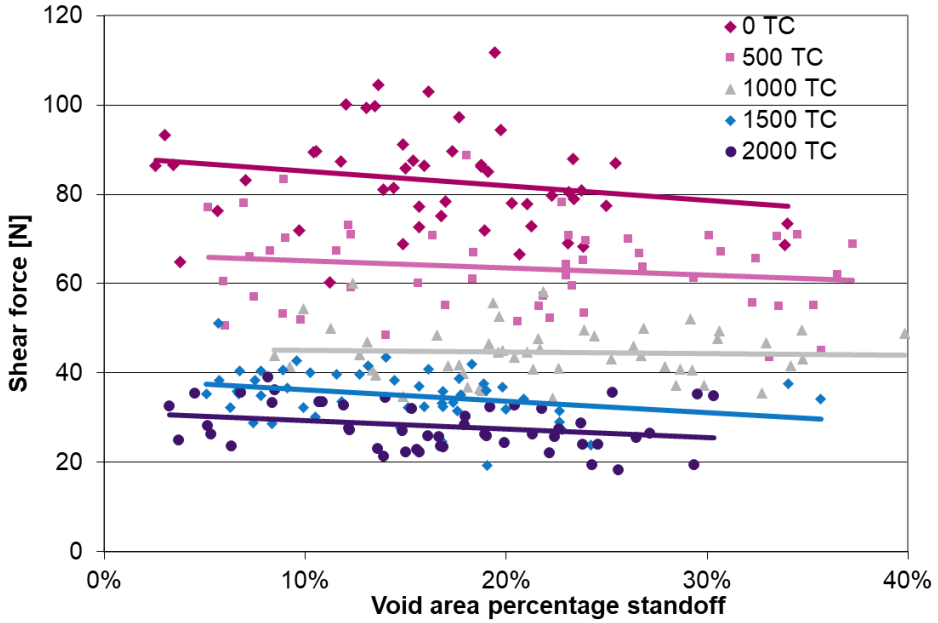


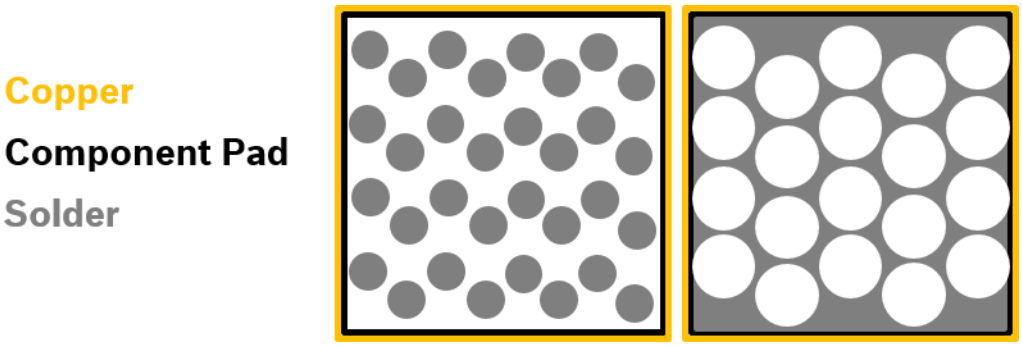
Figure 2: Correlation void level standoff chip resistor 1206 and shear force after TC

Figure 1: Correlation of lifetime of BGA (BGA 416) under thermal cycling (-40 °C/ +125 °C) with average and maximum void levels [3].

Various studies have been devoted to voiding in area-array components (see, e.g. [8] and references therein. In another study the TC lifetime of BGA416 (pitch 1.0) with normal and intentionally increased voiding has been compared [3]. The lifetime in this study was the time until the occurrence of an electrical failure during online measurement with temperature cycling between -40° and +125°C (see Figure 1). These results confirm the conclusion of theoretical studies that maximum voiding

even exceeding 30% in individual is not significantly affecting reliability. The second important finding from this investigation is the high variation of lifetime values independent of maximum void level.
For chip components there are only few investigations reported in literature. One result shows the shear force performance of soft terminated 1206 chip resistor solder joints after different levels of temperature cycling -40°C/ +125°C (see Figure 2, [3]). The void level within standoff area was highly varying due to a component specific termination outgassing issue.

This evaluation shows that independent of TC level the shear force is almost not affected by void level. The conclusion from this result is that void level does not affect thermomechanical lifetime performance significantly up to about 35% void level in the standoff area. This result is primarily valid for voids in standoff area due to different crack behavior of meniscus. But in most cases especially for standard SnAgCu solder alloys void rate within meniscus is normally rather low.
For bottom-terminated components (BTC) literature data is sparse. A very rigorous recent study did not address electrical grounding and thermal resistance of voids at thermal pads of QFNs, but instead focused on how board design (i.e. vias) affect the formation of voids and whether the presence of voids in the thermal pad impacts the solder joint reliability of the signal interconnect. This study concluded that, in the components tested in the study, the magnitude of voiding at the thermal pad did not affect the reliability [6].



	Example 1	Example 2
Voiding	0 %	65 %
Solder coverage	35 %	35 %

Figure 3: Exemplary calculation showing that two different distributions of solder at a thermal-pad solder joint can have very different voiding levels, but identical solder coverage.

Thermal functionality. Another concern in the context of voiding is a potential heat transfer reduction for large thermal pads, referred to as exposed pads. Within these large area solder joints void content is normally significantly higher than in small standard I/O solder joints. The voiding in such solder joints reduces the area with a connection between the components' exposed pad and the PCB land (in the following called 'solder coverage'). A relative percentage of solder coverage can be calculated by taking the ratio of the area with a solder connection between exposed pad and PCB land with respect to the total wettable area (i.e. area were the exposed pad of the component is overlapping with open Cu on the PCB). This solder coverage is directly related to the thermal transfer, see the sketch in figure 3. Defining a criterion for solder coverage rather than for void level is strongly recommended for thermal pads, since this parameter directly correlates to thermal connection, whereas void level might be a misleading value as can be seen in figure 3.

The range which usually can be found with standard production parameters is between 90 % and 50 %, sometimes down to ~40% solder coverage. The influence of reduction of solder coverage on overall thermal resistivity can be calculated.

A sketch of the simplified model behind this calculation is shown in Figure 4. The overall heat resistivity between component surface and heat sink or housing surface on the other PCB side is calculated for the whole exposed pad area.
For a realistic exposed pad constellation, the influence of voiding on vertical thermal resistivity of solder joint plus PCB is calculated and illustrated in Figure 5. Since via filling may reduce thermal resistance of PCB and enhance void influence, this

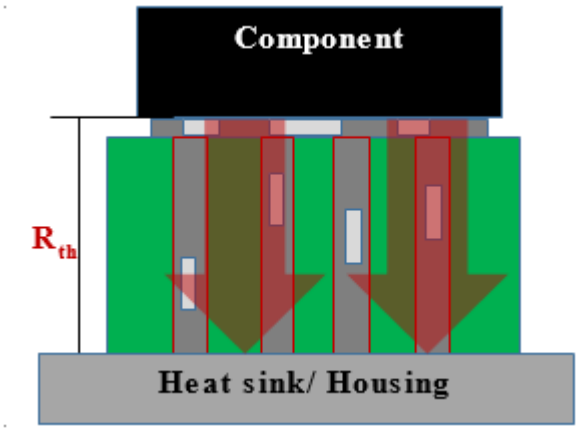


Figure 4 Sketch of heat transfer with exposed pad solder joints

effect was also considered.

This calculation clearly shows that solder joints of exposed pads on standard PCBs are not sensitive to voiding down to a soldered area of about 20 % or even 10 %. The main bottleneck for heat transfer is the PCB with the plated through holes, and
not the exposed-pad solder joint, even if a high number of vias is supporting the vertical transfer of heat through the PCB. Solder filling of vias also does not change the situation substantially.

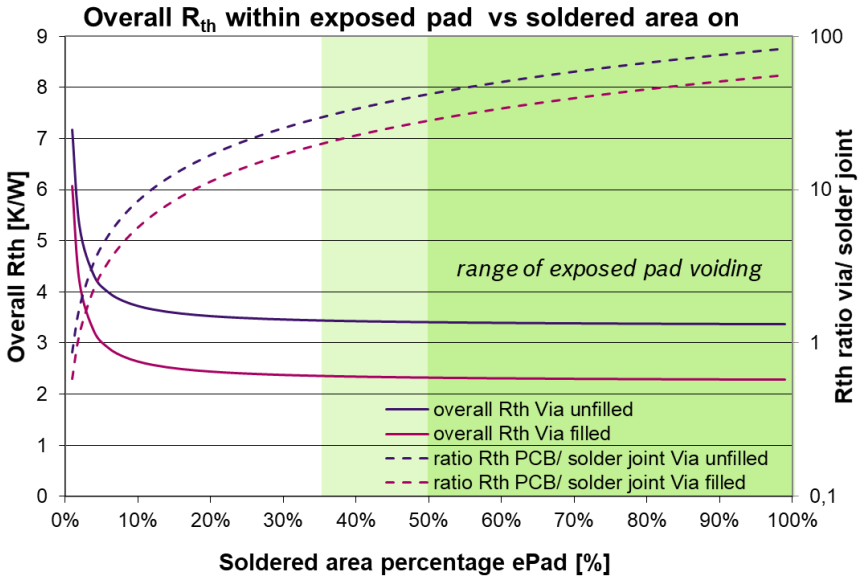


Figure 5 - Calculation of solder coverage at exposed pads on overall thermal resistance R_{th}

The influence of voiding within exposed pads on solder-joint lifetime under thermal cycling was not explicitly investigated, but from field experience it is known that this kind of solder joint is generally not an issue for reliability if sufficient thermal transfer is assured.
Thus at least the normal range of solder coverage down to about 35 % does not result in detrimental effects on thermal transfer. This may be different only if the component is soldered directly on a heat sink or to thick or massive copper. In this

case the PCB with the plated through hole is no longer the bottleneck for heat transfer and solder coverage shows a much more pronounced influence on thermal resistivity. For these applications vacuum soldering is known as an effective method for void reduction.
These considerations are valid for standard conditions and for overall heat transfer calculation. Special applications with higher heat transfer requirements or dynamic effects like hot spots within component exposed pad area may impose additional requirements. Therefor these results do not claim general validity and a given void level may be acceptable in one application, but inacceptable in another application.

Electrical functionality
Since electrical resistance of solder joints is not critical for most types of components voiding does not affect electrical functionality of components normally. Exemptions may be high frequency or high current applications only. These cases have to be assessed individually.

Recommendations for acceptability of voiding in automotive electronic assemblies
Based on the considerations outlined above, values for acceptable minimum solder coverage or maximum void level as well as ranges for process indicators have been discussed and agreed upon within DKE working group. The results of these discussions are shown in Table 3 as acceptability limits and process indicators. A process indicator is a condition (not a defect) that identifies a characteristic that does not affect the form, fit or function. Such condition is a result of material, design and/or operator/machine related causes that create a condition that neither fully meets the acceptance criteria nor is a defect (see also [6]). In the case of voiding/solder coverage, such condition should not occur at high frequency and should be taken as a hint that the process should be analyzed. This may results in action to reduce voiding or to increase solder coverage, respectively, and improve yields.

Table 3: Values for acceptable minimum solder coverage or maximum void level as well as ranges for process indicators.

Type of component/solder joint	***Voiding / solder coverage***	***Acceptability limit***	***Process indicator***	***Notes***
Area-array component	Voiding *v*	v <30 % (no via-in-pad design) v <50 % (via-in-pad design)	30 % < v < 50 % (via-in-pad design)	*1)*
Bottom-termination components – thermal pad	Solder coverage *c*	c > 35 %	35 % < c < 50 % average connection area	*1)2) 3) 4) 5)*
Bottom-termination components – pins	Solder coverage *c*	c > 50 %	50 % < c < 65 %	*1)*
Thermal pads of components with gull-wing solder joints as quad-flat packages	Solder coverage *c*	c > 35 %	35 % < c < 50 % average connection area	*1) 2) 3) 4)5)*
Thermal pads of transistors as TO-252 (D-PAK™)	Solder coverage *c*	c > 35 %	35 % < c < 50 % average connection area	*1)2) 3) 4) 5)*
Chip components (in stand-off)	Solder coverage *c*	c > 50 %	50 % < c < 65 %	*1)*

1) Type III - VI voids can typically not be detected in 2D X-ray imaging under mass-production conditions and are excluded from the above criteria.
2) For certain designs, e.g. via in pad, it may not be possible to comply with the above threshold values. In such cases, it is the shared responsibility of design authority and manufacturer to provide objective evidence for thermal and electrical functionality as well as solder-joint reliability.
3) If thermal planes of components are soldered directly on heat sinks, the thresholds for solder coverage shall be agreed between user and design authority.
4) If the above defined connection area is not sufficient for thermal transfer for a particular component, it is the responsibility of the design authority to define a component-specific minimum connection area.
5) Averages to be taken over at least 25 solder joints.

Determination of voiding levels in solder joints

Voiding can be investigated using metallographic cross sections. However, in view of the required effort, the number of solder joints that can be investigated is obviously restricted. Moreover, this approach is time consuming and the results cannot be straightforwardly interpreted, as a cross section at for example some central plane of a solder joint will generally not reveal the maximum dimension of the voids in a joint, or this plane may even miss voids in the solder joint completely. Thus, a 'sliced' cross section would be the ideal method of investigation from the perspective of accuracy and precision, increasing the required effort even further. Obviously, this destructive approach is not suitable as a quality gate in mass production and thus other methods of investigation are required.
X-ray imaging-based inspection (XI) operating mostly in two-dimensional (2D) mode is commonly used in automotive mass production for the inspection of non-visible, i.e. 'hidden' solder joints (as joints underneath components) and 'hidden' features of solder joints. A main advantage of X-ray inspection is that even in 2D mode it includes the whole volume information of the solder joints, compared to 2D information of cross sections. XI involves irradiation of a printed-board assembly with an (ideally) point-like X-ray source and recording of the transmitted intensity with a flat area detector. This can be done under different angles, but for the investigation of voiding the perpendicular (with respect to the plane of the PCBA) illumination is usually adopted. Inclined imaging can be employed if solder joints with a principal normal orientation with respect to the surface of the PCBA are investigated (e.g. for through-hole solder joints).
As high throughput is required in automotive mass production, these systems are normally automated both with respect to the handling of the assemblies to be inspected by the use of a conveyer systems as well as with respect to the analysis of the acquired images. As such, these systems are known as automated X-ray inspection (AXI) systems. Already the name indicates that these systems were devised as inspection, and not as measurement systems. Usually, these systems serve as quality gates in electronics manufacturing, by detecting wetting failures, bridging, solder balls etc. based on pass/fail classification of inspection features as gray values, gradients of gray values etc.

If such AXI systems are employed for the investigation of voiding the following challenges arise:

- Lack of reference samples for voiding: At present, no reference samples with known void content are commercially available for equipment calibration. Thin metal foils with drilled holes could be taken as reference, but still this is not the real PCB situation since void walls are not generally vertical in reality and thus detection of correct void size is more difficult. As an alternative a high-quality tomography could be chosen as reference if image resolution is significantly higher than for conventional X-ray imaging. Disadvantage of this concept is the high effort and the destructive procedure (high-resolution tomography requires a small sample size, in order to enable a sufficiently high number of projection directions by rotating the sample). Another approach could be realized by embedding small particles of known size featuring very low X-ray absorption (e.g. glass spheres) in solder joints, but this approach is not widely used. Thus, for this issue no satisfying solution has been found at present.
- Shadowing effects: A projection image of a PCBA contains not only contrast variations caused by solder joints and their voids, but all other structure above or below a solder joint, as components on the other PCB side, copper structures within the PCB as traces on outer and inner layers, buried vias etc. can result in pronounced contrast variations. These contract variations can affect the results of automated algorithms and can even make a manual voiding assessment difficult. Also solder joint thickness differences, as the difference in thickness between stand-off and meniscus of chip components, disturb image processing and analysis. This can result in slip, the non-detection of existing voids and pseudo-voiding, i.e. detection of non-existing voids caused by slightly brighter areas within solder joints.
- Influence of equipment settings on voiding results. As every X-ray image taken with a detector has only a limited dynamic range, optimizing illumination and detector sensitivity is crucial for voiding detection. A 'too dark' image tends to underestimate voiding levels, as voids may escape detection and the area of solder joints is maximized. On the other hand, a 'too bright' image tends to overestimate voiding levels, as areas of voids are maximized, whereas areas of solder joints may be determined as too small. For this reason, the use of 'bright' images generally leads to higher voiding results, whereas the use of 'less bright' images generally leads to lower voiding results (for such an assessment, see [3]).
- Influence of algorithm settings for void detection on voiding results. Similarly, to equipment settings, algorithm settings may have a pronounced effect on the obtained voiding results. In any algorithm, a threshold value will affect the identification of a certain region of a solder joint as a void. As an example, many algorithms rely on binarisation of measured images. Such binarisation thresholds obviously can have a major influence on the obtained results.

Some of the challenges can be addressed if X-ray inspection systems intended for manual operation are employed. A very thorough procedure is described in IEC 61191-6 [10], which addresses the X-ray investigation of voids in solder joints of

ball-grid and land-grid arrays. The method involves recording images of solder joints using two different illuminations, where an image taken with low tube voltage serves to detect the area of the solder joint, whereas an image taken with high tube voltage serves to detect the area of the void. Considering fixed printed board assemblies, a rather satisfactory agreement of the voiding levels determined with this approach by participants of a round-robin investigation has been found. However, most image analyses were done in manually and variations in shadowing effects were not taken into consideration. The latter can be detrimental for the reproducibility of voiding levels.
The above discussed challenges related to the investigation of voiding levels in mass production have also been realized by the working group DKE AK682.0.7. To address these challenges, a round-robin investigation among OEMs, Tier/EMS suppliers and equipment manufacturers has been initiated. In this round-robin investigation, various automotive electronic assemblies provided by the Tier1/EMS participants will be investigated for voiding/solder coverage by all round-robin participants. This will allow a very representative assessment of, in particular, the reproducibility of the measurements. The results will also enable conclusions on improvement potentials for Gage R&R performance. Results are expected until the mid of 2021.

Summary and concluding remarks

Voiding in solder joints is not generally a reliability concern unless untypical, excessive voiding levels are taken into consideration. Mass production, as it is required in automotive electronics, however, may result in a few assemblies with elevated voiding levels, as voiding generally exhibits considerable scatter, i.e. the full width of the underlying distribution function for voiding, including its tails, will actually occur in assemblies due to the large part count. This scatter, together with high reliability requirements for automotive electronics, may explain why the discussion on the acceptability of voiding is particularly lively for automotive electronic assemblies.

Consensus concerning voiding has been achieved among various stakeholders in the supply chain of automotive electronics for a set of solder joints geometries considered as most important. This consensus emerged from discussions among various stakeholders in the automotive electronics supply chain within a German standardization working group of the DKE (DKE – Deutsche Kommission Elektrotechnik), DKE AK682.0.7 ‘Assembly and Interconnect Technology in Automotive Electronic Assemblies’, considering typical voiding occurrence, typical environmental loads, required functional performance characteristics and processability conditions of solder joints. The such agreed requirements and criteria may serve as a starting point for discussions among additional stakeholders in the supply chain of automotive electronics.

As of today, X-ray inspection systems have very limited gage repeatability and reproducibility (G R&R) performance. This has also been addressed by working group DKE AK 682.0.7 by initiating a round-robin study on X-ray imaging G R&R performance. This study, in addition to documenting the current state-of-the-art, will also enable conclusions on improvement potentials for Gage R&R performance, to be implemented by equipment manufacturers.

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