System in Package (SiP) and CSPs Underfilling on Reliability

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Abstract
This paper presents assembly challenges and reliability evaluation by thermal cycling for a 2.5D [aka, System in Package (SiP)] in a fine pitch ball grid array (FPBGA). More importantly, it presents the effect of underfilling of the top CSPs assembled onto interposer on the overall SiP reliability behavior. A large number of variables were considered in the design of experiment including evaluation of bare FPBGA without parts on interposer, FPBGA balls either with SAC305 or SnPb solders, FPBGA fully/partially populated with CSPs and flip chip (FC) die on FPBGA interposers, and CSPs with and without underfills on the SiP interposer.

Assembly of mixed SiP packages becomes a challenging task and required to be characterized by X-ray for solder-joint quality and by Shadow Moiré analysis for warpage characterization. Acceptable assemblies with and without underfilling CSPs on interposers were then subjected to thermal cycling between –40°C and 125°C for reliability evaluation and failure-mechanisms assessment. Details of design, characterization by X-ray and Moiré, as well as reliability behavior of the SiP FPBGA due to thermal cycling exposures are presented. Failure analysis results also presented covering evaluation by optical, scanning electron microscopy (SEM), X-sectioning, and dye-and-pry evaluation. The Weibull plots of cycles to failures for SiP FPBGA with SAC305 and SnPb balls and CSP assemblies with and without underfills were presented. Finally, generic discussions were presented on the positive and negative effects of underfills at assembly level and specific reasons for early failures of SiP FPBGAs with CSPs assembled onto interposer with underfill.

KEY WORDS: SiP, system in package, 2.5D, Ball grid array, fine pitch BGA, FPBGA, solder joint reliability, underfill, thermal cycle, thermal shock cycle, Moiré, dye-and-pry

INTRODUCTION

Stack packaging—more than Moore's Law (MtM)—has now been widely implemented for use to increase the capabilities of commercial electronics because of increasing cost and limitation of die fabrication with finer features [1–3]. In addition, the increase in package density has further helped this miniaturization trend by using area arrays for interconnection rather than conventional packaging such as quad flat package (QFP) with peripheral leads [4–8].

System in package (SiP) is an MtM cofniguration that combines electronics parts/packages and integrated circuits (ICs) inside a single package. The SiP is different from system on chip (SoC) that integrates functional chips onto the same die within a package. SiP has been around since the 1980s in the form of multi-chip modules. Rather than put chips onto a printed circuit board (PCB), they can be combined into the same package to lower cost or to shorten distances that electrical signals have to travel. Die interconnections, historically have been through wire bonds; however, now connections are in the form of flip-chip die or other FPBGA packages.

While SiP saw limited adoption in its earliest forms, much work has been done on improving this concept recently with 2.5D and 3D ICs as well as package-on-package and flip-chip configurations. As stated by Rao Tummala and his co-authors [9], "Heterogeneous integration is necessary to continue the growth of electronics post Moore's Law." Electronic packaging integration enables faster and denser electronics by device-level integrations in 2D, 2.5D, and 3D using current stacking approaches. Stacking using inorganic laminates and Si interposers and next generation glass interposers, wafer fan-out, and embedding within printed circuit board (PCB) and packaging technologies. There are several key drivers for these changes.

These new MtM advanced electronics packaging technologies are fragile and are prone to early failures. To relieve stresses especially on fragile solder interconnections, underfill, which is a specially formulated polymeric adhesive that fills the gap between the die/package and substrate/PCB, is used to strengthen packaging system. Investigation of underfill behavior becomes extremely important with the recent emergence of advanced field programmable gate arrays and their use in high-reliability applications. For example, flip-chip ball grid array (FCBGA) package with a large number of solder balls under flip-chip die uses underfill within package under its die.

For the advanced packaging technologiee, the use of underfill under the die is necessary at the package level and may or may not be required at the assembly level, i.e., when these packages are assembled onto PCB. For flip-chip die, underfill is applied to fully cover the area under the die, whereas for package assembly, full or partial (such as an edge or corner)

coverage may be considered. Use of edge bonding is currently being investigated for commercial use whereas corner staking has been a common strengthening method for high-reliability applications.

For the past decade, the wider use of commercial electronics for mobile applications has led to extensive research to determine the effect of under-filling and more recently by edge-filling on enhancing reliability. Especially at the package assembly, underfilling is required to improve the resistance of fragile, high density fine pitch area array packaging assemblies under mechanical loading, such as repeated drops for mobile applications. However, the emphasis on mechanical reliability was not the case nearly two decades ago when most electronics applications were for office use only rather than current wider-uses including smart devices.

In early development of BGAs/CSPs, most commercial electronics applications were limited to thermally and mechanically controlled office use whereas the mechanical resistance aspects were required mostly for high-reliability applications. At that period, for high-reliability applications, R. Ghaffarian [10] and R. Ghaffarian and N. Kim [11] presented test data on the effect of underfilling on improving resistance of area array package assemblies under mechanical vibration.

Recently in 2014, R. Ghaffarian [12] and more recently in 2018, E. Suhir and R. Ghaffarian [13] presented two comprehensive reviews covering the state-of-the-art in the field of adhesive/underfill technologies for advanced electronic packaging technologies, including FPBGA and FCBGA, with an emphasis on high-reliability applications. The 2014 review addressed adhesive in electronics, curing methods, underfill and encapsulation techniques, application of flowable and no-flow underfills, fillers and filler particles, reworkable underfills, and the role of the underfill viscosity. Finally, it presented an extensive review of reliability test data including those for corner-filling, underfillin, and edge-bonding for BGA and column grid array (CGA).

The 2018 review addressed other attributes of FCBGA and FPBGA packaging technologies. It covered technologies and structural aspects including underfill induced stresses, the role of the glass transition temperature (Tg) of the underfill materials; some major attributes of the lead-free solder systems with underfill; reliability-related issues; thermal fatigue of the underfilled solder joints; warpage-related issues; and attributes of accelerated life testing of solder joint interconnections.

It has been shown by numerous authors that the effects of underfills on reliability are complex and even though analysis helps on narrowing the key parameters—nevertheless the test for validation is required. The complexity and inconsistency become apparent from widespread conflicting literature test data.

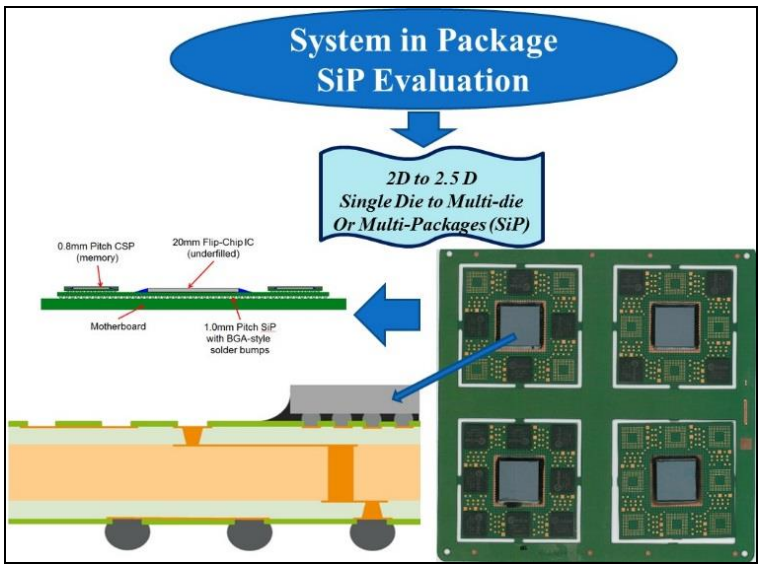

Fig. 1 SiP on a fine-pitch ball-grid array (FPBGA) interposer (on the right) with schematic drawing showing internal lay-up.

As schemetally shown in Figure 1, the SiP assembly configuration in this investigation is complex to begin with and investigation of the effect of underfill of CSPs at the coreners and centers adds further to this complexity. The paper presents not only assembly challenges and reliability evaluation by thermal cycling of SiP, it also compares thermal cycle reliability failure data with extracting specific failures to determine the effect of underfilling of the top CSPs on the FPBGA interposer.

Failure analyses indicate that the SiP FBGA solder joint life was significantly impacted by these variables, especially underfilling of CSPs on interposer.

SIP ASSEMBLY PROCEDURES

SiP Test Vehicles

The interposer FBGA of the SiP body was designed and assembled by the package supplier. The FPBGA package was populated with 3364 area array balls with 1.0-mm pitch. The interposer had an area of 60 × 60 mm^2 with 0.9-mm thickness utilizing blind and buried via structures providing signal conduction between the layers.

The SIP interposer with the flip-chip die assembled at the center and the CSP pattern surrounding the FC before the CSPs are assembled on the top of interposer. The interposer constructed using daisy-chain pattern to complement the IC and CSP daisy-chain patterns. The CSP simulates a memory package and had 160 solder balls ChipArray® ball-grid array (CABGA 160), 12 × 12 mm, with SAC305 balls (bottom image).

Interposer Warpage Characterization at RT to Reflow

Shadow Moiré analysis was performed during the reflow cycle to determine warpage deformation behavior of the SiP interposer alone (with no CSP) with temperature. The SiP-interposer deformation was measured at temperature intervals during ramp up at 25°C (room temperature, RT), 100°C, 150°C, 215°C, and 245°C. During ramp down it was measured at 215°C, 150°C, 100°C and 25°C. Analysis evaluated the free-body deformation across the FBGA bump side and for each component. The temperatures were selected to coincide with milestone temperatures experienced during typical lead-free reflow processes, including peak reflow temperature (245°C) and the expected solder solidification range of 215°C to 150°C. Figure 2 shows a typical Shadow Moiré color-coded warpage configuration for a bare SiP interposer.

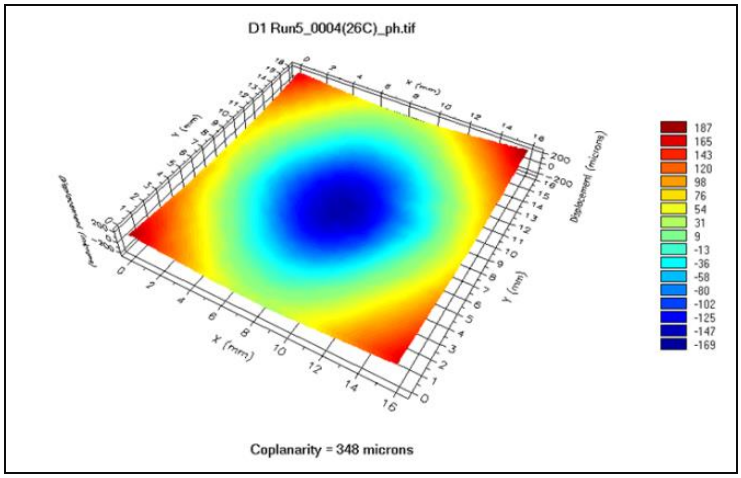

Fig. 2 Shadow Moiré contour plot at 25°C for a non-populated SiP FBGA interpose. Image is produced "ball side up" and indicates that the center of the package would be raised above the board surface.

Figure 3 shows plots of a number of interposer warpage profiles from RT to reflow temperatures. Image is produced "ball side up" and indicates that the center of the package would be raised above the board surface at RT during assembly. The contour plots indicate that the devices are significantly warped at room temperature, with coplanarity on the order of 320 to 350 microns. The results of the analysis indicate that the interposer has an extreme convex (corners up) shape profile for "ball side up" at RT that rapidly flattens with a slightly concave at elevated temperatures. This means that during assembly, balls become closer to PCB (ball-side down). The interposers are reasonably flat at solder solidification temperatures (215°C to 150°C).

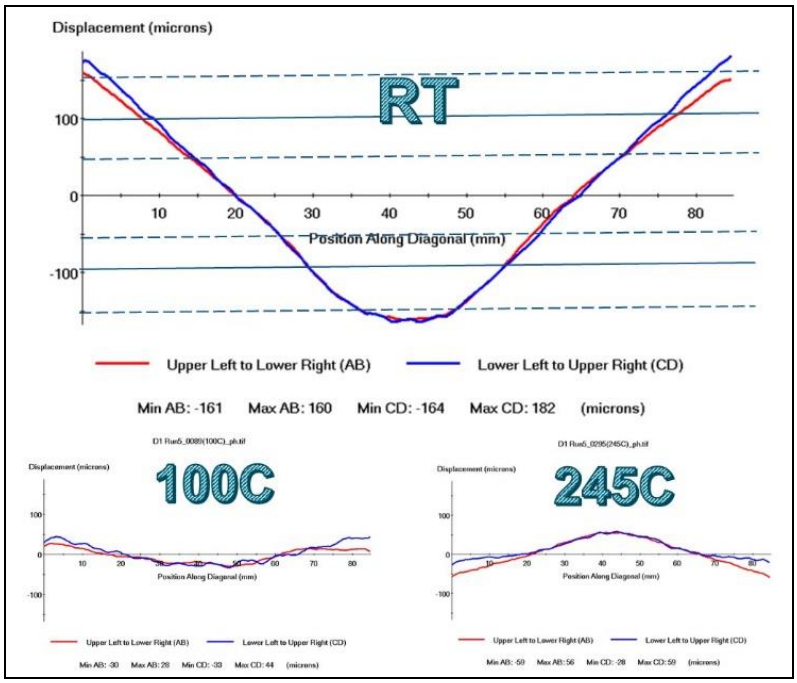

Fig. 3 Shadow Moiré diagonal plots for RT to reflow temperatures showing change in curvature sign and near flatness near the reflow temperatures. Images are for "ball side up" FPBGA.

Assembly and Inspection Processes

The basic process flow used to construct and evaluate the test assemblies was:

1. Print solder paste over the interposer
2. Place the SiP and the interposer CSP (with and without dip flux, as needed)
3. Dip flux and place the CSP on the SiP as required
4. Perform reflow soldering
5. Perform X-ray inspection
6. Perform the daisy-chain verification test

Reflow was performed using a convection reflow oven with 10 heating and 3 cooling zones. All assemblies were inspected by X-ray to characterize quality of the solder joints prior to environmental exposures. The X-ray inspection was primarily focused on characterizing voids in the solder joints and identifying solder bridging, if any. Both CSP and FBGA solder joints were inspected. Of 80 SiP assemblies, only two were found to have workmanship defects. One defect was attributed to a placement error during the pick and place process, which resulted in the SiP being placed one row off in the y-direction. The other defect was due to solder bridging. The solder-bridge defect occurred in a SiP assembled with SnPb solder. The X-ray images showed that six solder-joint pairs located at the center of the device had bridged (See Figure 4).

The reason for the bridges is unknown, but bridging at the center of a package often occurs due to the deflection profile of the device resulting either in a convex (corner ball up) or concave (corner balls down) that in both cases results in increased loading, leading to excess solder ball stretching or collapse and possible bridging. This is especially prominent for the concave condition. Based on the Shadow Moiré results, these defects most likely occurred while the samples were near the peak reflow temperature, when the parts demonstrated concave warpage of 120 to 140 microns (0.12 to 0.14 mm) at the center of the FBGA interposer.

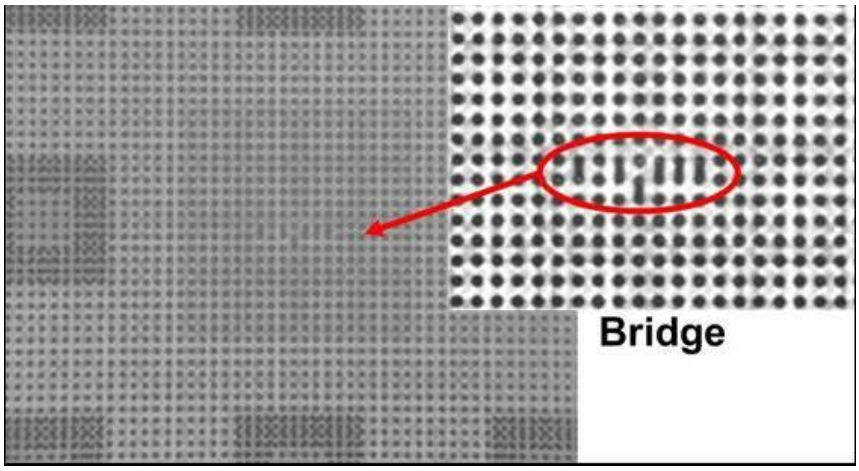

Fig. 4 Solder bridging at the center of device in the SiP interposer.

The other goal of the X-ray inspection was to characterize solder-joint void levels. In most cases, the number and/or size of voids observed in the CSP or SiP FBGA solder joints were negligible. However, the SnPb test cell did produce large and numerous voids in the SiP FBGA. Interestingly, the voids were primarily located near the center of the package as shown in Figure 5.

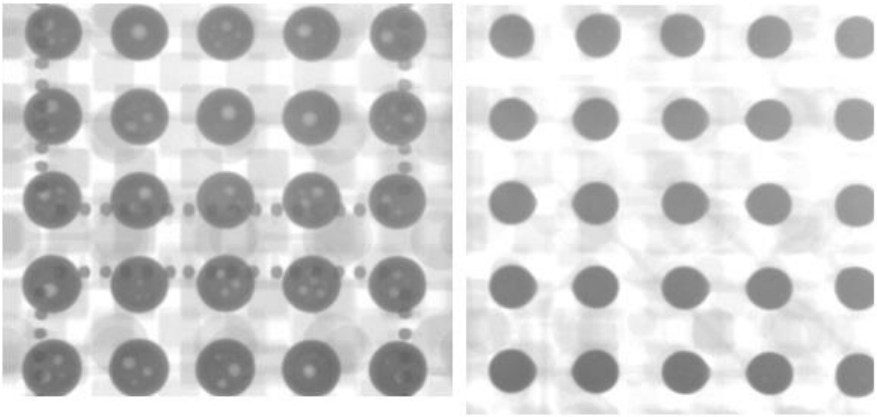

Fig. 5 Comparison of voids near center of SnPb SiP (left image) and perimeter of SiP (right image).

THERMAL CYCLE AND FAILURE ANALYSIS TEST RESULTS

Thermal Cycle Test Results

The SiP assemblies with acceptable daisy-chain continuity levels were subjected to accelerated thermal cycle testing in order to evaluate solder-joint reliability. During thermal cycling, an event detector was used to detect resistance spikes, exceeding 500 ohms and lasting in an excess of 200 nanoseconds per IPC 9701 [14] capturing solder joint failure during thermal cycling. Accelerated thermal cycling was performed between –40°C and 125°C with 15-minute dwells at the temperature extremes with a total cycle of 74 minutes. Figure 6 shows a typical warpage analysis performed on a SnPb solder SiP assembly after 2838 thermal cycles and prior to failure analyses. This figure shows that SiP curling up at the corners, imposing peeling stresses on the corner solder joints. Note that daisy-chain resistance measurement indicated that SiP (FPBGA solder joints) and all CSP solder joints had failed during cycling. In addition, during preparation for failure analysis, the center IC fell during cleaning process for cross-sectioning preparation.

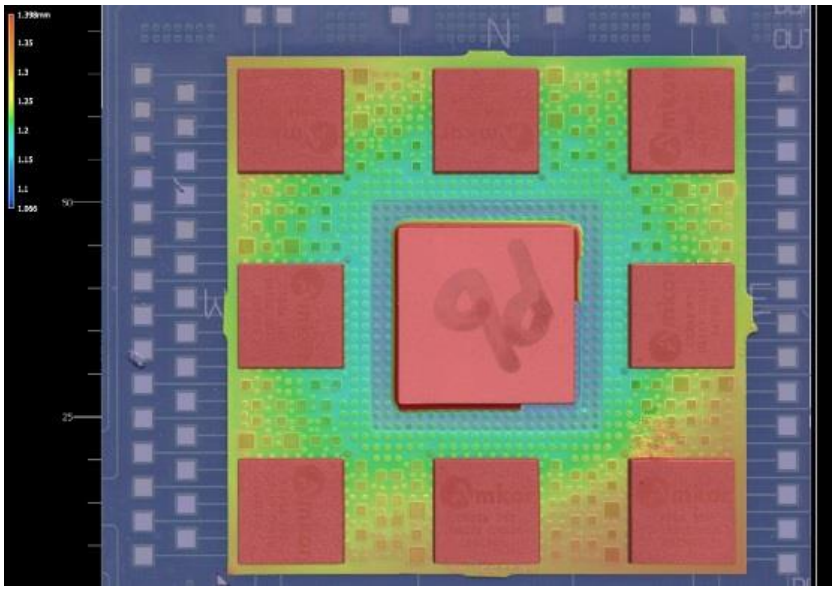

Fig. 6 Visual representation of SiP warpage SiP after thermal cycling with corner having the highest values. (Units for the values shown in the upper left are in millimeters.)

A large number of variables were considered in the DOE design including evaluation of bare FBGA and FBGA balls either with SAC305 or SnPb solders, FBGA fully/partially populated with CSPs and flip chip (FC) die, and CSPs with and without underfills on a SiP. Failure analyses indicate that the SiP FBGA solder joint life was significantly impacted by these variables. The first cycles-to-failures, which is critical for high-reliability applications, varied from about 300 to 1500 cycles. The Weibull plots were generated to determine failure characteristics and beta values for failure distributions. The Weibull failure characteristic life ranged from about 500 to 2000 thermal cycles and beta distribution from 2.5 to 7.5 revealing these variables affected significantly the integrity of SiP by inducing different failure mechanisms. Only a few aspects of these parameters and their effects are discussed in the following with failure mechanisms. For a SiP with SnPb solder balls and SnPb assembly, detailed failure analyses were presents to cover the aspects of SnPb use for high-reliability applications. For SnPb solder balls, X-ray of assembled SiP indicated higher levels of voids. Failure analyses were further verified by destructive dye and pry methods to determine the effect of voids on reliability.

Figure 7 shows failure accumulation percentage versus the number of thermal cycles for only three key SiP assembly conditions. The three conditions revealed the effect of CSP assembly condition on the SiP FPBGA with SAC305 or SnPb balls/joints. These conditions included the SAC305 SiP with all CSPs underfilled and SAC305 SiP or SnPb SiP with all CSPs not underfilled. The SiP FPBGA with underfilled CSPs showed the lowest cycles-to-failures indicating the negative impact of underfill on the SiP reliability even though the CSP assemblies had high reliability with no failures during the same cycling period. The lowest CTFs were for a SAC305 FPBGA with the eight CSP assemblies with underfill. For this case, the first failure was detected at 325 cycles and with the Weibull characteristic lifetime of 512 cycles (–40°C to 125°C) and beta distribution of 5.4. Cycling for this case was stopped after only 800 cycles because 7 out of 8 CSPs were had already failed.

For this SiP condition, an increase in cycles-to-failures was observed when CSPs were not underfilled. The SAC305 SiP with all CSPs without underfill showed the first failure at 455 cycles. The Weibull characteristic lifetime increased to 1339 cycles, but with much wider beta distribution of 2.5. Detailed analysis of the data revealed that wider distribution is related to failure mechanism changes. As shown in the figure, for the no underfill condition, failures occurred at the corner CSPs followed by the edge-center CSPs. For underfilled condition, all failures occurred at the corner CSPs. The possible theoretical reasons for earlier failures of underfill versus no underfill conditions are discussed in the following section.

The SnPb SiP with all CSPs without underfill showed even higher cycles-to-failures compared to the SAC305 under the same condition. The first failure for the SnPb case was at 925 cycles. The Weibull characteristic life increased to 1577 cycles with beta distribution of 5.7. The higher CTFs and narrower distribution possibly is due to failure mechanism. The SnPb SiP showed no failures at the corner CSPs, but failures at the mid-section CSPs and the center IC.

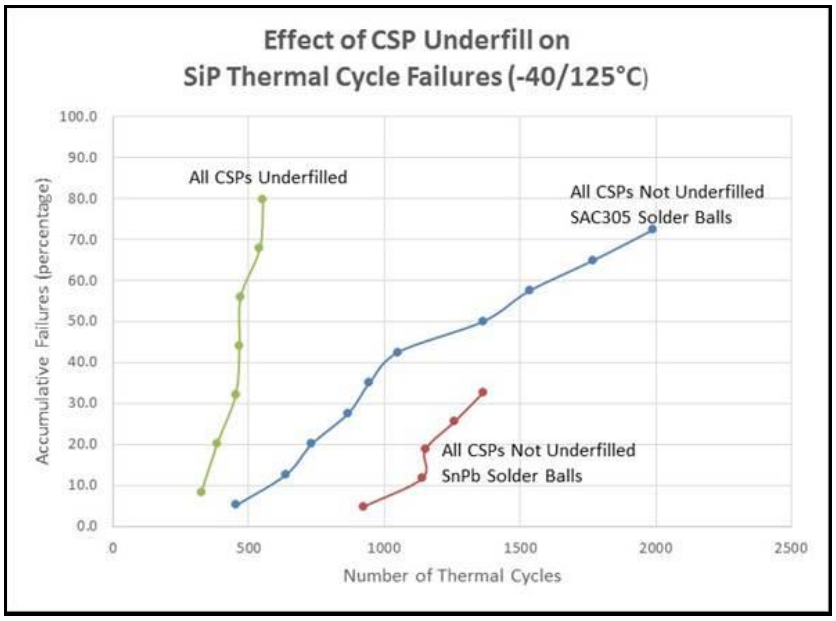

Fig. 7 Accumulative cycles to failures for SiP with all CSPs underfilled or no underfill condition for SAC305 and SnPb solder joints.

Failure Analyses

It was shown that failure mechanisms changed by the type of SiP assembly and solder alloy type. Extensive failure analyses were performed to narrow failure mechanisms for various SiP assembly conditions. Detailed failure analysis presented only for the SnPb SiP assembly with all CSPs assembled onto the SiP interposer (no underfill) and IC at the center with underfill. Figure 8 shows a representative optical image of SiP FPBGA with SnPb solder joints at the PCB level. There are signs of microcracks at 2838 cycles, but no failures even though all CSPs had already failed. Failures may have occurred at the other locations. Destructive dye and pry should reveal such potential failures. Figure 9 shows a representative of optical image for the center CSP, it shows complete cracking of most solder joints including the two shown at a higher magnification. Similar conditions were characterized for the two CSPs at the corners, but not shown in this paper.

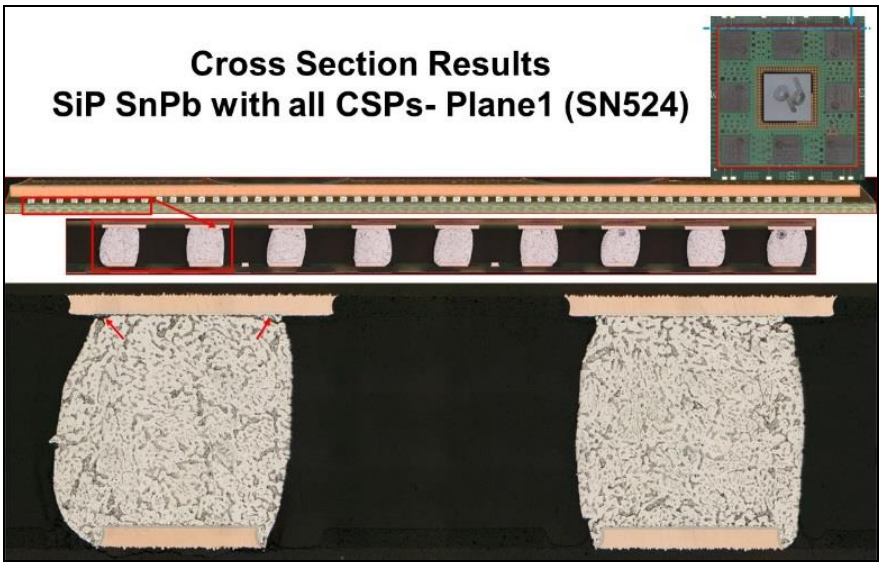

Fig. 8 Representative of optical microscopy of SnPb SiP after 2838 cycles (–40°C to 125°C) showing no signs of failure at this cross-section even though the assembly has already failed.

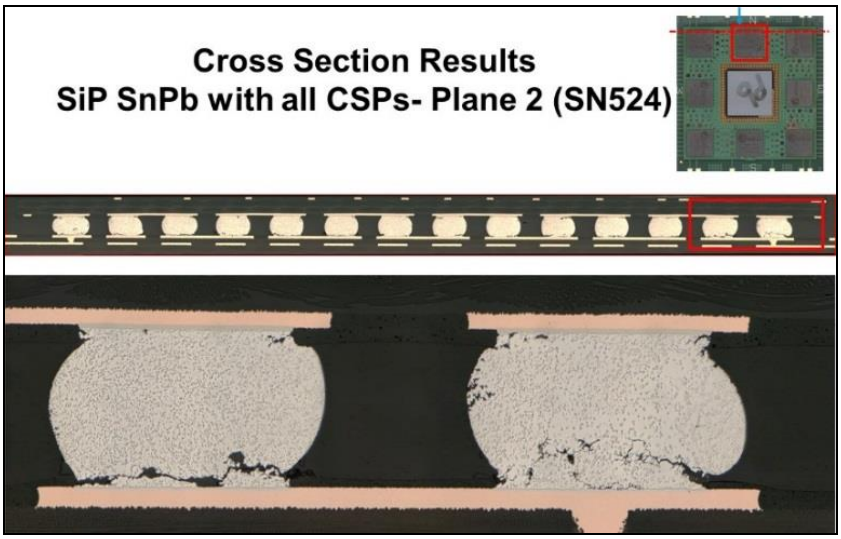

Fig. 9 Representative of optical microscopy of SnPb SiP after 2838 cycles (–40°C to 125°C) showing signs of full cracking at a number of solder joints.

Dye-and-pry failure analysis is another valuable approach that is simple and should provide an insight into the all solder-joint conditions. This method was used to determine failure locations, to verify daisy-chain resistance opens, and to also to define the site of failure (PCB or package) enabling an extensive verification beyond cross-sectional results. Figures 10-11 show the FPBGA and CSP solder joint interfaces after dye-and-pry showing stained red at interposer substrate and at the package pads. Areas of red dye are apparent on most pads; however, only a small number of pads either at the board for FPBGA assembly and at the substrate for CSP assemblies, showed full red coverage. The lack of full red stains indicates that there were a limited number of solder-joint failures at FPBGA and CSP sites.

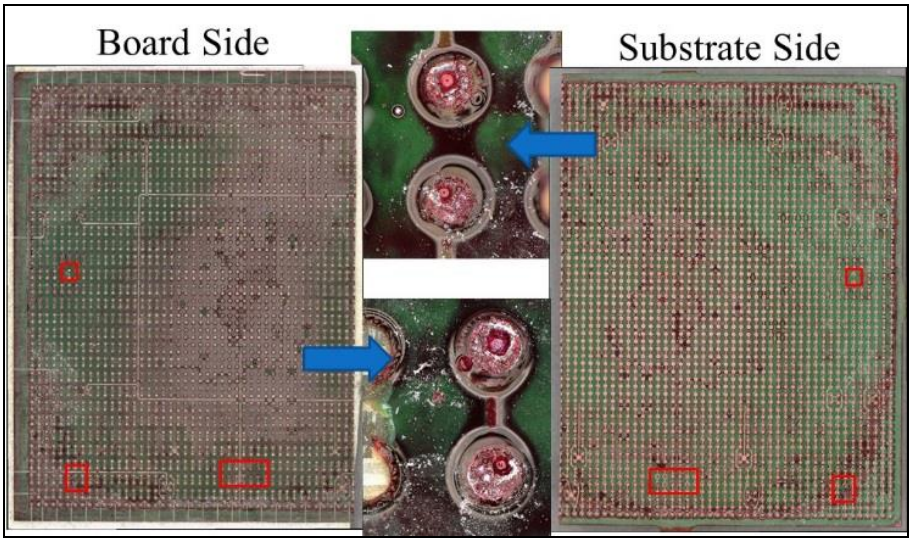

Fig. 10 Representative of optical microscopy after dye and pry of SnPb SiP after 2838 cycles (–40°C to 125°C) showing signs of voids and failures (full red color coverage).

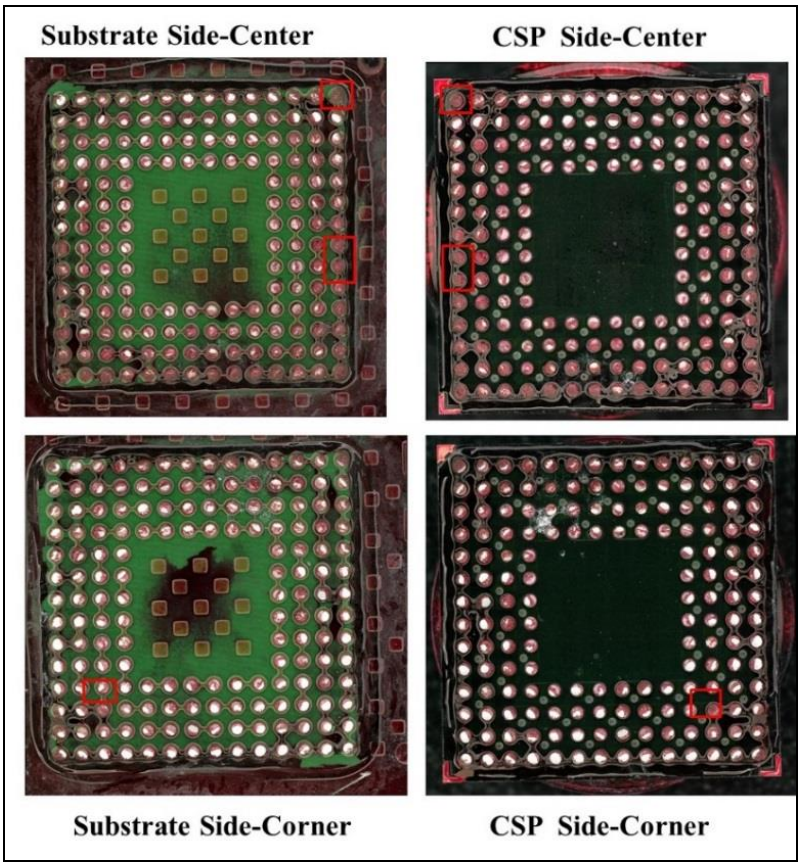

Fig. 11 Representative of optical microscopy after dye and pry of SnPb CSP on FPBGA substrate after 2838 cycles (–40°C to125°C) showing signs of failures (full red color coverage) at the corner and center of CSPs.

DISCUSSION:

General: Effect of Underfill

Conventional underfill uses the capillary behavior of resin, whereas other underfills (e.g., snap cure) are developed to improve processing throughputs. Early reliability test data for flip-chip die indicates that underfill significantly improves thermal cycle resistance. However, the level of improvement in thermal cycles to failures for flip-chip die depends on the adhesive's and the adherent's material characteristics.

In general, FEA models predict that an order of magnitude increase in thermal cycle reliability. These predictions are unrealistic because they conflict with test results. Test data show that the assumption of failure by solder joint may not be realistic—especially for new fragile packages/substrates— since failures occur due to the weakest link being interfacial bonding. Interfacial failure induces delamination initiation and progression with subsequent solder joint failure. Change in the local state of stress from shear to tensile plays a key role in inducing interfacial failures. Therefore, underfill adhesion and interfacial strengths at die/substrate as well as at the package level are key factors that should be considered for reliability projections with subsequent verification by testing for adjustment of the model parameters.

At assembly level, however, different failure modes are observed in reliability testing with sometimes conflicting requirements on filling material properties to address a specific packaging configuration. For example, high modulus underfill property is desirable to effectively couple the stress on solder joint, but low modulus is required to minimize residual stress due to thermal curing. In addition, a high modulus also could cause interfacial delamination causing solder failures. Therefore at assembly level, underfill have positive and negative impacts under thermal cycle testing. It may have negative effects if there is not an appropriate CTE match to adherents with enough stiffness and rigidity.

Specific: Effect of CSP Underfill in SIP

In early stage of introduction of chip-size packages, R. Ghaffarian [10] evaluated the effect of underfill on a large number of CSP assemblies under two thermal cycle conditions (–30°C to 100°C and –55°C to 125°C). The impacts of underfill on reliability were categorized in three groups: (1) improvement for quad flat no-lead (QFN), (2) minimal impact for chip-on-

flex, and (3) reduction in cycles-to-failures due to underfilling for the tape automated bonding (TAB) CSP assemblies. The TAB CSP was the only package that specifically was developed at that time to meet the high demand of thermal cycle requirement without requiring underfilling. The package internal TAB leads was designed such to reduce the CTE mismatches between package and board. However, as thermal cycle results indicated, the CTE mismatches were disturbed by underfill materials inducing different CTE mismatches and stress conditions, and therefore resulted in the underfill to have a negative impact under cycling.

Recently, K. Dhandapani et al. [15] presented experimental test results and discussed factors that affect PoP BGA assemblies, especially during accelerated temperature cycle (ATC) conditions. Under thermal cycling (–40°C to 125°C), the underfilled PoP assemblies (underfill materials identified as letter A to letter C) showed a drastic reduction in reliability versus the control assembly without underfill. Only underfill D improved reliability.

Our finding is new. Therefore, the negative reliability effect of CSP underfill on SiP under thermal cycling conditions needs further discussion. Reliability under thermal stress for SiP package and assembly affected by constituent elements and global/local interfaces. Solders in surface mount are unique since they provide both electrical interconnection and mechanical load-bearing elements for attachment of SiP package on PCB. So, three elements play key roles in defining reliability for SiP, global, local, and interconnections. The characteristics of these three elements affect thermal cycle reliability characteristics and failure mechanisms.

A majority of fatigue failures of solder joints in SiP assemblies are due to induced damage by global CTE mismatches, which result from differential thermal expansions of the SiP package and the PCB assembly and their rigidities. These thermal expansion differences stem from differences in the coefficients of thermal expansions (CTEs) covering the CSP and FC die assemblies and underfill condition. The shear strain representative of the global CTE mismatch due to thermal excursion is given as the following:

$$\Delta\gamma = (\alpha_{SiP} - \alpha_{PCB})\,(Tc - T_0)\,L_d/h = (\Delta\alpha)\,(\Delta T)\,DNP/h$$

Global CTE mismatches typically are the largest, since all three parameters determining the thermal expansion mismatch, i.e., the CTE-mismatch ($\Delta\alpha$), the temperature swing (ΔT), and the largest acting package length (L_d), a.k.a., distance to neutral point (DNP), can be large. In thermal cycling, this global expansion mismatches will cyclically stressed, and thus fatigue, the solder joints. The stress level on SiP assembly also affected by the local stiffness changes for FBGA due to addition of CSP/FC, solder balls and joints, and PCB. Considering this background, now, the possible reasons for early failure of SiP with CSP underfill and improvement without CSP underfill are as follows:

1. For this design, CSPs are located at the corner of SiP, The addition of CSP with underfill at these corners increased induced stresses due to local increase in rigidity. In addition, warpages are highest at the corners of SiP (see Figure 2) that add tensile stresses in addition to shear stresses due to global CTE mismatches. Combination of the two types of stresses increase the state of stresses on the corner of SiP; therefore, decreasing the fatigue life.
2. When CSPs on FBGA interposer are not underfilled, the local stiffness at a corner of SiP decreases relative to the CSPs with underfilled condition. This decrease in stiffness condition expected to increase cycles-to-failures. The thermal cycle test data shows this trend, cycles-to-failures for underfilled condition were in the range of 325 to 512 that were increased to 455 to 1339 cycles for the assemblies with CSPs without underfill. However, it was noticed that also there is a failure mechanism shift from the corner to the center CSP at higher cycles.
3. There was an improvement in CTFs for SnPb solder balls relative to SAC305 SiP FPBGA assemblies. Daisy-chain failure analysis revealed that even early failures occurred at the center CSPs with no failure at the corners. It is known that SnPb is more ductile than SAC305, which indicate potential earlier failure for SAC305 at corner balls with higher shear tensile stresses.

Fatigue inversely proportional to SiP stiffness and $(\Delta T)^2$. The cumulative fatigue damage will ultimately cause the failure of one of the solder joints, typically corner joints in complex BGA or the corner of the die within the package if the stiffness of die becomes a dominant factor in a full array BGA assembly. The effect of alloy of solder balls and solder joints also shown to play a key role in failure mechanisms and cycles-to-failures established by the weakest link in the SiP assemblies.

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REFERENCES

[1] *International Technology Roadmap for Semiconductors*, ITRS (web page), http://www.itrs2.net/itrs-reports.html, accessed Dec., 2018.

[2] *International Electronics Manufacturing Initiatives* (web page), INEMI, http://www.inemi.org/inemi-2017-roadmap-1, accessed Aug. 1, 2018.

[3] *IPC, Association Connecting Electronics Industry* (web page), http://www.ipc.org, accessed 8/1/2018.

[4] Ghaffarian, R., "Update on CGA Packages for Space Applications," *Microelectronics Reliability* (2016).

[5] Ghaffarian, R., "Thermal Cycle and Vibration/Drop Reliability of Area Array Package Assemblies," Chapter 22 in *Structural Dynamics of Electronics and Photonic Systems*, eds. E. Suhir, E. Connally, and D. Steinberg Springer, 2011.

[6] Ghaffarian, R., "Area Array Technology for High Reliability Applications," Chapter 16 in *Micro-and Opto-Electronic Materials and Structures: Physics, Mechanics, Design, Reliability, Packaging*, ed. E. Suhir, Springer, 2006.

[7] Ghaffarian, R., "BGA Assembly Reliability," Chapter 20 in *Area Array Packaging Handbook*, ed. K. Gilleo, McGraw-Hill, 2002.

[8] Fjelstad, J., Ghaffarian, R., and Kim, Y.G., *Chip Scale Packaging for Modern Electronics*, Electrochemical Publications, 2003.

[9] Tummala R, Nedumthakady N, Ravichandran S, DeProspo B, and Sundaram V., "Heterogeneous and homogeneous package integration technologies at device and system levels," *SMTA Pan Pacific Microelectronics Symposium 2018*, IEEE, pp. 1–5, 2018.

[10] Ghaffarian, R., "Long-Life Reliability of CSP Assemblies With And Without Underfill". Proceedings of SMTAI (2002)

[11] Ghaffarian, R., Kim, N., "Vibration Behavior Of CSP Assemblies With and Without Underfill". Proceedings of SMTAI (2003)

[12] Ghaffarian, R. "BOK─ Underfill Optimization for FPGA Package/Assembly", (web page) https://nepp.nasa.gov/files/23820/12_139_JPL_Ghaffarian_BOK%20Underfill%20Optimization%20for%20FPGA%20Package%20Assembly%20jpl%20pub%2012_13%20rec%209_29_12.pdf, accessed, Dec. 2018

[13] Suhir, E., Ghaffarian, R., "Flip-Chip (FC) and Fine-Pitch-Ball-Grid-Array (FPBGA) Underfills for Application in Aerospace Electronics—Brief Review." Aerospace 5, no. 3 (2018): 74.

[14] IPC 9701 Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments, http://www.ipc.org

[15] Dhandapani, K., Zheng, J., Roggeman, B. and Hsu, M., "Improving Solder Joint Reliability for PoP Packages in Current Mobile Ecosystem". In 2018 IEEE 68th Electronic Components and Technology Conference (ECTC) (pp. 1645-1650). IEEE.