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Single Device Traceability in Assembly without ECID

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Application-specific tracks: Automotive …
Topics of interest: End-to-End Data Analysis, Traceability

Abstract:
Use cases, solutions and standards for single device traceability in the supply chain to enable root case analysis, recall containment, device pairing, yield and reliability improvement and liability protection.

Introduction

Single device tracking (SDT) refers to the tracking of individual electronic assets such as dice, packages, PCBs, etc. The quality, reliability, performance and security of an asset is determined by its components (assets and consumables) and the process steps and conditions used to manufacture it.

The recent evolution of data analytics allows correlation analysis from wafer fab to wafer test to assembly and packaging to product level test and field performance. Such analysis offers further in-depth yield learning and may identify new issues such as silicon test coverage gaps and systematic and random defects introduced at assembly or found only during product level or system level test.

SDT offers many advantages such as…

- Higher reliability for automotive, medical, network and military applications
- Faster volume ramp for New Product Introductions (NPI)
- Early Life Failure (ELF) prediction
- Rapid and detailed response to field failures
- Swift recall containment and liability protection
- Improved product yield and cost reduction
- Accurate device calibration at all test stages
- Counterfeit prevention

…but its deployment is not as widespread as it should be. This paper will explore the reasons why now is the time to invest in comprehensive single device tracking.

Limitations of Existing Methods: Unique Electronic Identifier (ECID)

A first step for many companies to provide SDT is to use electronic chip IDs or ECIDs. While ECIDs can be used for some aspects of SDT such as the correlation of final package test data to wafer test data, there are many limitations for ECID-based SDT including:

- Inability to identify yield loss and failures caused by the assembly process
- Inability to correlate tests with devices in a multi-chip module (MCM) if they don’t all have ECIDs
- Requires tester or PCB insertion to read ECIDs
- May not be available at higher level assembly, e.g. printed circuit board (PCB), test
- May become unreadable if device fails or cannot be powered up
- Some devices (e.g. MEMS) inherently cannot support ECID

Traceability without ECID

The figure below shows an example of an MCM and all the die and other materials that are included in it and may affect its performance, reliability, etc.

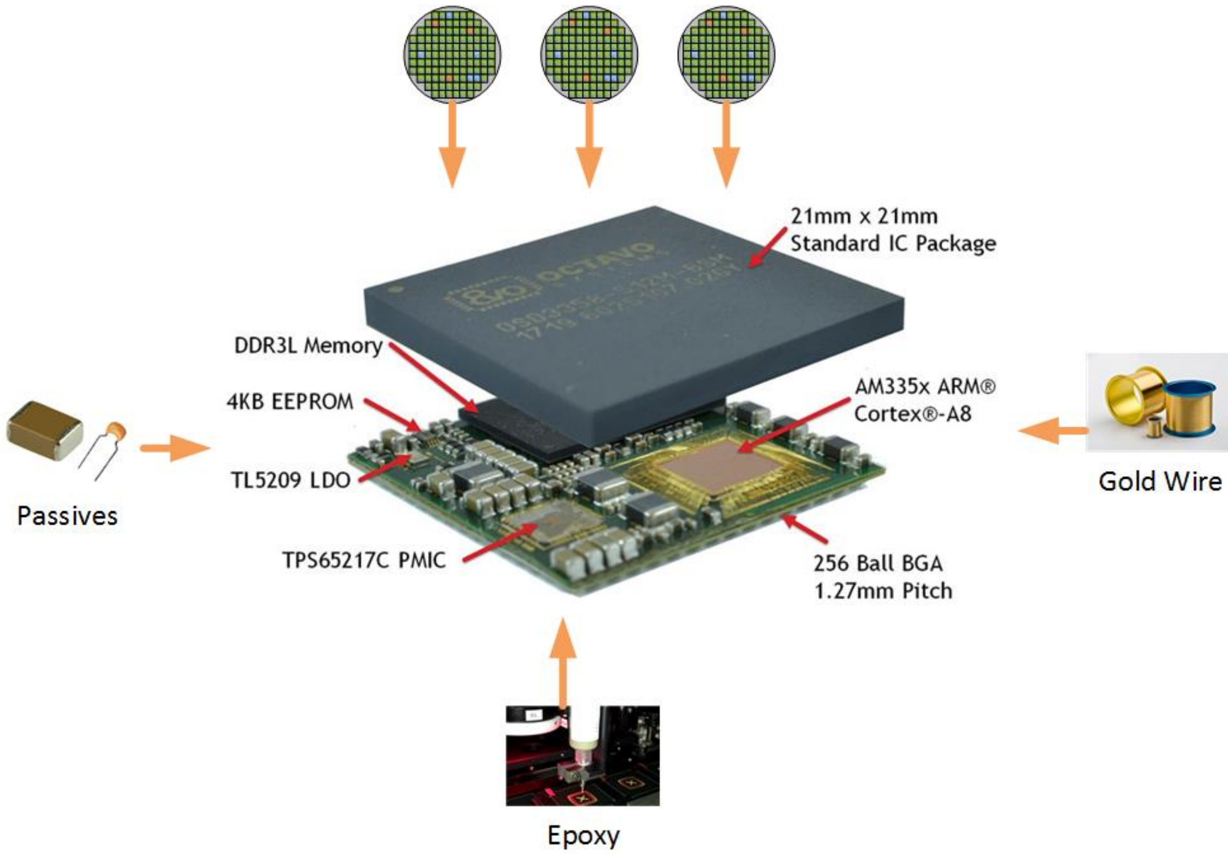

Figure 1: Tracking what goes into a Multi-chip Module Package

Let's assume that none of the die in the MCM can support ECID. How is it possible to track the package and the die it contains back to the wafer and XY location it came from? The answer is to collect data from the assembly processes that pick and place the die into the package and the laser marker that marks the package with a unique 2D matrix code. This package ID can then be read at final test and included in the test data logs thereby completing the traceability. See below.

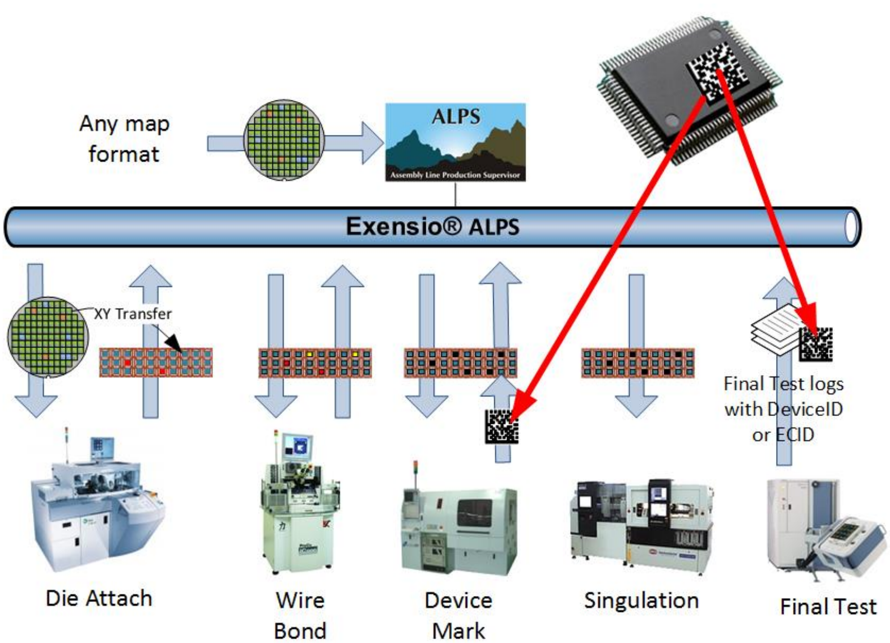

Figure 2: Singe Device Tracking in Assembly Process Flow (courtesy: PDF Solutions)

This diagram does not show the complexity of mapping the MCM packages on the strip. The SEMI E142 substrate mapping standard (E142) defines how to represent complex assemblies such as MCMs, PCBs, and more and map data to the single devices within that structure. It is the adoption of E142 by assembly equipment vendors that has made single device tracking in assembly possible and cost effective.

E142 can represent the structure of any electronic asset (e.g. MCM, PCB) and where its composite assets (e.g. die, package, raw materials) came from. All sorts of process information can be associated with this structure such as bin codes, package / PCB identifier, process step, equipment, process variables, etc.

SEMI E142 is not limited to mapping wafers and strips. The diagrams below show an MCM is being assembly on a strip from 3 different wafers and some other materials and a few examples of how different kinds of substrates[1] can be mapping with SEMI E142.

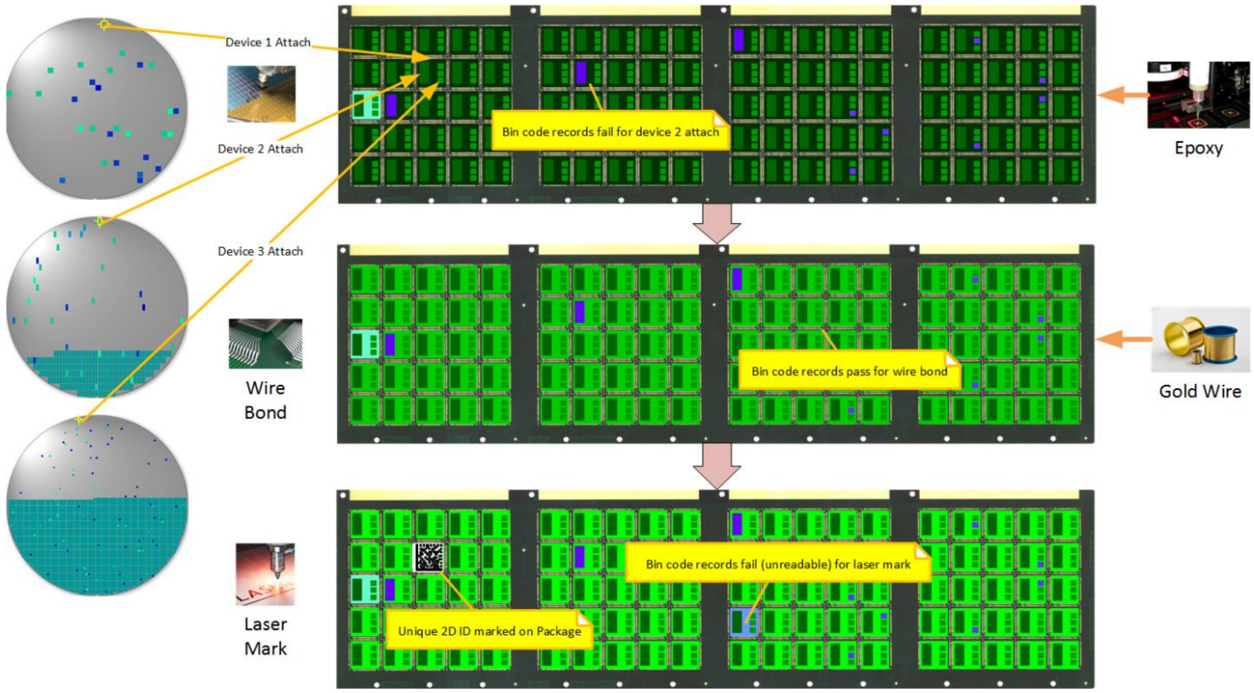

Figure 3: SEMI E142 allows precise tracking of die and materials in the assembly of complex packages (courtesy PDF Solutions)

[1] SEMI E142 defines Substrate as "any carrier of a two-dimensional array of devices including, but not limited to: wafers, trays, strips, tape, panels, or boards". The standard is not strictly limited to two-dimensional structures. It allows, for example, stacked packages.

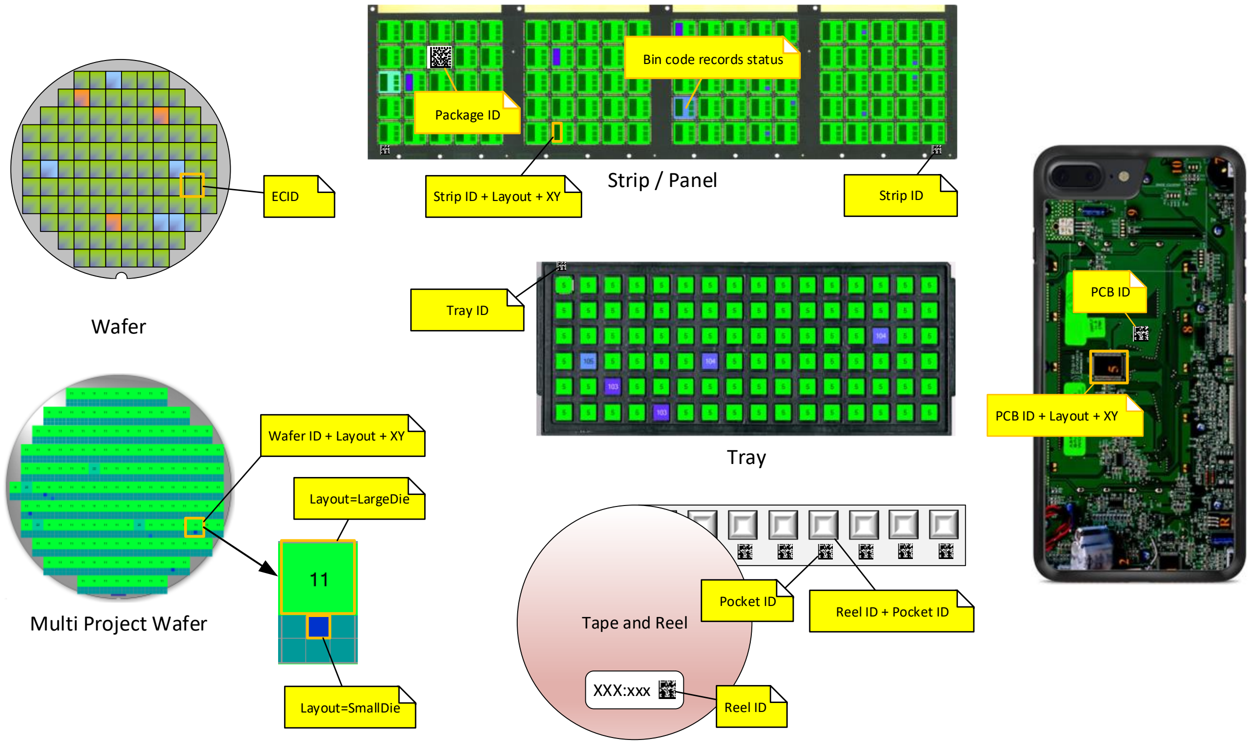

Figure 4: Examples of how "Assets" in the electronic manufacturing supply chain can be uniquely identified (courtesy PDF Solutions)

Some Use Cases requiring SDT without ECID

Medical application: SDT deployed in 2008
A six die MCM is the key component in a medical device to be embedded in the patient. None of the die in the MCM could support ECID. This used to be assembled in house but, to save cost, the assembly was outsourced to an offshore assembly and test (OSAT) facility. The lot size grew orders of magnitude to 5000+ and, since only lot level tracking was available, failures or recalls would cause the whole lot to be scrapped or recalled.
This became too expensive and the public relations impact was intolerable. ALPS[2] SDT was deployed at the assembly facility which transferred the SDT data back to the US where final test took place. Root cause analysis of failures typically identified a single wafer or process equipment which might affect only 100-200 devices. With ALPS SDT the scrap or recall can then be contained to these few devices.
The return on the investment in $ terms was less than one year. The positive public relations impact is hard to quantify but difficult to overestimate.

Mobile phone application 1: SDT deployed in 2016
An MCM including a MEMS device is the key component in a mobile phone. None of the die in the MCM could support ECID. There were several issues that needed to be resolved:

- It took 3 months to track it down a catastrophic yield loss to a single assembly tool at the OSAT.
- Yield loss at final test was unexplainable without correlation with the wafer test results.
- Their biggest customers demanded that they have SDT to win the contract.

ALPS SDT was deployed at the OSAT and the data was uploaded to the Exensio[3] analytics platform which also contained all the wafer and final test results. With more visibility into the assembly process, the root cause for the catastrophic yield loss event could have been identified in hours rather than months. Correlation between wafer and final test results enabled them to improve their front-end processes and weed out potential final test failures prior to assembly. They were able to demonstrate their SDT capability with ALPS to win the big contracts.

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[2] The Assembly Line Production Supervisor (ALPS) is a product from PDF Solutions that provides defect mapping and single device tracking for assembly based on SEMI E142.
[3] Exensio is a family of products from PDF Solutions providing big data analytics for the enterprise across wafer fab, test, assembly and final test. Exensio may be integrated with ALPS.

Mobile phone application 2: SDT deployed in 2017

Several die, some for external sub-contractors, were assembled into an MCM. None of the die in the MCM could support ECID. Two of the die had to be paired at final test which involves looking up the parametric wafer test results for die A and programming them into die B and vice-versa.

ALPS was deployed at the assembly site and the SDT data enabled the lookup of the parametric wafer test results at final test. Without pairing enabled by ALPS SDT final device would not function correctly and the important contract would not have been won.

Deploying SDT

For each member of the supply chain[4], the following steps need to be taken:

- Mark substrates (wafer, strip, tray, reel, PCB, etc.) with unique IDs
- Identify process steps to be traced
    - This must include any steps that transfer assets between substrates or associates the package ID with the substrate and location
    - This should include process step that could introduce defects or early life failures, e.g. wire bond
- Identify equipment supplier, make and model for each process step
- Equipment must be capable or upgradable to read the substrate ID, support E142, and report processing (e.g. die attach, laser mark, inspection, test, etc.) per device with the location on the substrate.
- Develop or purchase a system to manage the data and make it available for analysis.

The lead-time and cost for such deployments was prohibitive in the past, but increasingly equipment vendors are supporting E142 and software vendors are offering the corresponding data management, reporting and analysis as off-the-shelf solutions. It is expected that this trend coupled with market intolerance for less than perfect reliability and security will ensure that SDT deployment will become commonplace over the next 10 years.

Conclusion

Single device tracking without ECID will become a mandatory requirement for a wide range of applications, not just the high reliability segments like medical, automotive and military, but relatively low cost and less critical consumer products also. The high reliability products continue to require near perfect reliability, i.e. zero defects in the field. The challenges inherent in the very fast ramp to high volume for new consumer products drives the requirement for single device tracking for all components and materials in an electronic part to maintain high yields and rapid respond to excursions. Fortunately, the equipment and software suppliers can now offer solutions based on SEMI standards in a timely and cost-effective manner.

[4] Wafer fabs / foundries, package assembly and test, electronic manufacturing services (EMS) companies assembling PCBs, etc.