# Progress in Understanding and Prediction of Bi Electromigration in SnBi Functional Motherboard Solder Joints

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## **ABSTRACT**

The movement of bismuth atoms under the influence of electric current flow, referred to as electromigration, has been extensively studied in relation to tin-bismuth based low temperature solder joints; however, literature work most commonly uses idealized test vehicles under highly accelerated conditions of electric current and/or ambient temperature. While useful for a fundamental understanding and for comparing the electromigration performance of various solder material compositions, the resulting microstructures and failure mechanisms may not be representative of solder joints in applied applications. This paper will review an effort to describe the expected microstructures in use case settings as well as a model to predict effective Bi boundary layer conditions created during current stress. The estimates will be compared with actual accelerated samples and the impacts of the current stress plus thermal aging on solder joint mechanical performance will be documented.

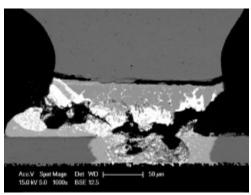
Key words: Electromigration, Current, Reliability, Low Temperature Solder, Predictive Methodology

### INTRODUCTION

The re-evaluation of tin-bismuth (SnBi) low temperature solders as replacements for tin-silver-copper (SAC) solders currently in use by the electronics industry was initially limited by concerns related to solder joint reliability. During the lead-free transition, eutectic SnBi received significant attention but was noted for having lower mechanical performance than the leading candidate material, SAC. While certain capability deltas still exist between SnBi materials and SAC, solder paste suppliers have demonstrated impressive gains in the reliability performance using material dopants such as silver, antimony, copper, and nickel [1, 2, 3]. The improvements in solder joint reliability have supported increased adoption of LTS materials. As new segments, such as higher power desktop, workstation, and server/AI are risk assessed for the use of LTS, current induced Bi electromigration (EM) has received growing attention.

Due to the larger scattering cross section of a Bi atom, the force of electric current flow can more easily drive the movement of Bi atoms compared with SAC materials at a comparable current density and temperature. Much work has been reported in the literature showing the ease with which continuous layers of Bi can be formed at the anode [4]. The associated resistance increase created by the Bi-layer can

then result in increased joule heating that further accelerates Bi accumulation leading to solder joint melting (Figure 1).



**Figure 1**. Post-current stress solder joint showing evidence of solder melting.

Unfortunately, most of the current densities and acceleration temperatures chosen for these studies are well above values likely to be encountered in actual system applications. Excessive acceleration conditions can activate alternate Bi diffusion modes not expected to be present under functional conditions. Wang, Liu and team [5] have shown the impact of current levels and temperature on Bi diffusion modes (Table 1).

**Table 1**. Changes in Bismuth diffusion mechanism with different temperature and current densities [5]

Tempera- ture (°C)	Current density (×10 <sup>4</sup> A/cm <sup>2</sup> )	$B_2 = n$	$B_1 = K/d_0^n$	Remarks
30	0.5	6.655	0.0835	Dislocation diffusion
	0.7	7.077	0.2891	Dislocation diffusion
	1.0	3.006	0.0640	Volume diffusion
50	0.5	5.263	0.09	Dislocation diffusion
	0.7	5.567	0.2	Dislocation diffusion
	1.0	1.731	0.026	Interface controlled growth
70	0.5	4.629	0.1292	Dislocation+grain boundary diffusion
	0.7	4.055	0.1050	Dislocation + grain boundary diffusion
	1.0	2.400	0.1269	Volume diffusion+interface controlled growth

While current densities above 5kA/cm2 and temperatures of 125°C have been used to study Bi EM behavior, actual notebook system sustained current densities are likely less than 1,700 A/cm2 and solder joint temperatures of less than 70°C [6] are noted in practice. Wang, Liu, and team [5] have also noted the potential for a critical current density below which Bi EM may not occur or progresses at a significantly lower rate than predicted by highly accelerated studies.

Examination of SnBi based solder joints from late life (> 2-3 years) notebook systems have shown no evidence of significant Bi accumulation and would support the existence of critical current level (Figure 2).



**Figure 2**. Functional LTS based system power FET solder joint post-2.5 years of operational life.

Previous reliability studies have shown the potential for negative impact of Bi accumulations near the pad intermetallic compound (IMC) [7]. If continuous layers of Bi near the pad interface are not likely under use condition assumptions, it would still be desirable to predict the EM behavior of Bi. This information could then be used to determine how the interface conditions created during accelerated stressing compare to those expected during late life system usage. Any associated impact on solder joint mechanical performance could then be related to lifetime solder joint conditions. The iNEMI Electromigration Work Group has published Arrhenius equations for Bi EM based on a novel planar solder joint test vehicle as well as industry standard bottom terminated components (BTC) [8]. These equations can be used to predict Bi migration under a set of current and temperature assumptions. The only challenge is the equation requires a knowledge of starting solder joint resistance and the allowable change in resistance. Under system level conditions, this level of resistance data is not typically available.

To address this challenge, this work maps Bi concentrations across a solder joint using high resolution scanning electron microscope (SEM) images and a novel image analysis methodology. The approach allows the comparison of Bi concentrations between T0 and post-stress samples.

The results of the concentration analysis were then used as a reference to assess Bi concentrations at the failure interface of mechanical drop samples. Ball grid array (BGA) packages that have been current stressed at a known current density and temperature were drop tested. The post-current stress results were then compared to as assembled (Time 0/T0) drop test results. The magnitude of the difference in mechanical capability provides a guide to how solder joints in late life systems would be expected to perform and highlight any high conditions that may require mitigation using adhesives or system level mechanical optimizations.

### **METHODOLOGY**

### **Test Vehicle Details**

The experimental work was conducted using two different BGA test vehicles. Each was populated with Sn-40Bi LTS solder balls. Package surface finish was Nickle-Palladium-Gold (NiPdAu). See Table 2 for a summary of the test vehicle attributes.

**Table 2**. Current stress test vehicle attributes.

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Test	BGA	BGA	Packa	PCB	Appli	Max.	
Vehicle	Material	Sphere	ge	SRO	ed	Current	
		Size	SRO	(um)	Curre	Density	
		(um)	(um)	, í	nt (A)	(A/cm2)	
A	Sn-	200	250	250	0.6	1,200	
	40Bi						
В	Sn-	610	500	500	2.55	1,200/6	
	40Bi					00	

### **Electrical and Thermal**

BGA packages were surface mounted FR-4 printed circuit boards using a Sn-58Bi-0.5Sb LTS paste. PCB pad surface finish was copper organic surface protectant (Cu-OSP).

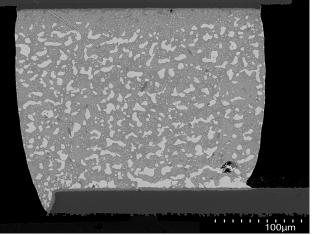
For Test Vehicle A, the daisy chain design allowed only two chains to be current stressed. Solder joints associated with other daisy chains received only thermal stress. Test boards were connected in series using a current controlled power supply. Test boards were placed in a thermal chamber at an ambient temperature of 107°C. The choice of acceleration temperature was made to duplicate other non-electromigration reliability tests to maintain a consistent baseline. No adjustment to chamber temperature was made to account for joule heating, so solder joint temperatures are expected to be several degrees higher. Test boards were left under stress conditions for 1000 hours. After stressing, sample boards were removed and cross-sectioned to compare post-stress microstructure with T0 solder joint results.

Test Vehicle B used a daisy chain design that allowed certain solder joints to receive full current exposure while other solder joints received only half of the current load. A purpose built thermal chamber was utilized to provide the thermal acceleration. Chamber temperature was maintained at 70°C.

# **Quantification Approach**

It is well known that electromigration in SnBi alloys progresses by migration of Bi in the direction of current flow. Given sufficient thermal and electrical stress, Bi will eventually accumulate on the anode side. This differs than the microstructural evolution in SAC alloys where the failure mode typically begins with void formation at the cathode side, increasing the resistance and effective current density, leading to catastrophic failure. Bi accumulation is a known risk of electromigration-induced microstructure evolution, as Bi has a higher resistivity and lower ductility compared to the bulk Sn phase. Previous studies on EM in SnBi [4] used highly accelerated test conditions, resulting in a thick and continuous Bi migration. However, this may not be representative of the conditions that a real product would

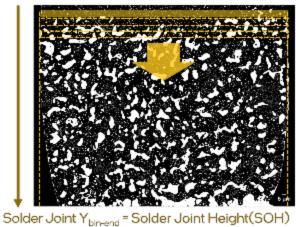
experience [6]. Under real use-conditions, we expect to observe levels of Bi accumulation that result in non-continuous layers (Figure 3).



**Figure 3.** SEM cross-section of an electrically stressed SnBi joint, showing non-continuous Bi layer

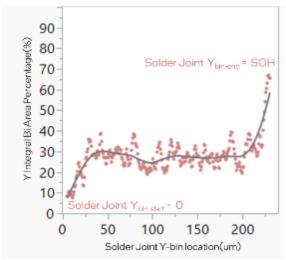
To quantify the progression of Bi accumulation in such cases, we developed a methodology based on image analysis of SEM images. First, each image was converted to a binary image to enable thresholding to separate the image into Sn, Bi, IMC, and voids. The analysis region is selected as a rectangle from the top of the board IMC to the bottom of the package IMC, with the width of the region limited by the SRO size. Finally, the analysis region is uniformly sliced into 300 equal bins. The Y axis is defined as the vertical distance from package to board. For each slice from Y=0 to the bottom of the solder joint, the bins are individually analyzed for the content of bright phase (Bi) and dark phase (Sn) while excluding voids and IMC. An example can be seen in Figure 4.

# Solder Joint $Y_{bin-start} = 0$



**Figure 4.** Schematic view of selection of analysis region, thresholding, and bin content measurement for Sn and Bi.

Once the bins have been individually measured, we then plot the Bi content as a function of vertical position on the Y axis. The resulting Y-integral plot can be seen in Figure 5.



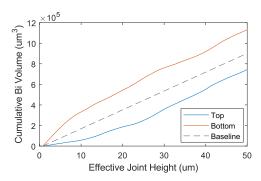
**Figure 5.** Y-integral plot of an electrically stressed SnBi joint. Each datapoint corresponds to the measured Bi area % of an individual Y-bin.

The Y-integral plot reveals the local Bi content as a function of vertical position along the solder joint. By this methodology, we can now quantify the level of Bi accumulation at the anode and Bi depletion at the cathode as a result of extended electrical stresses.

Utilizing this data to quantify a thermomechanical risk metric based on the degree of electromigration in the joint is beneficial. However, due to the inherent microstructural variation in the joint this still might not be straightforward directly from the Y-integral data. The natural microstructural variation may compete with electromigration induced variation, especially for lower levels of electromigration. Ideally, the risk metric should have the following characteristics: it is relatively insensitive to general microstructural variation noise; it is based on information over the whole joint, not just near the interfaces; it contains some physically understandable meaning; it should be effective for a wide range of material configurations and joint geometries; it should be consistent relative to its level of electromigration; and it should translate to a level of thermomechanical risk.

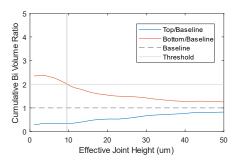
In order to fulfill these criteria, a methodology was developed to translate the Y-integral percentage plots and geometric information into cumulative Bi volume ratios vs the effective joint height. First, the effective height along the joint is calculated by finding the cumulative volume up to each Y value, assuming a circular cross section in each region of interest, and then dividing by the average cross-sectional area. This helps to reduce disproportionate influence of Y values with smaller areas due IMC or voids. Next, the cumulative Bi volume was calculated by integrating Y-integral Bi percentage multiplied by the cross-sectional area

over the effective joint height. This is calculated from both sides of the joint toward the center. The first 50 microns of this plot are shown in Figure 6. This plot also includes a baseline cumulative volume which is idealized based on a completely homogenous distribution of Bi over the effective length of the joint, as calculated by the Bi area throughout the whole image. This plot shows whether the region near each end of the joint contains more or less Bi than there would be for a uniform distribution.



**Figure 6.** Cumulative Bi volume from each end of the joint over the first 50 um of the effective length of the solder joint. Baseline assumes a completely homogenous Bi distribution.

To capture the degree of deviation from the baseline, the cumulative Bi volume for each end of the joint is divided by the baseline cumulative Bi volume over the effective length of the joint as shown in Figure 7, which effectively normalizes and denoises the original plot in Figure 6, according to the previously specified criteria.



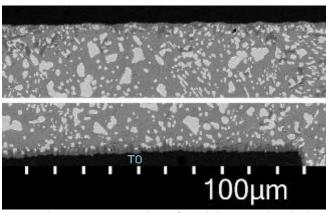
**Figure 7.** Cumulative Bi volume ratio from each end of the joint over the first 50 um of the effective length of the solder joint.

A threshold for this cumulative Bi volume ratio can be set based on experimental data for a specific level of thermomechanical or electrical risk. In the current study that threshold was set to 2 such that the effective Bi accumulation length is defined by the furthest point where there is twice as much Bi compared to an idealized average. For the case shown in Figure 7 the effective Bi accumulation based on this threshold is 9.5 microns. If the cumulative Bi volume ratio doesn't reach this threshold, the electromigration-induced risk is said to be negligible.

# RESULTS & DISCUSSION

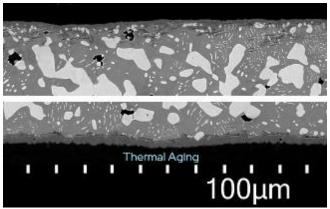
### **Microstructural Observations**

Due to the configuration of the packages, we observed solder joints that experienced only thermal stresses (no current in the joint, thermal stress due to chamber temperature) and both electrical and thermal stresses for joints that were part of the daisy chain. Additionally, we examined un-stressed joints (T0). Figure 8 shows the cross section of the T0 joint, before any electrical or thermal stresses are applied. Near the IMC on both the package and board side we observe a fine distribution of smaller Bi particles, on the order of 10um or finer. The IMC itself has an average thickness of 2um for both the package and board sides.



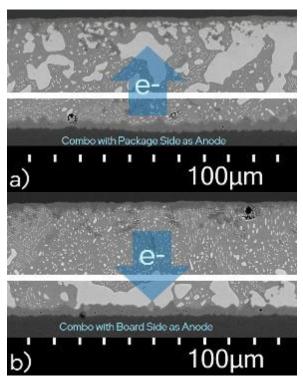
**Figure 8.** SEM cross-section of T0 joint, pre electrical or thermal stressing. Zoomed-in view provided for package side (top) and board side (bottom).

Figure 9 shows the cross section of the thermal stress only joint (no daisy chain). It can be seen that larger, coarser particles on the order of 10's of microns are observed. Additionally, we observe a slight denudation of Bi from the near-IMC region on both the board and package side. This suggests the typical coarsening behavior, with dissolution of small particles feeding the growth of larger particles. The denudation of Bi near the IMC region indicates the diffusion of Bi from near the IMCs towards larger particles in the center of the joint. Additionally, we observe a slight increase in average IMC thickness from the T0 condition.



**Figure 9.** SEM cross-section of a thermal-stress only joint, without electrical stressing. Zoomed-in view provided for package side (top) and board side (bottom).

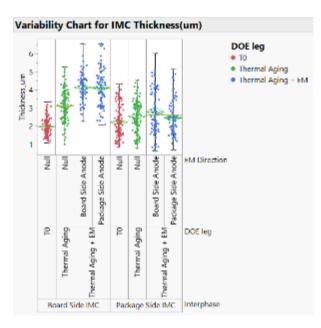
Figure 10 shows the cross section of joints exposed to both electrical and thermal stress combo. Both directions of current flow are shown, with a) package side as anode and b) board side as anode. It can be seen that large Bi particles can be observed on the anode for both directions of current flow. Additionally, we observe denudation of Bi at the cathode side, with the remaining Bi presenting as small, discontinuous particles. We also observe an increase in the IMC thickness from the T0 condition, with the board side being thicker than package side regardless of current flow direction.



**Figure 10.** SEM cross-section of a joint exposed to both electrical and thermal stressing. A) for current flow towards package anode, b) for current flow towards board anode.

Figure 11 shows the variability plot for IMC thickness for all 3 conditions, at both the board and package side. At T0 the

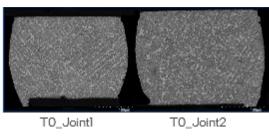
IMC thickness is fairly consistent between both board and package side. After thermal stressing and combo stressing, we observe a slight increase in IMC thickness as well as an increase in the IMC thickness variability. On the board side, we observed thicker IMC in comparison to package side. after both thermal and combo stress. We attribute this different behavior to the ENEPIG metallization at the package side, and the Cu-OSP used on the board side. Additionally, the slight increase in IMC thickness on the board side when both thermal and electrical stresses are applied can be explained by the increase in temperature due to joule heating. We also note that the IMC thickness differences are independent of current flow direction, suggesting that IMC growth is not primarily driven by Bi atom migration, but rather by the ambient thermal conditions with an additional joule heating resulting from the current stress.

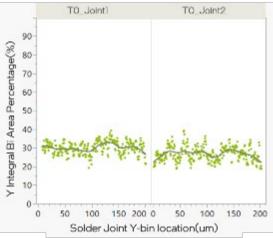


**Figure 11.** Variability plot for IMC thickness for T0, thermal aged, and combo stressed solder joints on both package and board side.

# **Quantification of Bi Migration**

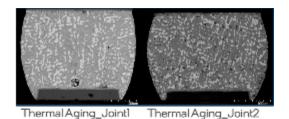
Figure 12 shows SEM images of two typical solder joints at T0 without any thermal or electrical stressing, along with the Y integral plots associated with these images. The T0 plots show significant variations in Bi content (seen as jitter about the curve fit) which are due to the complex eutectic structure. However, there is no overall trend in Bi content with respect to the location in the joint, and the overall Bi content is roughly centered around 30% Bi with a local variation of 10%.

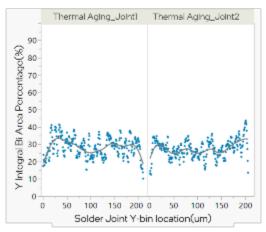




**Figure 12.** Cross sections of typical T0 solder joints with associated Y-integral plot, showing Bi content as a function of position along the vertical Y axis of the joint.

The cross sections of 2 typical solder joints with thermal stressing only are shown in Figure 13. It can be seen from the Y integral plot that the distribution of Bi has changed from the T0 condition due to the aging treatment. We observe a drop-off in Bi content near the package side and board side IMCs. This local reduction indicates diffusion flow towards the center of the joint due to coarsening effects. However, the Bi content of the center of the joint remains similar to that of the T0 structures. Additionally, we see that the variation of Bi content is higher in thermally aged joints which can also be attributed to coarsening effects.

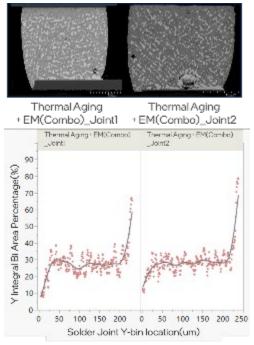




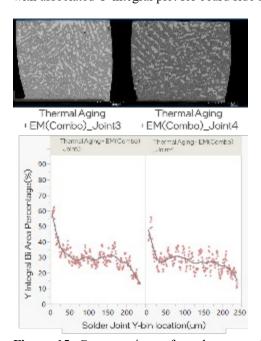
**Figure 13.** Cross sections of thermally aged solder joints with associated Y-integral plot.

Figure 14 shows the cross sections and Y-integrals for both thermally aged and electrically stressed joints with the board as the anode, with the reverse (package side anode) in Figure 15. Here we see a clear signal of Bi accumulation to the anode side. Just as in the T0 and thermal aged specimens, the center of the joint shows local variation centered around the 30% Bi content; however, we see that near the cathode the Bi content drops to near 10%. On close observation, the remaining Bi at the cathode is quite fine and disperse, with most particles having a diameter below 5um. On the other hand, at the anode side we see the Bi content rise to 60% or higher in some cases and up to 80% in the accelerated cases tested in the current work.

Based on our analysis of Bi content, we can make the following observations. During the primary stages of electromigration-induced Bi migration, the changes in Bi content are mostly confined to the local regions close to the cathode and the anode. The accumulation near the anode side depletes the Bi content of the center of the joint, which is fed from the cathode side. Overall, the Bi content in the center of the joint remains the same, however thermally induced coarsening does affect the particle size, which creates some local variability.



**Figure 14.** Cross sections of combo stressed solder joints with associated Y-integral plot for board side anode.

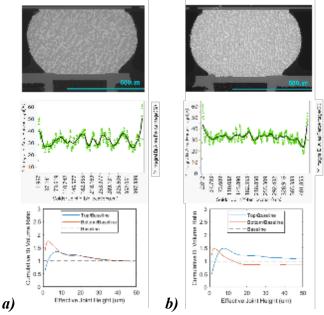


**Figure 15.** Cross sections of combo stressed solder joints with associated Y-integral plot for package side anode.

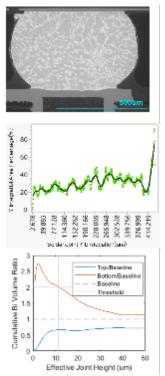
### **Metrics of Bismuth Migration Severity**

To further investigate the extent of electromigration in various conditions, the cumulative Bi volume ratio methodology was applied to an additional set of solder joints with two different current densities. All of the solder joints were kept at an ambient temperature of 70°C. Half of the joints were subjected to a current density of ~1200 A/cm² while the rest were subjected to half the current density of approximately 600 A/cm². Most of the full-current bumps exhibited some level of Bi electromigration while none of the

half-current bumps exhibited any discernible electromigration. The cumulative Bi volume ratio plots showed fairly consistent trends, and 3 unique cases are shown in Figure 16 and Figure 17 below.



**Figure 16.** Cross sectional images, Bi Percentage vs effective joint length, and cumulative Bi Volume ratio vs effective joint length for (a) a half current bump, and for (b) a full current bump showing no significant Bi electromigration.



**Figure 17.** Cross sectional images, Bi Percentage vs effective joint length, and cumulative Bi Volume ratio vs effective joint length for full current bump showing significant Bi electromigration.

There are several key takeaways from these figures. First, the cumulative Bi volume ratio risk metric reasonably capture the level of electromigration seen in the joint. The bumps in Figure 16 do not show discernable electromigration and they are below the threshold, while the bump in Figure 17 does show visible electromigration and it is above the threshold. The metric was seen to work for all of the images we analyzed. Second, as demonstrated in Figure 16(b), not every joint subjected to the same current saw the same level of electromigration. Individual geometric differences, local heating, and current paths likely affect electromigration. Finally, a consistent pattern can be seen in all of the joints (both half current and full current): there is an initial dip followed by a peak in the cumulative volume ratio. As mentioned previously we observe this drop-off in Bi content near the package side and board side IMCs. This is likely due to aging affects, which cause coarsening near the interface and IMC growth [9]. This effect seems to happen to some degree regardless of the electrical stress. To summarize, we developed a metrics to quantify severity of Bi migration to enable further quantitative analysis of parameters and impact of electromigration in SnBi solder joints. The definition of risk level depends on desire of mechanical reliability. Here, our drop test is conducted on the boards with a cumulative Bi volume ratio > 2.

### **Mechanical Impact of Current Stressing**

Twelve Test Vehicle A test boards each from the T0 and poststress populations were subjected to drop testing to quantify the change in mechanical capability resulting from the current and thermal stress. Each board began testing at 80G using a 2 ms, half-sine shock pulse. Solder joint continuity was monitored in-situ. 5 drops were completed at the initial G level. If no solder joint failures were detected, the G level was increased by 20 G and another 5 drops were completed. This process was repeated until first failures were recorded for both the current stressed solder joints (labelled NCTF) and the thermal stress only solder joints (labelled CTF). See Figure 18 for an illustration of the testing set-up.

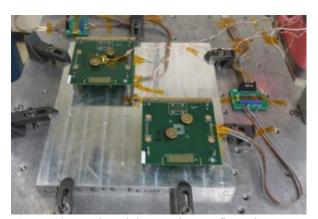


Figure 18. Test board drop testing configuration.

When compared with the pre-stress units, the solder joints receiving only thermal stress showed a 12% reduction in median stress to fail. However, the results were impacted by three boards that showed early failures that may not have

been representative. The solder joints receiving current and thermal stress showed approximately 30% reduction in median stress to fail. See Table 3 for summary details.

**Table 3**. Post-drop test results summary.

		Normalized Median Stress to Fail at 5 drops	
Structure	Stress	Pre-Stress	Post-Stress
	Condition		
CTF	Thermal	1	0.88
	Only		
NCTF	Current +	1	0.70
	Thermal		

Based on the post-stress SEM images, there was no evidence of a continuous Bi layer in any of the samples. As can be seen from the analysis presented above, there is an increase in the Bi concentration near the anode. This increased Bi concentration does appear to create additional reductions in mechanical capability when compared to the effects of thermal only stressing.

# **CONCLUSIONS**

Understanding and predicting Bi electromigration behavior in solder joints is becoming increasingly important as the use of SnBi LTS pastes are extended into higher current/higher temperature product segments. The techniques presented in this paper offer a useful tool to understand the Bi concentration changes that develop at the IMC interface with stressing under current and temperature.

By developing an understanding of the expected solder joint microstructure at solder joint end of life, post-accelerated stress results can be more accurately assessed to ensure the represent real world conditions. As well, these results demonstrate that while current stress and temperature stressing can reduce the mechanical capability of solder joints, the impact is not necessarily catastrophic under some product use conditions.

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