Potted Assembly Interfacial Reliability and Predictive Models Under Inclined 25000g Mechanical Shock

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ABSTRACT
Electronics utilized in military defense applications are increasingly reliant on commercial off-the-shelf electronics. These applications subject electronics to extreme environments, including high temperatures and high g acceleration loads during transportation, storage, or handling. Given the critical nature of these applications, it is crucial to understand the survivability, failure mechanisms, and the effectiveness of supplemental restraints such as potting materials in reducing the likelihood of failure. Currently, there is a lack of information regarding interfacial damage thresholds needed for predictive modeling and the impact of sustained high temperatures on interfacial potting failure. This study aims to measure potting material interfacial fracture toughness after exposure to high temperatures for up to 1 year, assess the effect of mode mixity using CNF and ENF measurements, and develop and validate high-g mechanical shock models. The potting/PCB interfaces have been exposed to high-temperature exposures at 100C and 150C. A circular printed circuit board assembled with fine-pitch electronic packages and multilayer ceramic chip capacitors has been potted and tested under high G shock loads. The fracture toughness parameters have been used to calculate the cohesive zone parameters at the interface. Additionally, the effect of shock orientation on failure propensity under 30-degree and 60-degree shock orientation has been examined. To predict interface and interconnect failure, a model has been developed and validated with experimental data acquired from high-speed imaging and digital image correlation for measurement of out-of-plane deformation and strains.
Keywords: High-g, Potted Assemblies, Delamination, Cohesive Zone, Non-Perpendicular Shock, High-Temperature Aging

INTRODUCTION

The durability of electronics under sustained exposure to extreme environments is necessary for aerospace and defense systems. Potting materials are often used to augment the reliability of electronic assemblies, provide supplemental restraints, and increase the damage thresholds for mechanical strength. Prior research, including [1], [2], and [3] has explored the selection of potting materials for defense and aerospace applications while [4] delves into the thermo-mechanical impact of polyurethane potting on gun-launched electronics. Despite their advantages, potting materials have certain limitations. One major failure mode in potted electronics is delamination at the interface between the potting and PCB under high g shock loads. This delamination can create a pathway for moisture or contaminants, potentially causing short circuits or chemical damage. Furthermore, interfacial cracks may extend to the solder interconnects, leading to interconnect failure. Therefore, the reliability of potting is closely linked to the properties of the potting-PCB interface.

This study focuses on the reliability of potted electronics when subjected to inclined drop angles and high g shock loads while considering isothermal aging. Most board-level tests traditionally involve a 0-degree drop angle, but real-life scenarios often feature varying drop angles. The reliability of electronics at inclined angles has not been extensively explored. The study examines the evolution of interfacial properties using PCB-potting bi-material specimens, which undergo isothermal aging for 30-360 days at 100°C and 150°C. Its primary focus is on understanding the interfacial fracture behavior and evolution of potting-PCB assemblies, with the aim of predicting and preventing failures in solder interconnects. A four-point bend loading configuration has been used to determine steady-state strain energy release rates and mode-I and mode-II stress intensity factors, key parameters for characterizing interfacial fracture toughness based on Charalambides' work [5] on bi-material interface fracture. The experimental data has been utilized to compute cohesive zone parameters for the interfacial crack. These parameters are then used to create a predictive finite element model of the bi-materials specimen. The validated cohesive zone parameters are integrated into an explicit finite element high-g shock framework to assess the reliability of potted boards. This study contributes to our comprehension of interfacial failures in potting-PCB assemblies, providing a foundation for developing strategies to reduce such failures and improve the reliability of solder interconnects in diverse applications.

EXPERIMENTAL METHODS

Sample Preparation

This study investigates the performance of four potting materials (A, B, C, D) under isothermal aging conditions,

focusing on their suitability for potted electronics exposed to high g-shock loading, as studied by earlier researchers [8], [9], [10]. Bi-material specimens of potting-PCB are fabricated using a Teflon-coated mold, as shown in Fig. 1. A 0.4 mm thick Kapton tape is used to create a pre-crack at the potting-PCB interface. This pre-crack serves two purposes: it introduces the weakest region in the sample, facilitating controlled crack propagation under loading, and it allows for steady and predictable crack growth during testing. The four potting materials under investigation exhibit varying properties, including maximum elongation, density, elastic modulus, glass transition temperature, and density. Table 1 provides a comprehensive comparison of these properties.

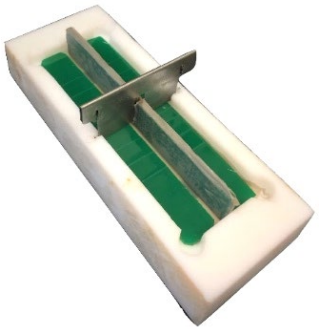


Fig. 1. Teflon Mold to dispense Potting Compound

Table 1: Potting Properties

Potting	Cure Time (hrs)	Cure Temp (ºC)	T_g (°C)	Hardness	Density (Kg/m3)	Max Elongation %	Elastic Modulus (GPa)
A	2 hours	130	120	ShoreD 85	1024	5	2.81
B	1 hour	70	60	ShoreD 72	1320	12	1.42
C	2 hours	120	~85	ShoreD 35-45	936	80	0.315
D	2 & 4 hours	165	68	ShoreD 92	2190	0.3	6.413

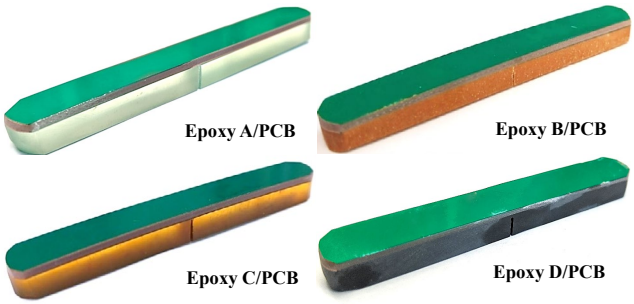


Fig. 2. Potting-PCB Interfacial Samples

The Teflon-coated mold is sprayed with a PTFE release agent; the PCB samples are carefully placed inside. A precise vertical notch, only 0.2 millimeters thick, is then created in the center of each specimen. The potting compound is dispensed into the mold and cured according to its specific curing schedule. Once fully cured, the samples are carefully removed and polished to the required dimensions of 70mm x 8mm x 6mm. Among the four potting materials studied, potting C and D exhibit the most contrasting mechanical properties, with C being the most compliant and D the stiffest. All four materials share a two-part composition consisting of resin and a curing agent. Potting C, however, further incorporates a modifier resin, contributing to its unique properties. The curing temperature for these materials has been studied in detail in previous research [11]. Fig. 2 showcases the interfacial samples prepared from potting compounds A through D.

Experimental Setup and Fracture Toughness Calculations

The PCB-potting interfaces are tested under a dynamic four-point bend loading to assess their interfacial strength. This experiment involves an Instron machine equipped with a 1 KN load cell. A span ratio of 3 was established using a load span of 20 mm and a support span of 60 mm. To ensure a steady crack growth at the interface, the testing was performed at a controlled loading rate of 2 mm/min. A schematic of the loading geometry of the bi-material specimen with a central notch and end-notch flexure specimen is shown in Fig. 3 and Fig. 4, respectively. During the experiment, the potting-PCB specimens were mounted on the dynamic four-point bend and three-point bend test setup for each of the experiments. The setup includes a Nikon camera for 2D digital image correlation (DIC) for capturing precise data. A previous study [13] compared the effectiveness of three-point and four-point bending loads on bi-material specimens, providing valuable insights into their respective strengths and limitations.

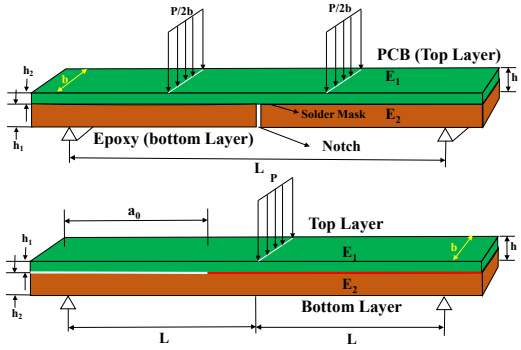


Fig. 3. Bi-Material Specimen with Notch under 4-Point Bend Loading and End Notch Flexure Specimen under Three-Point Bend Loading

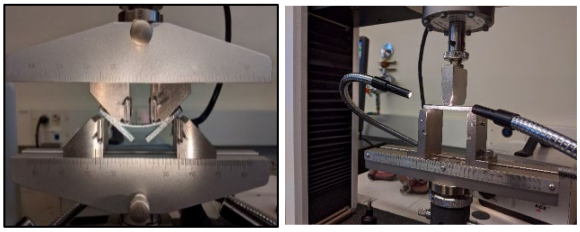


Fig. 4. Potting-PCB Dynamic 4-Point Bend and 3-Point Bend Loading

The peak critical load required to initiate crack propagation at the interface has been measured for the study of fracture toughness between the potting material and the printed circuit board. Previous research by [10] and [11] explored similar interface specimens. Charalambides [5] developed expressions for calculating interfacial fracture toughness in structural materials. The values of K_I and K_{II} can be obtained by applying the following equations [17]. The stress intensity factors for mode-I (K_I) and mode-II (K_{II}) values are determined using equations (2) and (3).

$$\zeta_{ss} = \frac{M^2\left(1-\nu_2^2\right)}{2E_2}\left(\frac{1}{I_2}-\frac{\lambda}{I_C}\right) \quad (1)$$

$$K_I = \mathrm{Re}\left(|K|e^{j\psi}\right) = |K|\cos\psi \quad (2)$$

$$K_{II} = \mathrm{Im}\left(|K|e^{j\psi}\right) = |K|\sin\psi \quad (3)$$

Terminology: ζ_{ss}= Steady state energy rate, M = Bending moment of the bi-material sample, ν_2 = Poisson's ratio of PCB, E_2 = Young's Modulus of PCB, I_2, I_C =Moment of Inertia, |K| = Modulus of Stress Intensity Factor, K_I = Mode-I Stress Intensity Factor, K_{II} = Mode-II Stress Intensity Factor

In the ENF (end-notch flexure) specimens a load deflection method has been used to determine the mode-II strain energy release rate and mode-II stress intensity factor as shown in equations (4) and (5). This methodology has been adopted based on ASTM D7905 [14]. The term a_0 represents the length of the pre-crack, P_C represents the peak critical load of crack initiation, δ_C represents the cross-head extension at peak critical load. B represents the width of the specimen, and L represents the half-span length of the specimen [15].

$$G_{II} = \frac{9a_0^2P_C\delta_C}{2B(2L^3+3a_0^3)} \quad (4)$$

$$K_{II} = \sqrt{\frac{9a_0^2P_C\delta_C E}{2B(2L^3+3a_0^3)(1-\nu^2)}} \quad (5)$$

Terminology: P=Peak load at initiation, δ_C = Displacement at crack initiation, a_0= Initial crack length, B = Specimen width, h = Specimen half thickness, L = half span length, G_C = Critical Stress Energy Release Rate, K_{II} = Mode-II SIF

High G Shock Setup

This study investigates the performance of a circular potted assembly (PCB) designed for harsh environment applications. The PCB serves as a test vehicle, incorporating nine components on its surface-mount device (SMD) side.

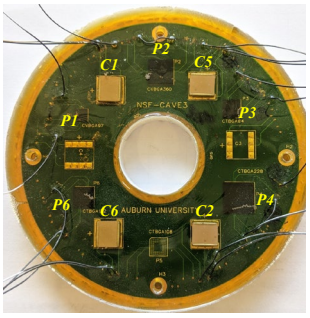


Fig. 5. Potted PCB with SMT Components

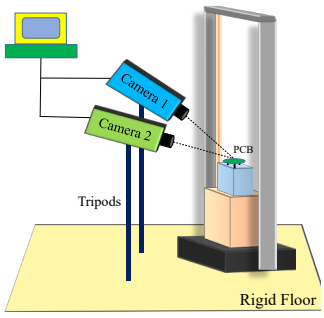


Fig. 6. 3D-DIC Setup Layout

The potted assembly with surface mount components on the printed circuit board is shown in Fig. 5. High-speed cameras are used to measure the deformation of the printed circuit assembly during the mechanical shock event (Fig. 6). In drop testing, the circular electronic assemblies are subjected to high-impact shocks to understand their real-world performance. Fig. 7 shows the 25,000g shock pulse. Fixtures for shock testing are manufactured at 30-degree, and 60-degree drop angles, as illustrated in Fig. 8. The circular PCB has been securely positioned on the fixture surface using standoffs, and the entire fixture is affixed over the DMSA table.

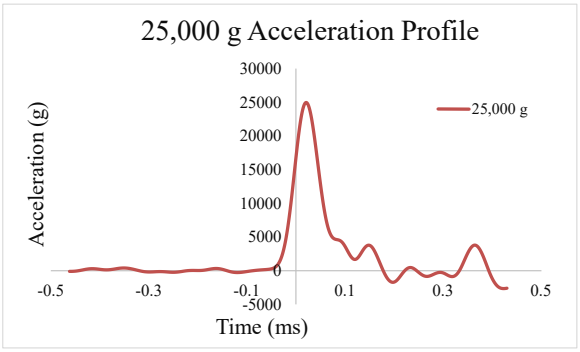


Fig. 7. Shock Pulses – 10,000G and 25,000G

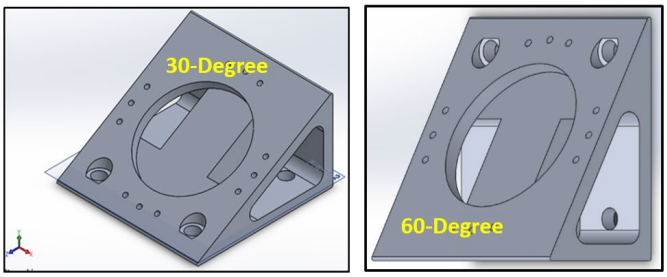


Fig. 8. Drop Fixtures – 30-degree & 60-Degree

RESULTS AND DISCUSSION

Fracture Toughness Evolution – Central Notch Specimen

This study investigates the interfacial strength of four different potting materials with a printed circuit board (PCB). The flexural load versus flexural extension data from the experiment is used to determine the peak critical load as in Fig. 9. The stress intensity factors for each material have been calculated through the measurements of the peak loads and the crack length.

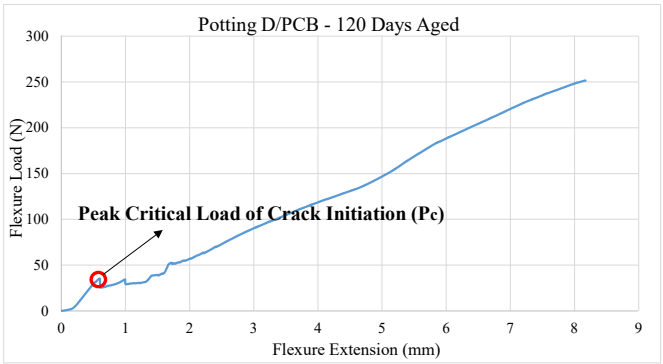


Fig. 9. Flexural Load to Extension Plot

A flexural load versus displacement plot for potting A/PCB interface has been highlighted in our earlier work [17]. We've also discussed the failure mode, the vertical notch extends into the interface, acting as the catalyst for crack initiation. The interfacial properties evolve with aging temperature and duration. Potting B exhibits delamination due to isothermal after 180 days at 100°C. Potting C has no delamination, with aging up to 180 days. However, delamination is observed at Potting C interfaces for longer

durations of thermal exposure after 180 days. This change in behavior points to the evolution of interfacial properties with isothermal exposure. Potting A and D, show regular delamination behavior of vertical notch extending into the interface followed by crack initiation and crack propagation. The evolution of failure modes has been tabulated in Table 2 Fig. 10 highlights potting B and C interfaces' evolved failure modes.

Table 2: Evolution of Potting-PCB Interface at 100°C Aging

100C	Potting A	Potting B	Potting C	Potting D
Pristine	Interface Delamination	Interface Delamination	No Delamination	Interface Delamination
30 days				
60 days				
90 days				
120 days		Delamination under Thermal Aging	Interface Delamination	
180 days				
240 days				
300 days				
360 days				

Similarly, at 150°C aging failure has been discussed in detail in [17], from which we can see the propensity of the failure modes has shifted and the rate of degradation is higher than 100°C aging. Interfacial cracks are observed at potting B-PCB interfaces after 90 days of isothermal aging without mechanical loading at 150°C in place of the prior 120 days observed at 100°C

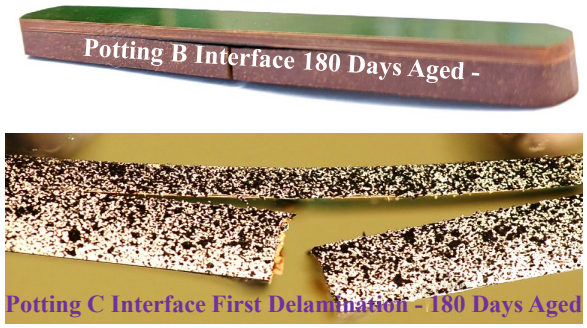


Fig. 10. Potting B and C-PCB Evolution of Failure Mode

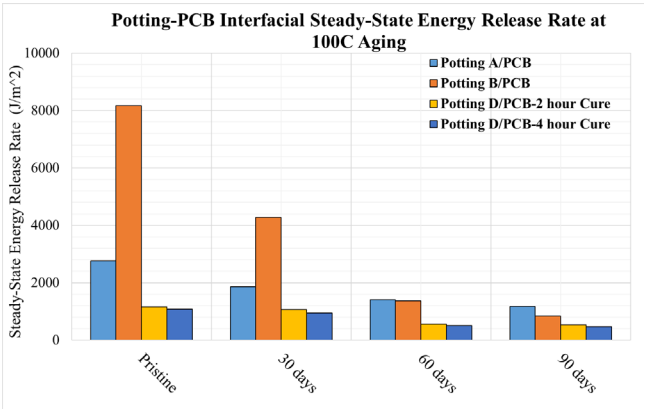


Fig. 11. Potting-PCB Interfacial Mode-I Stress Intensity Factor at 100°C

Equations (2) and (3) have been used to calculate the Mode-I and Mode-II stress intensity factors for each aging duration. This analysis allowed us to investigate how the fracture toughness of the potting-PCB interfaces changes over time. Fig. 11, Fig. 12, and Fig. 13 reveal the evolution of steady-state energy release rate, mode-I and mode-II stress intensity factors in the potting-PCB specimen at 100°C aging. These fracture toughness results have been discussed in detail for 1-year aging for both 100°C and 150°C temperatures in our earlier work [17] and [18].

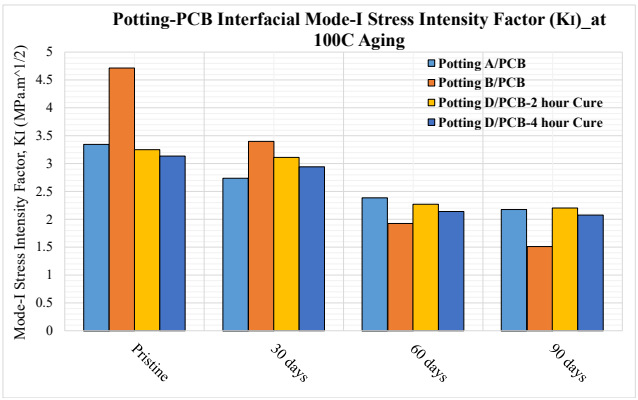


Fig. 12. Potting-PCB Interfacial Mode-I Stress Intensity Factor at 100°C

For this particular specimen and loading geometry, mode-I stress intensity factors are higher than mode-II values. The increased cure time of 2-4 hours for Potting-D shows an increase propensity for fracture with a decrease in the fracture toughness under 100°C thermal aging temperature. Potting A shows a gradual decline in its stress intensity values with each aging duration increment. Potting B has a higher mode-I stress intensity factor at pristine conditions, but with aging it has a rapid drop in stress intensity until 120 days, ultimately resulting in delamination. Potting C exhibits its strength by having no delamination for 180 days, after which it delaminated, followed by a decrease in stress intensity factors. Potting D, has a remarkably stable behavior, showcasing the most minimal decline in the stress intensity factors.

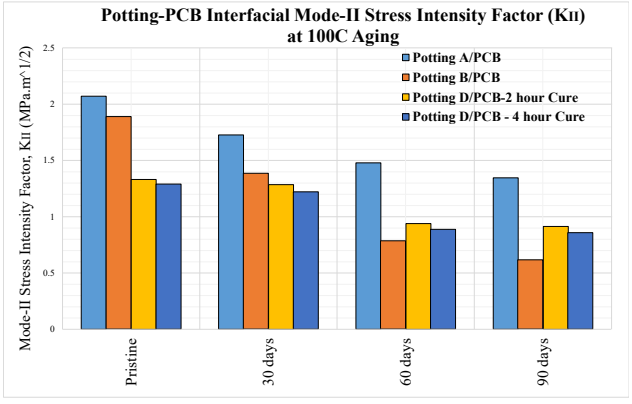


Fig. 13. Potting-PCB Interfacial Mode-II Stress Intensity Factor at 100°C

Fracture Toughness Evolution – End Notch Flexure

Equations (4) and (5) have been used to calculate the Mode-II strain energy release rate and stress intensity factors for pristine, 120 days and 180 days of aging at 100ºC. Fig. 14 shows the three-point bend loading of potting A/PCB of ENF specimens at no load, loading and crack opening conditions. Fig. 15 shows flexural load versus flexural extension plot for the ENF specimen, from which the peak critical load is determined to calculate mode-II stress intensity factors.

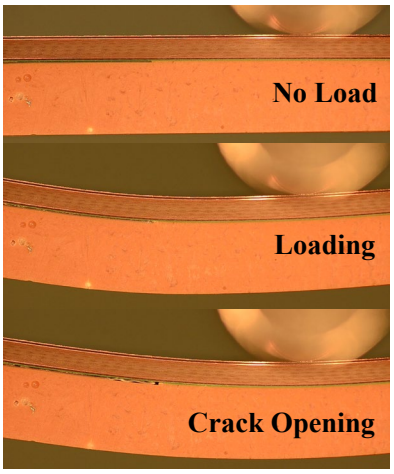


Fig. 14. Potting A-PCB Interfacial Crack Initiation and Propagation

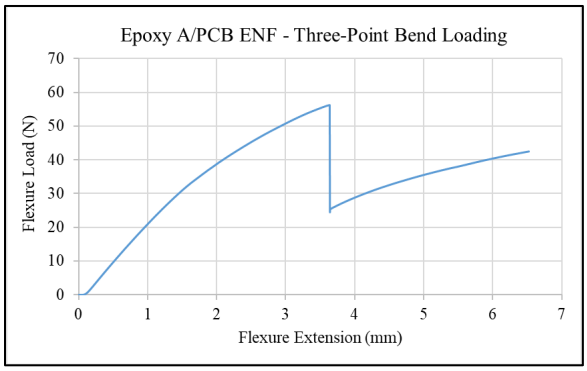


Fig. 15. ENF Flexural Load to Extension Plot – Potting A/PCB Interface

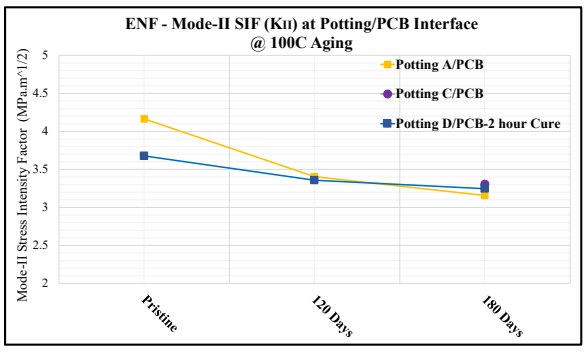


Fig. 16. Mode-II Stress Intensity for ENF Specimens at 100ºC

Fig. 16 shows the mode-II stress intensity factor values. Both potting materials A and D show a steady degradation in the fracture toughness with the increase in the time of exposure to 100°C. In contrast, potting material-C does not show fracture at the interface and thus the first reported measurement is at 180 days of thermal exposure at 100°C.

PREDICTIVE INTERFACIAL MODELING

Cohesive Zone Simulation

A similar approach to our earlier work [17] and [18] has been followed to determine cohesive zone parameters in this study. The earlier work [17] and [18], have discussed validation of cohesive properties for potting A. In this section we'll be discussing validation of potting C cohesive properties after 180 days of aging at 100ºC. This taken into account of the evolution of failure mode at potting C interfaces.

The four-point bend loading configuration is precisely modeled, applying forces at the designated locations on the specimen. Both the potting and PCB materials are assumed to behave linearly under the applied stress, simplifying the initial analysis. The four-point bend finite element model constructed in ABAQUS has been shown in Fig. 17. The model has been simulated to predict interfacial crack at the potting-PCB interface.

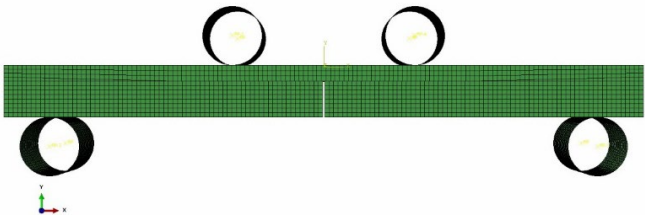


Fig. 17. Potting-C/PCB Four Point Bend Model

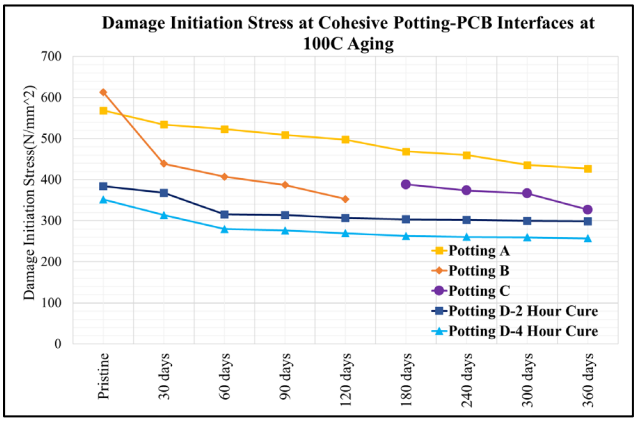


Fig. 18. Cohesive Parameters - Damage Initiation Stress at 100ºC Aging

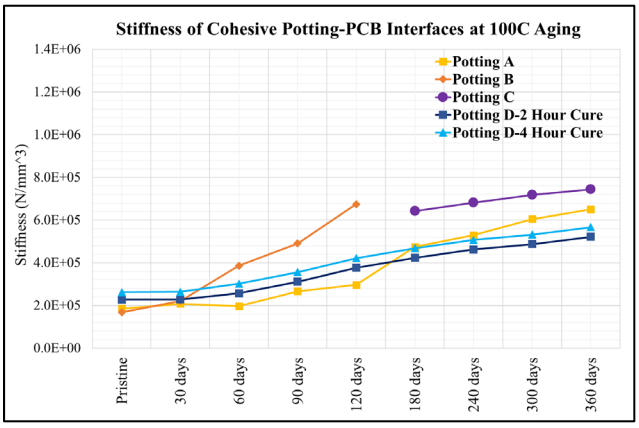


Fig. 19. Cohesive Parameters – Stiffness at 100ºC Aging

Fig. 18 and Fig. 20, shows the computed damage initiation stress of the cohesive elements at 100ºC and 150ºC aging conditions. The damage initiation stress is decreasing with increase in aging duration and temperature. Fig. 19 and Fig. 21, shows the computed stiffness of the cohesive elements at 100ºC and 150ºC aging conditions. The stiffness values are decreasing with increase in aging duration and temperature. A detailed explanation on the computation of cohesive parameters have been shown in [16] and [17]. A cohesive layer of 0.01mm thickness is inserted between the potting and PCB to simulate crack initiation and propagation. This layer incorporates specific properties derived from experimental data. The COH3D8 ABAQUS elements are specifically used for modeling cohesive behavior.

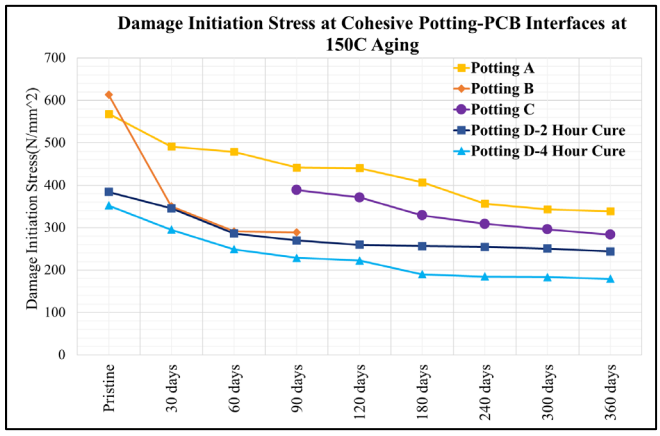


Fig. 20. Cohesive Parameters - Damage Initiation Stress at 150ºC Aging

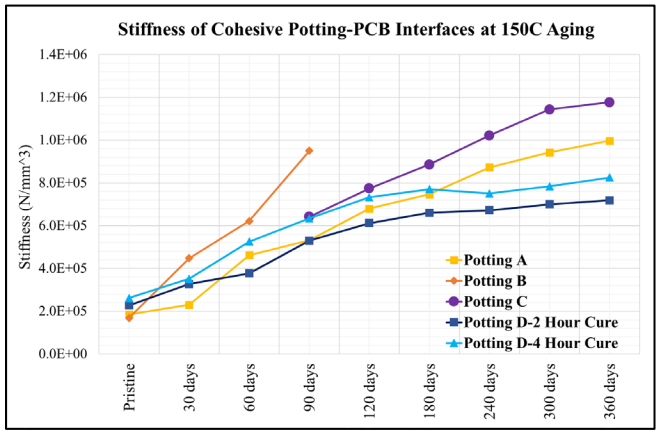


Fig. 21. Cohesive Parameters – Stiffness at 150ºC Aging

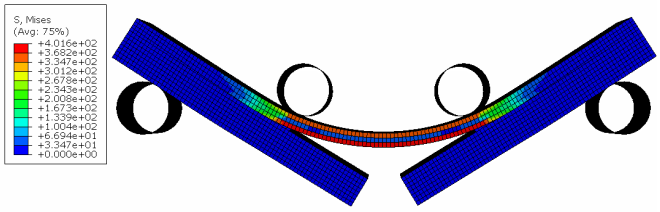


Fig. 22. Potting-PCB Interfacial Simulation of Four-Point Bend Loading

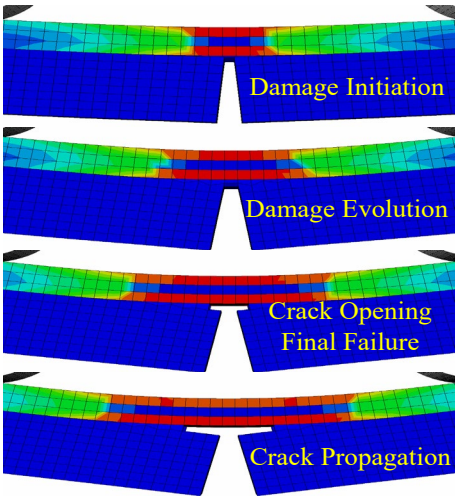


Fig. 23. Simulation of Interfacial Delamination of Potting C-PCB Interface at 180 Days of Aging

The four-point bend loading configuration is precisely modeled, applying forces at the designated locations on the specimen. Both the potting and PCB materials are assumed to behave linearly under the applied stress, simplifying the initial analysis. Fig. 22, and Fig. 23 show the evolution of the interface delamination with displacement in a 4-point bend configuration. Fig. 24 shows the correlation between the predicted and measured downward displacements. By analyzing these figures together, one can gain a deeper understanding of the potting C-PCB interface's response to aging and stress.

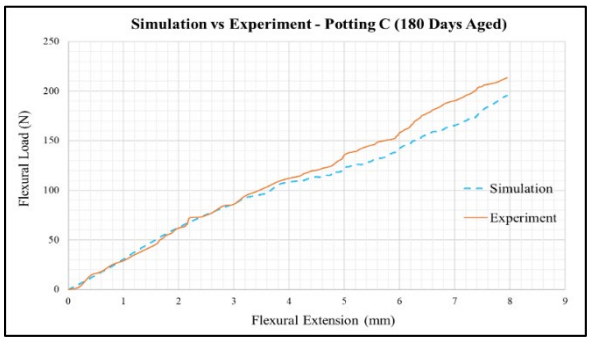


Fig. 24. Simulation vs Experimental Comparison

High-G Shock Predictive Model

The validated cohesive parameters have been used in the explicit finite element simulation to predict failures at a potted electronic assembly under high G shock.

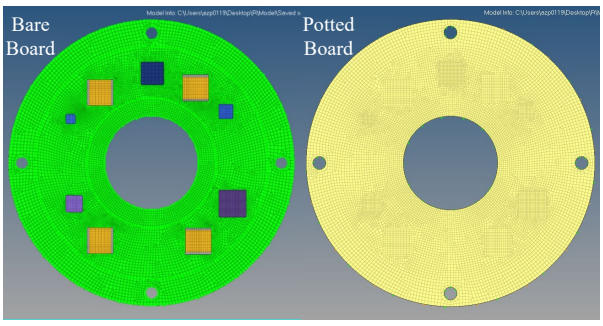


Fig. 25. Bare and Potted Board Finite Element Model

This model, constructed in hypermesh and simulated in ABAQUS as shown in Fig. 25, represents a circular PCB with nine components embedded within a potting material.

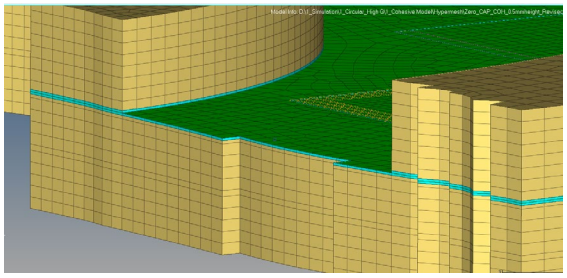
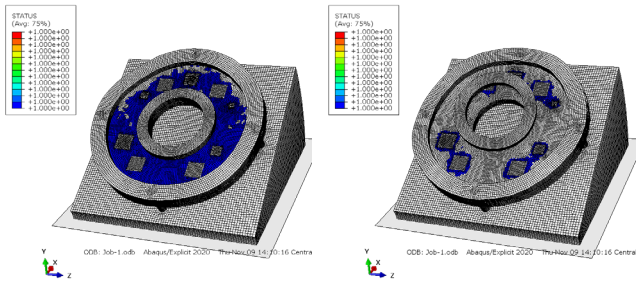


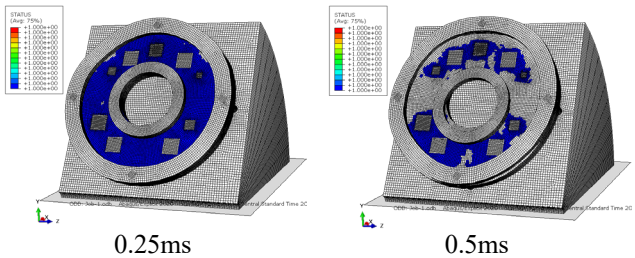
Fig. 26. Cohesive Zone Cross-Sectional View

Fig. 26 shows the cross-sectional view between the PCB and the potting, highlighting the cohesive layer. Solder interconnects between the PCB and the package are modeled with three-dimensional B31 Timoshenko beam elements, capturing both bending and shear deformation. PCB has been modeled by two-dimensional S4R reduced integration elements, offering a balance between accuracy and computational efficiency. Capacitors, drop base, fasteners, packages, and potting compound are modeled as individual components using three-dimensional C3D8R reduced ABAQUS elements, providing a detailed representation of their geometry and material properties. The floor is modeled using three-dimensional R3D4 elements. Fig. 27 to Fig. 28 illustrate the predicted cohesive element deletion at the potting C-PCB interface at various instances of time during a simulated 25,000G high-g shock event. The deleted cohesive element represents delamination at the potting-PCB interface. Notably, the figures indicate a potential for the inner disc to separate from the assembly following delamination. Validating these predictions against experimental data is crucial for ensuring the accuracy of the simulation model.



0.25ms 0.5ms

Fig. 27. Simulation at 30-degree at 0.25ms and 0.5ms – Element Deletion



0.25ms 0.5ms

Fig. 28. Simulation at 60-degree at 0.25ms and 0.5ms – Element Deletion

One can also see at 0.25 ms in 30-degree and 60-degree drop angles, the cohesive elements in upper quadrants of the board delaminates earlier than the lower quadrants of the board. This directly indicates non-uniform strain distribution at inclined drop angles as discussed, where the upper quadrant of the board experiences a higher stress than the lower quadrant. The stress distribution is more uniform at 0-degree drop angles in both simulation and experiments of a similar test vehicle, as discussed in [16].

Validation of Inclined Predictive Model - High-G Shock

This study sought to validate the delamination behavior observed by the predictive modeling by subjecting potting C/PCB assemblies to real-world conditions. Following 180 days of aging at 100°C, these assemblies were subjected to high-g shock loads at inclined drop angles of 30-degree and 60-degree. Potting C displayed the highest initial compliance and did not exhibit delamination or failure in drop tests. However, after aging for 180 days, significant changes were observed. Similar to behavior seen in interfacial specimens, delamination emerged in the aged potting C/PCB assemblies. Furthermore, electronic components on the board experienced failure. High-speed recording at 8000 frames per second captures the drop events. Full-field strains and displacements in the potted assemblies are derived using 3D-Digital Image Correlation (3D-DIC) techniques. In pristine condition, the potting C/PCB assembly tested at 25,000G do not fail without any delamination in its pristine condition which has been discussed in detail in our earlier work [9]. The pristine boards successfully endured up to 40 drops without any signs of delamination or failure at all drop angles 0-degree, 30-degree and 60-degree. However, following isothermal aging, delamination has been predicted through the simulation in potting C/PCB drop assemblies.

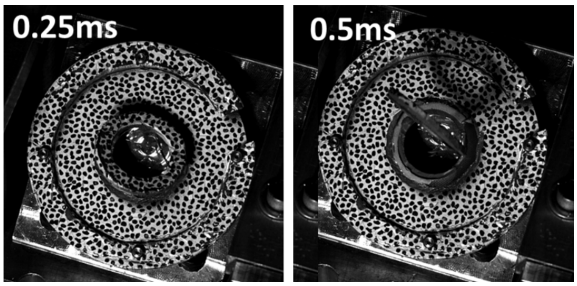


Fig. 29. 30-degree High G shock Experiment at 0.25ms and 0.5ms

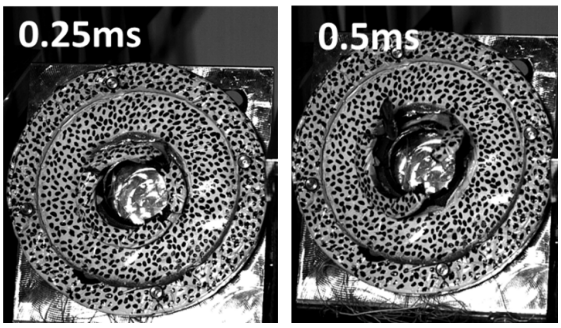


Fig. 30. 60-degree High G shock Experiment at 0.25ms and 0.5ms

Fig. 29 displays show the delamination of the inner disk of the board at a 30-degree drop angle. Similarly, Fig. 30

displays show the delamination of the inner disk of the board at a 60-degree drop angle. The high g shock experiment at 30-degree and 60-degree angles validates the finite element predictions on the delamination of the inner disk. The non-uniform strain distributions resulting in delamination and failure at the upper quadrant of the board before the lower quadrant of the board have been observed in the experiment as well. The top side of the inner disk delaminates earlier than the bottom side due to the non-uniform strain distribution.

SUMMARY AND CONCLUSIONS

This study investigates the time and temperature-dependent evolution of interfacial fracture toughness in four distinct potting compounds for printed circuit boards (PCBs). The investigation focuses on the evolution of the interfacial fracture toughness at the potting material-PCB interface over a range of aging durations at elevated temperatures at 100°C and 150°C from 30-360 days. This aging profile allows for a detailed assessment of the interfacial properties between the potting material and the PCB over extended time scales. Potting A and D showcase a gradual decline in interfacial fracture toughness over time, suggesting progressive interfacial degradation. Potting B exhibits a more pronounced decrease in these parameters, indicating a significantly faster degradation process. Delamination due to purely thermal aging was observed solely at the Potting B interface after 180 days, highlighting its vulnerability to high-temperature conditions. Potting C, characterized by its higher compliance, exhibits an ability to dissipate energy from bending loads, effectively protecting the interface from damage. This attribute makes it a potential candidate for low-temperature applications with high mechanical loading where energy absorption is crucial. However, even Potting C shows signs of interfacial delamination after prolonged aging 180 days at 100°C and 120 days at 150°C, indicating limitations in its long-term stable performance. In contrast, potting D shows the most stable behavior and minimal degradation over aging. The findings highlight the importance of considering both material properties and operating conditions when selecting a potting compound. Cohesive zone modeling (CZM) has been used to predict interfacial delamination in potting-PCB assemblies under various aging and loading conditions. By determining key cohesive parameters for each testing condition and validating them against experimental data, the model can accurately capture the onset and progression of interfacial failure. The extracted cohesive parameters are unique to each potting-PCB interface. This study further demonstrates the predictive capabilities of the validated CZM by simulating interfacial fracture in a high-g shock assembly. The inclined high-g shock experiments provided crucial validation data, confirming the model's ability to accurately capture the effects of aging and its influence on delamination behavior. Notably, the model successfully predicted the observed changes in delamination behavior for aged Potting C/PCB assemblies.

ACKNOWLEDGMENTS

The Research was conducted at Auburn University's NSF-CAVE3 Electronics Research Center under SERC ART-018, Combat Capabilities Development Command Armaments Center.

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