Panel Level Package (PLP) – Scaling up Fan-Out Packaging

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ABSTRACT
The persistent push for electronics miniaturization calls for a different approach to make packages smaller, higher performance and lower cost. Fan-out (FO) packages are well suited to serve this market trend. Via interconnects between the chip and package RDL (redistribution layers) provide higher interconnect density and lower inductance than traditional FC (flip chip) or WB (wire bond) connections. Furthermore, elimination of substrate or leadframe pieceparts simplifies the supply chain. FO packages are used in a range of end market applications including mobile, IOT (internet of things), consumer, industrial, automotive and AI (artificial intelligence).

The initial FO package manufacturing format was identical to a 200mm wafer to leverage existing WLCSP (wafer-level chip scale package) infrastructure. This FOWLP (fan-out wafer-level package) met performance requirements, but the small round manufacturing form factor proved inefficient, especially for lager package sizes. Later expansion to 300mm slightly improved efficiency and utilization. However, the large (up to 700mm) rectangular format utilized by PLP (panel level package) is a game changer.

While similar, the PLP final package is not identical to a FOWLP. Differences in materials, process, and final structure required package reliability validation. This paper summarizes reliability results for a 0.5mm pitch, 5mm PLP with one RDL layer. The package passed all component level and board level stresses for mobile and commercial applications. Margin was verified when it also passed all read points at >2x the required durations. Freestanding component package stresses were JEDEC MSL1/260°C (moisture sensitivity level 1), HAST 110°C (highly accelerated stress test), HTSL 175°C (high temp storage life). Board level reliability (BLR) included both daisy-chain and functional parts cycled from -40°C to +125°C.

Key words: Panel Package, PLP, Fan-out Package, Package Assembly, Solder-Joint Reliability

INTRODUCTION
Wafer-level (WL) and Fan-Out (FO) packages are increasingly used in a range of end market applications including mobile, IOT (internet of things), consumer, industrial, and AI (artificial intelligence). Among their advantages are: small form factor, I/O pitch 0.5mm or less, and a “chips first” assembly process which eliminates the need for leadframe or substrate inventory. The WLP (wafer-level package) assembly process forms repassivation and redistribution layers (RDL) directly on the wafer. Although straightforward, this process limits the package I/O to reside within the die area. By contrast, a FO package includes some I/O located outside the die perimeter. This is enabled by “reconstitution”: die are sawn from the wafers and placed onto a carrier at the package pitch. After molding to lock the die in place, repassivation and redistribution layers are applied.

Fan-Out (FO) packages have been available for over a decade using 200mm or 300mm “reconstituted wafers”. Known as FOWLP (Fan-Out Wafer-level Package), this was a logical first implementation for volume manufacturing as it reused existing wafer-level equipment and infrastructure. However, area utilization was suboptimized forcing rectangular packages into a round carrier. Panel Level Package (PLP) assembly follows the same general flow, but reconstitutes into a rectangular panel, typically 600mm to 700mm on a side. Thus utilization efficiency was improved (no partial packages at the perimeter) and unit manufacturing cost reduced due to the larger processing format (area over 6x larger).

However, this scale-up plus manufacturing form factor enhancement compelled changes to BOM (bill of materials), equipment and process. For example, it has proven simpler to laminate a dielectric dry film for PLP than spin coat a liquid. Also, material property and layer thickness adjustments were necessary to manage warpage [1, 2].

This paper summarizes the reliability results for the first in a series of TVs (test vehicles). The product was a commercial application PMIC (power management integrated circuit). This 5mm x 5mm BGA package was run through a battery of industry standard freestanding component and board level reliability stresses [3, 4, 5, 6, 7, 8]. Follow-on investigations are in progress for larger two RDL layer products meeting automotive reliability standards published by AEC (Automotive Electronics Council) [9].

FOPLP PROCESS FLOW

Fan-Out process flows can be divided into three broad categories. A good summary was described by Braun et al. [1]:

- Mold First – Die Face Down
- Mold First – Die Face Up
- RDL First

Among these, the Mold First – Die Face Down flow was selected, as depicted in Figure 1. Wafer repassivation was deposited before pre-assembly (back-grind, dicing). Acting to stabilize the die surface during dicing, the repassivation film helped to lower dicing defects such as topside chipping and cracking. Reconstitution die face down eliminated the need for expensive copper pillar formation on the wafer, provided a shorter direct via connection to the RDL, and facilitated full protection of the embedded chip. While the traditional FOWLP reconstitutes into a round 200mm or 300mm wafer size, this PLP flow reconstituted directly into the large panel format. The lithography and plating processes were performed in the full panel format. Prior to ball drop, the panel was cut into smaller subpanels due to tooling and alignment tolerance constraints. Lastly, individual packages were singulated for final inspection and packing.

In summary, the technical reasons for selecting the Mold First, Die Face Down flow were:

- Wafer dicing with repassivation to lower die chipping or cracking defect loss
- Fully embedded chip for 6-sided die protection
- Shortest electrical path between die and package

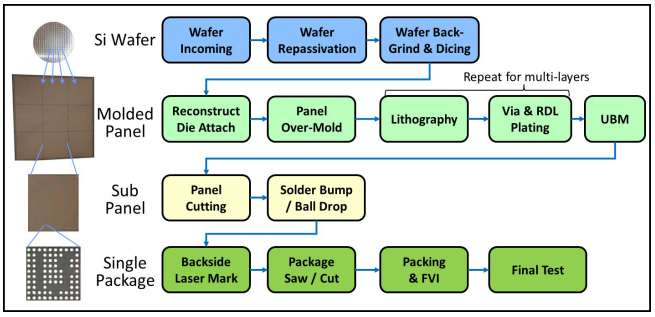


Figure 1. PLP Assembly Process Flow

TEST VEHICLE

To serve as a reliability TV, a 56 I/O 7mm x 7mm wirebonded QFN (WBQFN) was redesigned into a 78 I/O 5mm x 5mm one RDL layer PLP, hereafter referred to as PLP78.

General package characteristics of the PLP78 are summarized in Table 1, and a footprint comparison is shown in Figure 2. The PLP78 was a significant shrink versus the original WBQFN. The footprint area is ~50% smaller with ~25% lower package height for the same die. Also, 22 additional I/O were added for improved power and ground. Furthermore, package inductance was reduced by eliminating the long wirebond interconnects. The net by net comparison in Figure 3 shows the PLP package had lower inductance for all critical nets. The PLP78 was a fully functional BGA (ball grid array) version of the original WBQFN, and could be tested on production test equipment with automated handlers.

The TV cross-section is illustrated in Figure 4. The epoxy mold compound encases the Si die and repassivation layer during the panel over-mold process. The via and RDL trace are built through lithography and plating, then further encapsulated by the final repassivation to protect the layers. Finally, the solder ball attach and package singulation to conclude the assembly. With this configuration, solder ball locations can extend away from the die location to achieve the fan out characteristics.

The repassivation layer above the die is critical in developing vias and acts as a stress absorber from mechanical stresses within the package. Weak repassivation material may result to dielectric crack. Consequently, this study evaluated two repassivation materials (BOMs). While details of the materials cannot be disclosed, comparative attributes are summarized in Table 2. They were manufactured by the same supplier and have similar processing characteristics. They primarily differed in their mechanical properties. Dielectric-B had higher CTE and lower modulus, but much higher elongation to break.

Table 1. Package Characteristics

Parameter	WBQFN	PLP78
Body Size	7mm x 7mm	5mm x 5mm
I/O Count	56	78
BGA Pitch	0.4 mm	0.5 mm
Package Height	0.850 mm	0.635 mm
Die Size	3.25mm x 3.05mm	
Repassivation Material	n/a	Variable: Dielectric-A Dielectric-B
Sphere Diameter	n/a	0.330 mm
Sphere Alloy	n/a	SAC-Bi

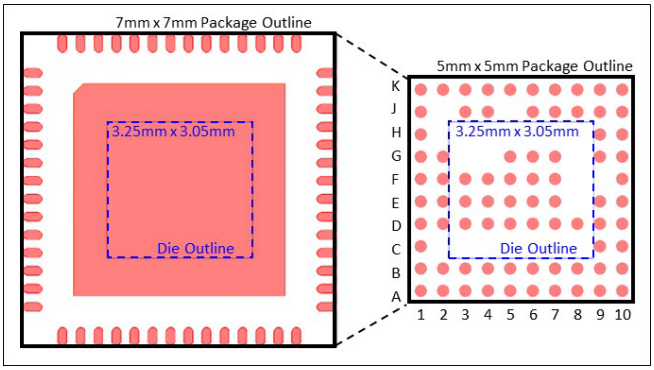


Figure 2. Package Footprint with Die Outline

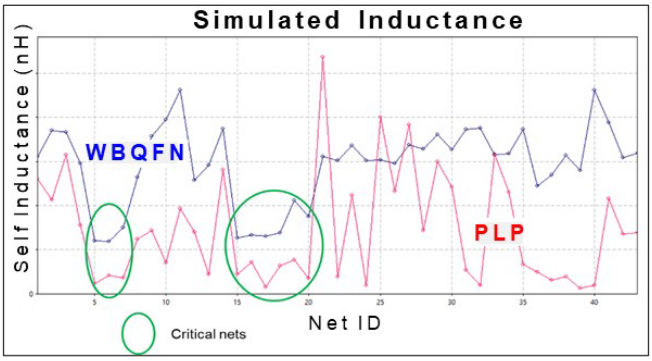


Figure 3. Self Inductance by Net: PLP vs. WBQFN Package

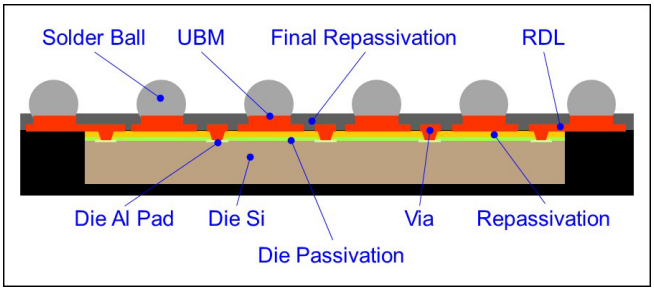


Figure 4. Package Cross-Section Schematic

Table 2. Comparison of Two Repassivation Materials

Parameter	Dielectric-A	Dielectric-B
Supplier	X	X
Form	Film	Film
CTE	Lower	Higher
Modulus	Higher	Lower
Strength	Lower	Higher
Elongation to break	Very Low	Higher

BOARD LEVEL TEST METHODOLOGY

Table 3 summarizes the two methods employed to validate board level reliability. First, designated BL-TC (board level temperature cycle) a level one daisy-chain (DC) was used to continuously monitor the solder-joint, package, and die integrity during thermal cycling. As illustrated in Figure 5, a daisy-chain net was routed through the PCB, solder-joints, RDL layer, vias, and die top metal layer. To achieve this, daisy-chain versions of the die and package were created by making small modifications to the PLP78 design, while maintaining critical features such as BGA footprint, physical dimensions, BOM, die size and thickness, and redistribution layer (RDL) metal densities.

Table 3. Board Level Reliability TV Description

	Board Level Test Vehicle Type	
Parameter	**BL-TC**	**AL-TC**
Device Type	Daisy Chain	Functional
TV Design	Modified PLP78: routing density & mechanical similarity	PLP78
PCB and SMT	Mimic the application	Mimic the application
Cycle Range	-40°C to 125°C	-40°C to 125°C
Electrical test	In Situ	Final Test
Electrical test frequency	Continuous	At read point
Target Failure Mode	Solder-joint fatigue	RDL or BEOL fracture

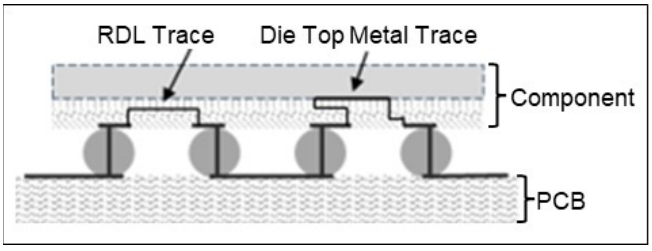


Figure 5. Daisy-Chain Schematic

The board design followed IPC specifications [8]. Solder paste was printed to boards using a no-clean, SAC305 solder paste (Table 4). Device placement onto the PCB was accomplished with automated pick and place. The fully populated PCB underwent reflow with a peak temperature at 240°C.

Table 4. PCB (TLB) and SMT Assembly Details

Parameter	Value
PCB Material	FR4 Tg >180°C CTE X-Y ~13ppm/°C
PCB Thickness	1.0 mm, 8-layer
PCB Pad Diameter	0.280mm
Stencil	Aperture = 0.340mm Thickness = 0.125mm
Paste	SAC305, No clean

After assembly, the PCBs were cycled between -40°C and 125°C in a single chamber system at one cycle per hour. Test nets were monitored in situ during cycling, with the Anatech STD256 event detector logging a failure when a net resistance exceeded 1000 ohms. The BL-TC application requirement for PLP78 was 500 cycles minimum before the first failure. However, stresses were continued beyond this required point until nearly all the units failed in order to generate Weibull plots.

During technology and package development, one must be attentive to potential new failure modes. JEDEC standard JEP150A [10] suggests that a component attached to the PCB may develop greater internal package stresses than encountered in free-standing component testing. Even though the BL-TC TV included connections through the RDL and die layers, simple direct current monitoring through the daisy-chain with a high failure threshold (1000Ω) could detect only near or hard open circuits.

Therefore, a second board level reliability method AL-TC (application level temperature cycle) was employed using functional PLP78 components. Final test of functional devices could detect parametric shifts, enabling AL-TC to be more sensitive to package RDL or die BEOL (back end of line) fractures than BL-TC. Following the methodology of Roucou et al [11], the components were mounted on an application-like translation board (TLB). The design and assembly parameters of the TLB and subsequent SMT followed Table 4. As for BL-TC, these assemblies were cycled from -40°C to 125°C, though in a dual chamber system. Because in situ monitoring was not possible, the boards were removed at fixed read points for final test.

RESULTS

BL-TC: Board Level Reliability with Daisy Chain

Daisy-chain samples from one component lot of Dielectric-A and two component lots of Dielectric-B were mounted and stressed as described in the Methodology section. Board level temperature cycle stressing continued far beyond the application requirement (500 cycles) in order to fit two parameter Weibull distributions using MLE (maximum likelihood estimate) as shown in Figure 6. As no difference was observed between the two component lots of Dielectric-B, these data were pooled for analysis in Figure 6. The first failures occurred at 3417 cycles and 3510 cycles for packages with Dielectric-A and Dielectric-B, respectively. The corresponding characteristic lifetimes (η, 63.2% failure rate) were 5462 cycles and 5679 cycles, respectively.

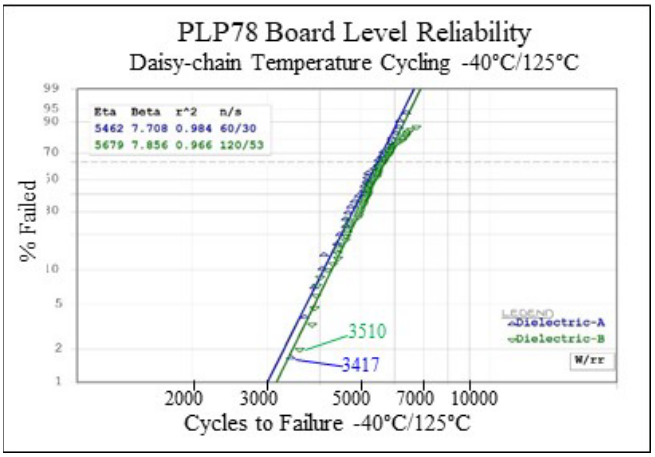


Figure 6. Board Level Temperature Cycle Weibull Plot

Cross-section analysis was performed on the first failure for both Dielectric-A (Figure 7) and Dielectric-B (Figure 8). Dielectric-A failed at solder-joint J3 near the die corner and de-populated BGA area (Figure 9). Dielectric-B also failed at solder-joint J3 near the die corner and de-populated BGA area. The empirical first solder-joint failure at J3 location corresponded to simulated solder-joint reliability (SJR) maximum energy dissipation per cycle at J3 location on the component side (Figure 10).

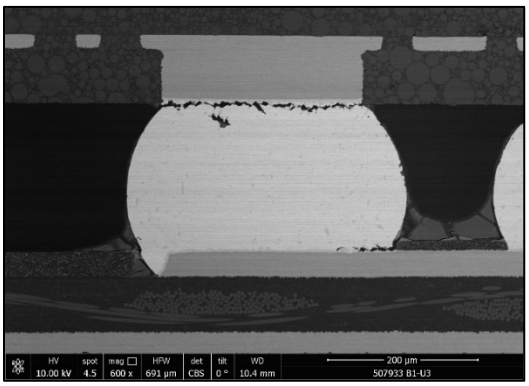


Figure 7. Dielectric-A First Failure at Solder-Joint J3

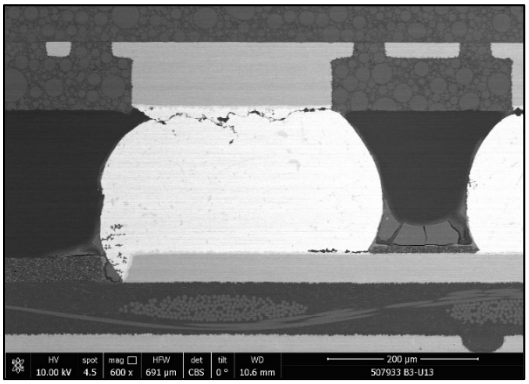


Figure 8. Dielectric-B First Failure at Solder-Joint J3

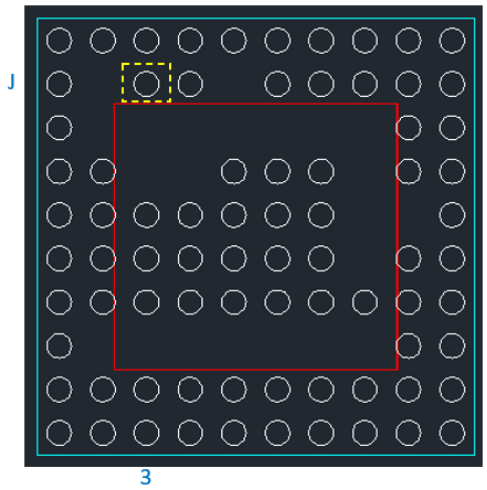


Figure 9. Ballmap Location of First Solder-Joint Failure J3 for Both Dielectric Materials

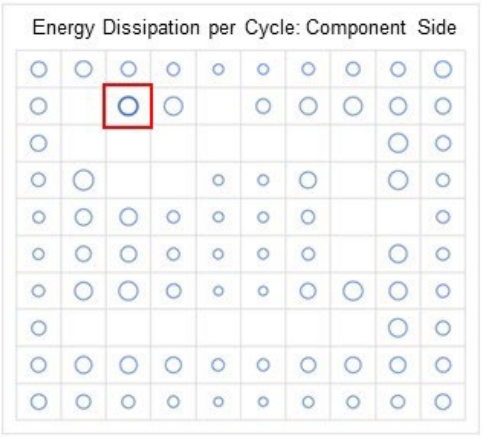


Figure 10. SJR Simulated Energy Dissipation per Cycle at Package Side Showing Maximum Energy at Location J3

AL-TC: Board Level Reliability with Functional Device

As described in the Methodology section, AL-TC testing was supplementary to BL-TC for overall technology development to assess if any package internal or die BEOL failure modes occurred. To assess process variability, samples from three separate component lots for both dielectric materials were assembled and stressed (6 lots total). As in situ monitoring was not possible, fixed read points were selected covering the range up to 3x the BL-TC application requirement. PLP78 boards were withdrawn from the test chamber for interval read points at 300, 600, 750, and 1500 cycles. Final test results are summarized in Table 5.

Post stress analysis included Confocal Scanning Acoustic Microscopy (CSAM) for delamination check and cross-section for solder-joint and/or dielectric cracking confirmation. Figure 11 compares representative die area CSAM images from each BOM, where the image for Dielectric-A showed apparent delamination in the lower left corner. Subsequent cross-section (Figure 12) confirmed delamination between the dielectric film (repassivation) and the die passivation. Cross-sections were made on random units to examine for solder-joint or package cracking. These cuts were made through the BGA rows near the die edge because both the BL-TC empirical and simulation results indicated this was the highest stress region (Figures 9 & 10). After 600 cycles of AL-TC, no cracking was observed in the solder-joints from either BOM. Representative cross-sections are shown in Figure 13.

Table 5. Application Level Temp Cycle (# Failed / # Tested).

Read point	Dielectric-A		
	Lot 1	Lot 2	Lot 3
300 cycles	0/87	0/87	0/87
600 cycles	0/79	0/77	0/77
750 cycles	0/73	-	-
1500 cycles	0/73	-	-
Read point	**Dielectric-B**		
	Lot 1	**Lot 2**	**Lot 3**
300 cycles	0/87	0/87	0/87
600 cycles	0/77	0/77	0/77
750 cycles	0/72	-	-
1500 cycles	0/72	-	-

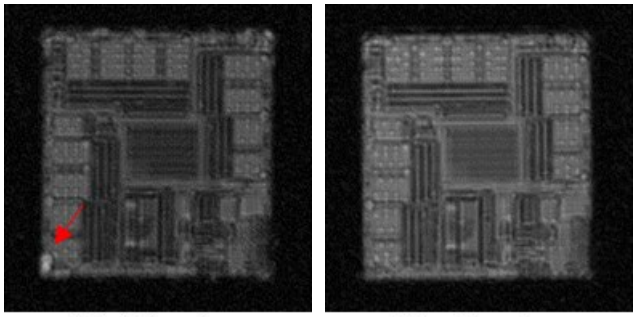


Figure 11. Representative Die Area CSAM Images After 600 Cycles AL-TC. (a) Delamination Noted in Die Corner for Dielectric-A. (b) No Delamination with Dielectric-B.

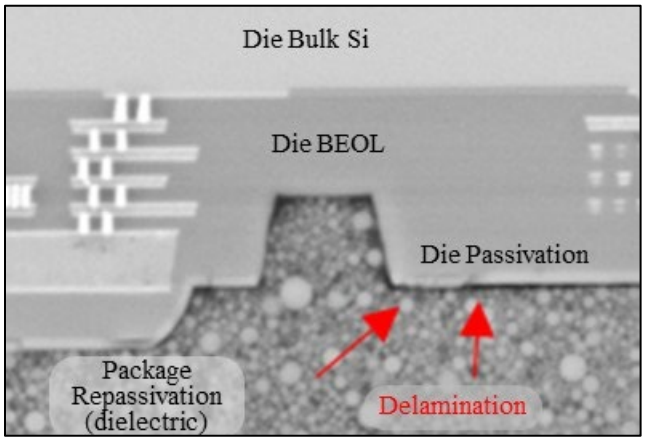
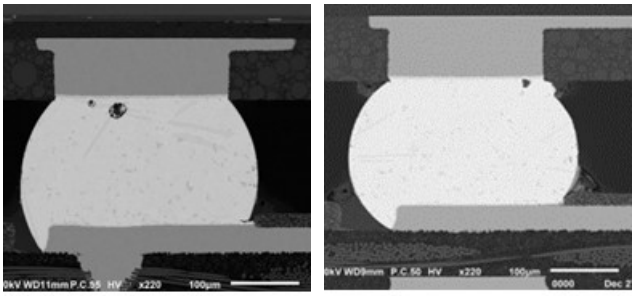


Figure 12. Dielectric-A Lot 3 cross-section to location of delamination post AL-TC 600 cycles. Delamination observed between the dielectric film (repassivation) and the die passivation.



(a) Dielectric-A (b) Dielectric-B

Figure 13. Cross-sections after AL-TC 600 cycles. No solder-joint crack observed in either dielectric material.

Component Level Testing

In addition to board level testing, freestanding component level stresses were conducted to demonstrate the overall package reliability. These tests used functional PLP78 components with final testing at specified read points. Table 6 summarizes the component stress conditions and the industry standard test method references. Included were JEDEC MSL1/260°C plus Highly Accelerated Stress Test (HAST), High Temperature Storage Life (HTSL), Electrostatic Discharge Charge Device Model (ESD-CDM), and High Temperature Operating Life (HTOL).

Table 6. Summary of Component Level Stresses

Stress	Condition	Specification
MSL	Level 1 260°C	J-STD-020 [3]
HAST	110°C	JESD22-A101/A110 [4]
HTSL	175°C	JESD22-A103 [5]
ESD-CDM	100-1250 V	JS-002-2022 [6]
HTOL	175°C Tj	JESD22-A108 [7]

HAST and HTSL stresses were performed on six component lots (three for each dielectric type). Die focused stresses ESD-CDM and HTOL were tested on only one component lot from each BOM. Results are summarized in Tables 7-10. No failures were seen during component level stresses.

Table 7. Highly Accelerated Stress Test (# Fail / # Tested)

HAST	Dielectric-A		
Read point	**Lot 1**	**Lot 2**	**Lot 3**
MSL1/260°C	0/87	0/87	0/87
264 hours	0/87	0/87	0/87
528 hours	0/87	0/87	0/87
1056 hours	-	-	-
HAST	**Dielectric-B**		
Read point	**Lot 1**	**Lot 2**	**Lot 3**
MSL1/260°C	0/87	0/87	0/87
264 hours	0/87	0/87	0/87
528 hours	0/87	0/87	0/87
1056 hours	0/87	-	-

Table 8. High Temperature Storage Life (# Fail / # Tested)

HTSL	Dielectric-A		
Read point	**Lot 1**	**Lot 2**	**Lot 3**
200 hours	0/77	0/77	0/77
400 hours	0/77	0/77	0/77
600 hours	0/77	-	-
HTSL	**Dielectric-B**		
Read point	**Lot 1**	**Lot 2**	**Lot 3**
200 hours	0/77	0/77	0/77
400 hours	0/77	0/76	0/77
600 hours	0/77	-	-

Table 9. ESD Device Model (# Fail / # Tested)

ESD-CDM	Dielectric-A
Read point	**Lot 1**
100 V	0/3
200 V	0/3
300 V	0/3
400 V	0/3
500 V	0/3
600 V	0/3
750 V	0/3
1000 V	0/3
1100 V	0/3
1250 V	0/3

Table 10. High Temp Operating Life (# Fail / # Tested)

HTOL	Dielectric-B
Read point	**Lot 1**
500 hours	0/30
1000 hours	0/30
2000 hours	0/30

DISCUSSION

High tensile and compressive stress during board level temperature cycling (BL-TC and AL-TC) pull and push the package and die along the stress direction. In addition to bulk material fracture, these stresses make the package susceptible to interfacial delamination, especially at die corners and edges [12]. Accordingly, the package materials selected must be able to withstand these stresses.

The BL-TC Weibull plot in Figure 6 showed that both PLP78 dielectric materials passed by a considerable margin: first failures at 3417 cycles for Dielectric-A and 3510 cycles for Dielectric-B versus the 500 cycles requirement. This 93 cycles (3%) difference between the two materials was not significant. Neither was the 4% difference in characteristic life (η, 63.2% failure rate).

While both Dielectric-A and Dielectric-B passed final electrical test after 1500 cycles of AL-TC, Dielectric-B was preferred because no delamination was observed (Figures 11 & 12), indicating a more robust BOM. Future applications with larger packages in auto grade applications will need this extra margin.

Dielectric-A with 70% higher modulus than Dielectric-B was more resistant to deformation, i.e. was a stiffer material. Conversely, Dielectric-B with lower modulus exhibited a rubber like/flexible character to deformation, i.e. achieving larger strain at small stress yet maintaining its elasticity. Even though lower modulus, Dielectric-B's strength to withstand yield or fracture stress was approximately 50% higher than Dielectric-A; hence the reason for Dielectric-B's elasticity. Both these characteristics translated to 140% higher elongation to break on Dielectric-B compared to Dielectric-A. In short, a flexible yet strong material like Dielectric-B was preferred as it endured high tensile and compressive stress better than Dielectric-A. This explains why Dielectric-B had no interfacial delamination and survive slightly longer characteristic life cycle than Dielectric-A. Both dielectrics' mechanical properties were still good enough to survive component level stresses.

Shear strain of a solder-joint increases as distance from the neutral point (package center) increases [13], though local effects from the die also play a role. The 1st solder-joint fractures during BL-TC were observed in the solder-joints at the die corner for both dielectrics. Comparing Figures 9 & 10 indicates this result coincided with the simulated energy dissipation per cycle bubble plot and Mandal and Chong's observation where the first solder-joint failure location is at the silicon chip corner/edges because of maximum strain energy accumulation at that region [14].

In both dielectrics, package bulk solder fracture first occurred on the package side, indicating a strong solder-joint to BGA pad when SAC-Bi was used [15]. Matahir et. al. found that at low Bi concentration, IMC formed islands of narrow plates with a matrix of Bi in solid solution of β-Sn which is necessary to have high shear strength while maintaining good ductility [16]. Package side fracture is primarily due to coefficient of thermal mismatch of composite material on the package side [17].

CONCLUSIONS

A Panel Level Package (PLP) test vehicle (TV) was designed and stressed to demonstrate reliability in mobile and commercial applications. In summary:

- A PLP78 package design was created which improved over the incumbent QFN:
  - Smaller package (5mm vs. 7mm)
  - More I/O (78 vs. 56)
  - Lower inductance by eliminating wires
  - Streamlined supply chain (no leadframe)
  - Wafer dicing with protective film
  - JEDEC moisture sensitivity (Level 1 vs. 3)
- Board level reliability passed -40°C to 125°C cycling:
  - Exceeded 3400 cycles using a PLP78 daisy-chain.
  - Application level testing with the PLP78 functional version verified that components on board were functional to 1500 cycles with no evidence of internal package fracturing.
- Component level stresses all exceeded application requirements.
- Two repassivation materials both met requirements, but the one with higher fracture stress provides more margin.
- Future work will include larger packages, two layers of RDL, and Auto grade reliability.

ACKNOWLEDGEMENT

The authors would like to thank Varun Thukral, Minh Chau, Nelson Chang, Chaoyi Wu, Dora Chang, and Kevin Weng for carrying out much of the board assembly and reliability testing, Eric Meeuwsen, Pieter Gommers, and Steven Hung for failure analysis, and lastly the continued support of management and colleagues including Mark Klatt, Dr. Veer Dhandapani and Glenn Daves.

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