Optimization of PCB SI Coupon Design that Minimizes Discontinuity through Via-In-Pad Plated Over (VIPPO) Technique

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Abstract

The importance of signal integrity is emphasized as signal speed increases, and higher frequencies are applied. The PCB manufacturer uses SI coupons that can replace the in-product circuit to measure and calculate the signal loss. In this study, we tried to minimize the discontinuous path of Delta-L coupon by using the VIPPO (Via In Pad Plated Over) technique to improve the signal integrity. We compared the VIPPO-applied design that has minimal discontinuity with the conventional Delta-L design. In order to minimize discontinuity, circuits connected to pads and via holes were removed from the outer layer, and the pads were designed directly above the via holes. First of all, we simulated the optimized design that eliminated discontinuities using Signal Integrity Software, Simbeor. Second, we measured and verified Delta-L by using Introbotix's Accu-prober program. In the future, higher measurement frequencies will further increase signal loss due to unnecessary pathways and discrete signals, therefore minimizing the effects of discontinuity will be an important issue, and using the VIPPO technique will help to improve signal integrity.

Introduction

In order to increase the speed of the signal, high frequency is applied, which emphasizes the importance of signal integrity. Many methods have been introduced to prevent noise and loss of signals such as low dielectric constant materials or low roughness surfaces. However, there are inherent components in the PCB structure that interfere with the signal quality, and how to remove them is also important. The Via-In-Pad Plated Over (VIPPO) structure has been adopted in many BGA footprint designs within the PCB. These VIPPO structures are preferred over the more traditional dogbone pad structure in order to shrink signal path lengths, reducing two parasitic effects, capacitance and inductance, for improved high-speed performance. The signal traces, which connect the BGA pads with the vias, act as inductors. Additionally, as high-speed designs typically have ground planes immediately below the outer layer, there is also a capacitive effect that is generated. With the VIPPO structure, the outer trace layer is eliminated, thereby cancelling both parasitic effects.

In the PCB manufacturing process, a coupon for measuring signal loss is inserted outside and analyzed as one way to verify the characteristics of the signal. Coupons are methods for verifying on behalf of the actual products and it is important to make them as identical as possible to the product. Developed by Intel, the Delta-L coupon measures a long, short circuit and calculates the tow differences to extract the loss. The greatest feature of Delta-L is a simplified de-embedding methodology to accurately measure stripline loss by using two test structures, long and short stripline traces, to remove unwanted effect, such as vias. The condition algorithm can eliminate the loss value variation induced by the multi-reflections between these impedance mismatches. Probe type is measurable and is applied to mass products due to its short measurement time. In this study, the effect of structure with minimized discontinuity path on signal loss using VIPPO process is analyzed using Delta-L coupon.

Methods

1. Design of Delta-L Coupon with Minimized Discontinuity

Representative methods of measuring signal loss include SMA connector type and probe type. The SMA connector is tightened at the end of the cable to minimize noise and improve accuracy, but the disadvantage is that it takes time to fasten and dismantle. On the other hand, the probe type is connected to the probe at the end of cable and connected to the PCB circuit from the probe, causing noise to the probe and difficulty in the calibration to the end of the probe, but the measurement time is short, so it is widely used for mass production by PCB manufacturers.

Litek Company's differential probe used in this study is a structure that contacts signal and ground at the same time as figure 1. The pins of probe are fixed so that the signal pad spacing of the outer layer is the same.
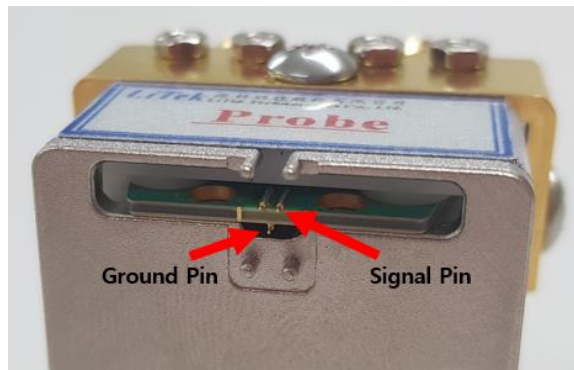
Figure 1. Litek Co. Probe Pin Structure

However, in order to match the impedance, the circuit width and spacing are different, and there is a short circuit on the outer layer connected by the outer layer pad and the via to control this. This short circuit in the outer layer causes the discontinuity of the signal, which results in the reflection and distortion of the signal. To minimize the discontinuity, Delta-L coupon was designed to eliminate the outer circuit and connect directly from via using the VIPPO technique as below.
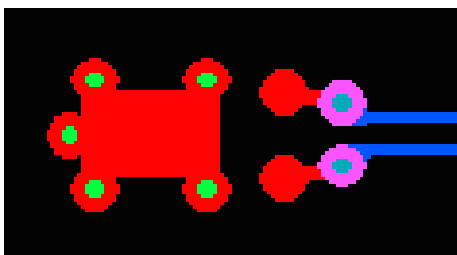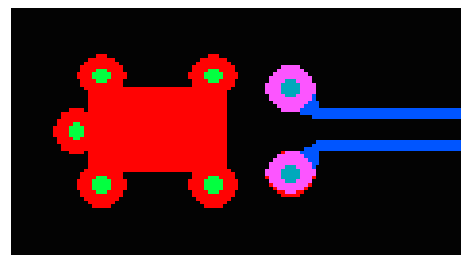

Figure 2. Conventional design of Gerber

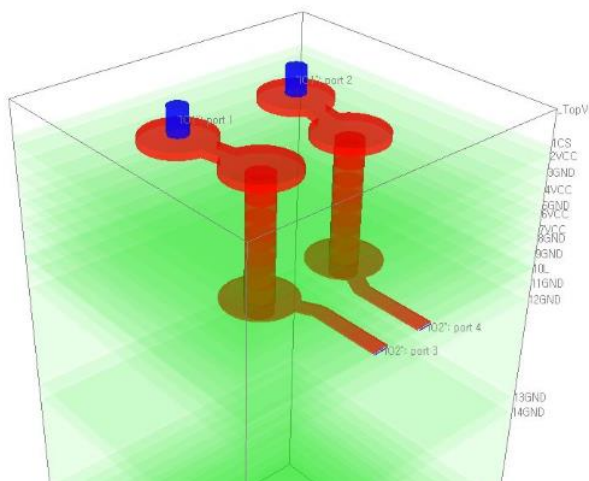Figure 3. Design with minimal discontinuities of Gerber

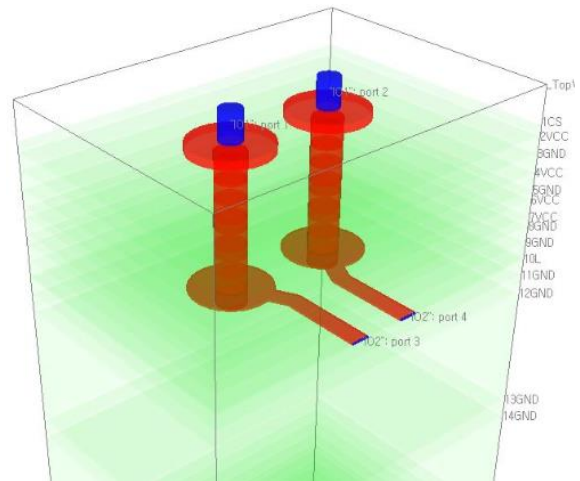Figure 4. Conventional design of 3D modeling

Figure 5. Design with minimal discontinuities of 3D modeling

2. Simulation

The simulation was performed using Simbeor, Simberian's electromagnetic analysis software. The signal layer is 10 and 23 layers, and the rest is stacked up to the ground and power layers. In order to prevent resonance and to improve signal quality, the stub is minimized, the stub of signal 10 layer is set to 11 layers, and the signal 23 layer is set to 24 layers. Material property is dielectric constant (Dk) 3.25 and dielectric loss (Df) 0.004 based on Doosan materials DS7409DV and impedance is matched 95ohms. Via hole size is 0.3mm, circuit width is 133um, anti-pad size is 0.76mm, and circuit lengths are 100.3mm and 201.9mm.

Figure 6. Via cross view of signal 10 layer of conventional design
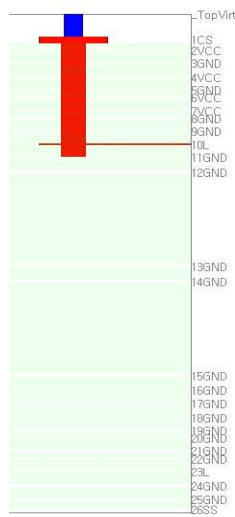
Figure 7. Via cross view of signal 10 layer with minimized discontinuity
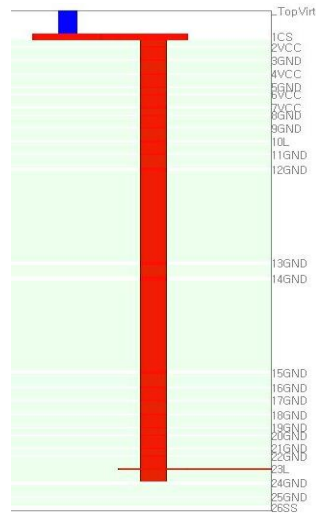
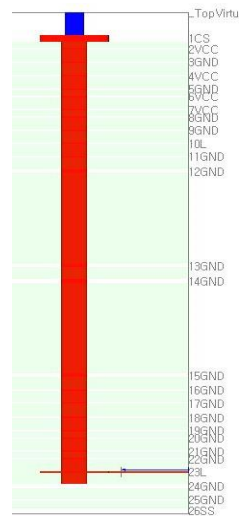Figure 8. Via cross view of signal 23 layer of conventional design

Figure 9. Via cross view of signal 10 layer with minimized discontinuity

3. Test vehicle fabrication and measurement

The product was manufactured with the same layer structure as the simulation model. Doosan DS7409DV is used for the materials. Of the total 26 layers, 10/23 layers are signal layers, and the rest are ground/power layers. The VIPPO process was applied as the MLB type to produce the following process as below.

Figure 10. VIPPO Process

The Delta-L coupons were produced in three designs. (Figure 10)

a. Conventional design coupon: It is the most basic design, and there is a circuit that connects from the outer signal pad to the via hole. (Figure 11)

b. Via hole plugging coupon: Basic design and structure are the same but via hole is plugged and cap plated. (Figure 12)

c. Coupon with minimized discontinuity path: The outer layer signal pad is formed by cap plating by VIPPO process so that the pad to which the probe contacts and the via hole coincide. This minimizes the discontinuity path of the signal by eliminating the circuit that connects the outer pad and via holes. (Figure 13)
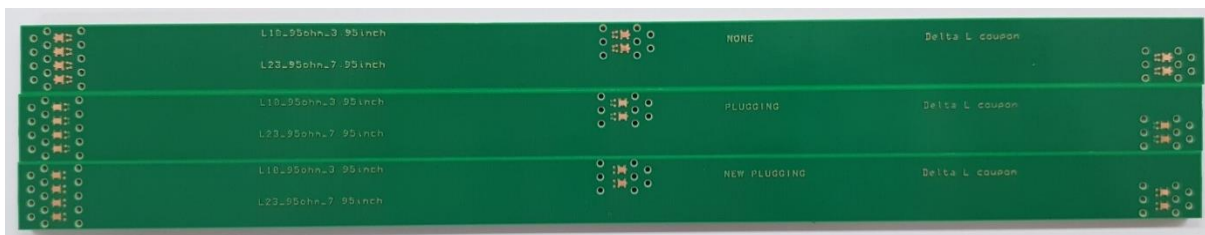

Figure 10. Test vehicle of Delta-L coupons

Figure 11. Conventional design coupon
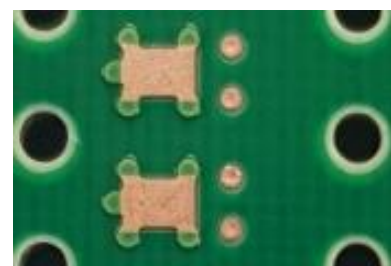
Figure 12. Via hole plugging coupon

Figure 13. Coupon with minimized discontinuity path

Signal loss was measured with Accu-prober Delta-L 3.0 version using VNA. The return and insertion loss of the frequency domain were extracted. VNA is the N5225A from Keysight Company, and probe uses Litek's diff probe. Since the measured values and waveforms may be shaken according to the pressure and movement during the measurement, the measurement was performed at a constant pressure using a weight.
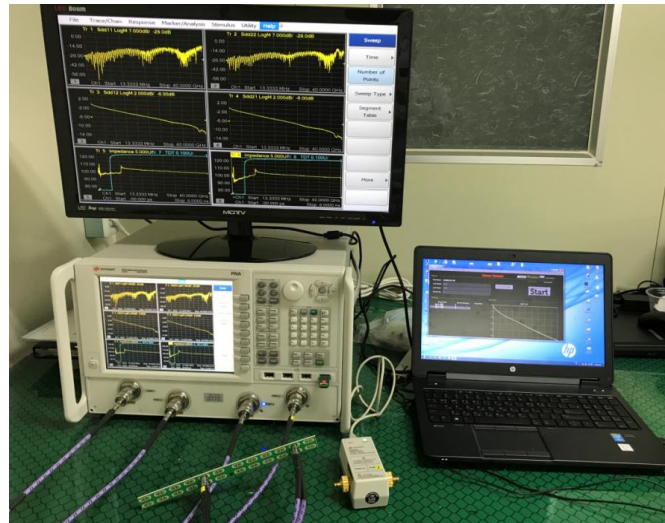

Figure 14. VNA Delta-L 3.0 measurement system

Results

1. Simulation Results

Simulation results showed that the minimized discontinuity design had less loss than the conventional design, and the difference was larger at higher frequencies. Return loss improved from 59% to 470% at 40GHz on the 10 layer, 52% at 10GHz and 297% at 30GHz on the 23 layer. Insertion loss also showed higher improvement with higher frequencies. On the 10 layer, 9% to 42% loss was reduced, and on the 23 layer, 6% to 32% were decreased. The minimized discontinuity design had a greater impact at 10 layer than 23 layer. The reason is that the 10 layer may have been further affected by the short length of via.

Table 1. Loss data extracted from simulation

Loss	Layer	Coupon design	10Ghz	20Ghz	30Ghz	40Ghz
Insertion Loss	10L	Conventional design	-4.8	-7.8	-11.3	-22.2
		Minimized discontinuity design	-4.1	-7.0	-10.0	-12.9
		Percentage of Improvement	14%	9%	11%	42%
	23L	Conventional design	-4.6	-9.9	-14.8	-20.0
		Minimized discontinuity design	-4.3	-7.5	-10.1	-15.1
		Percentage of Improvement	6%	24%	32%	24%
Return Loss	10L	Conventional design	-9.5	-8.1	-5.5	-1.7
		Minimized discontinuity design	-17.8	-13.0	-10.7	-9.5
		Percentage of Improvement	88%	59%	93%	473%
	23L	Conventional design	-10.1	-3.8	-3.0	-2.2
		Minimized discontinuity design	-15.4	-10.1	-11.8	-5.5
		Percentage of Improvement	52%	169%	297%	153%

The graph below shows that the difference is not large below 10GHz, but the gap is widening with higher frequencies. The graph of the minimized discontinuity design is closer to a straight line than the conventional design of the 23 layer showed waveforms close to resonance phenomena.
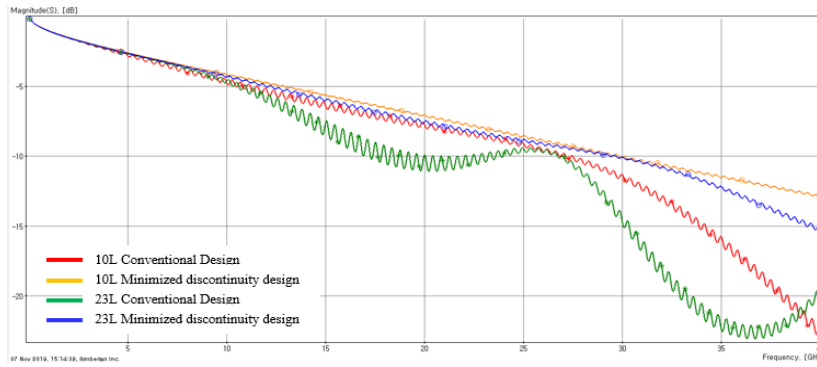
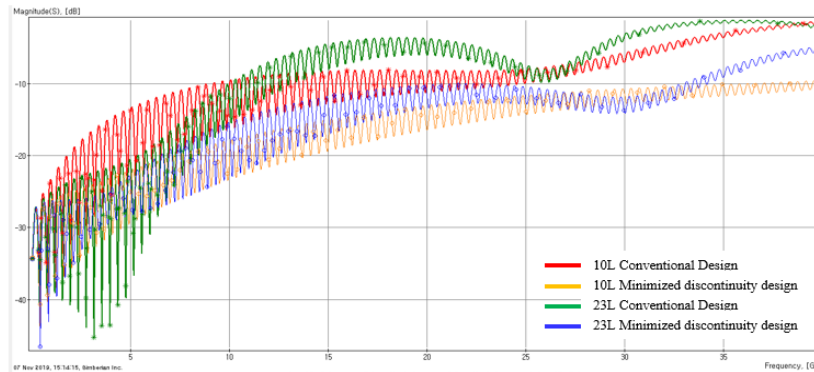Figure 15. Insertion Loss Graph of Simulation

Figure 16. Return Loss Graph of Simulation

2. VNA Delta-L 3.0 Measurement

Delta-L coupons were measured by 5 specimens, and the probe used in this study consisted of 3.6mm connector, so resonance occurred at 27.7GHz, and the measurement data was extracted with the maximum setting of 25GHz. According to the Delta-L measurement on the 10 layer, the conventional design was 0.196dB/inch lower than the minimized discontinuity design at 25GHz, and with the exception of 5GHz, the measurement loss data was lower. On the other hand, the 23 layer was measured 0.017dB/inch higher than the conventional design at 5GHz, but 0.22dB/inch lower at 25GHz as a results of the opposite from 10 layer.

An important point here is 'Uncertainty', one of the Delta-L extraction data. This value is the degree of discrepancy between the measured data and raw data calculated by the regression technique from raw data. The larger this value, the more judged that the extracted value of delta-L can be judged to be incorrect. Table 2 shows that the mean value at the frequencies other than 25GHz: conventional design 16.3%, Via plugging design 20.4%, Minimized discontinuity design 18.2% at 10 layer, and conventional design 13.8%, Via plugging design 25.1%, Minimized discontinuity design 15.4% at 23 layer.

Table 2. Delta-L 3.0 Measurement Data

Layer	Coupon Type	Loss (dB/inch)	Frequency				
			5GHz	10GHz	15GHz	20GHz	25GHz
10L	Conventional design	Insertion loss	0.438	0.653	0.813	0.941	1.046
		Uncertainty (%)	14.1	5.6	7.7	37.6	46.6
	Via plugging design	Insertion loss	0.439	0.651	0.808	0.932	1.033
		Uncertainty (%)	14.8	8.2	10.8	47.6	62.2
	Minimized discontinuity design	Insertion loss	0.417	0.668	0.879	1.069	1.242
		Uncertainty (%)	10.7	24.0	11.3	26.9	85.7
23L	Conventional design	Insertion loss	0.378	0.732	1.112	1.515	1.943
		Uncertainty (%)	6.2	20.0	23.8	5.3	210.6
	Via plugging design	Insertion loss	0.384	0.769	1.16	1.556	1.954
		Uncertainty (%)	13.1	26.4	35.6	25.2	204.1
	Minimized discontinuity design	Insertion loss	0.395	0.735	1.068	1.397	1.723
		Uncertainty (%)	11.5	16.1	16.5	17.3	161.2

The graph of measured values shows that it is easier to identify the influence of design than the table. Conventional design and via hole plugging design resulted in lower loss at high frequencies because the measurement of raw data was shaken. Since the values of large deviations are calculated, the fitted data is distorted, and the fitted graph shows the tendency to bend at high frequencies. The deviation of the fitted and raw data graphs was greatest in the via hole plugging design, and the minimized discontinuity design was the smallest.
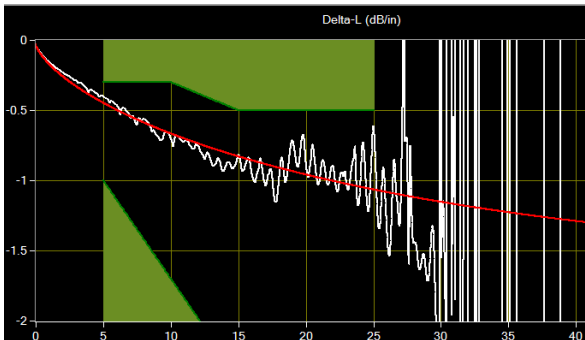
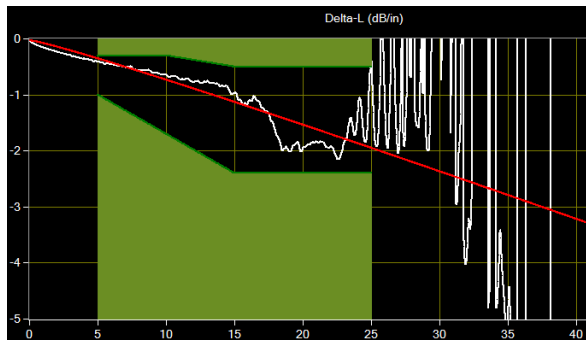Figure 17. Delta-L graph of conventional design on10 layer

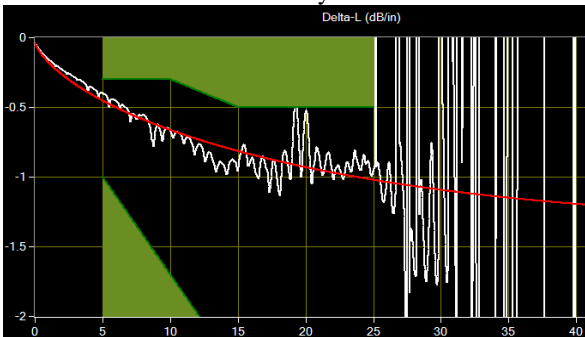Figure 18. Delta-L graph of conventional design on 23 layer

Figure 19. Delta-L graph of via hole plugging design on10 layer
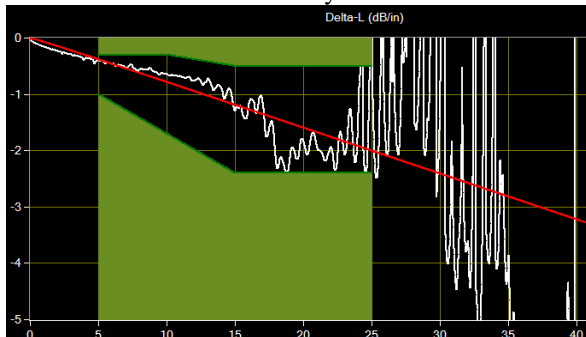

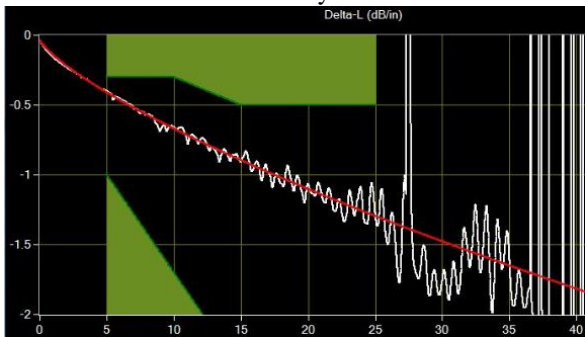Figure 20. Delta-L graph of via hole plugging design on 23 layer

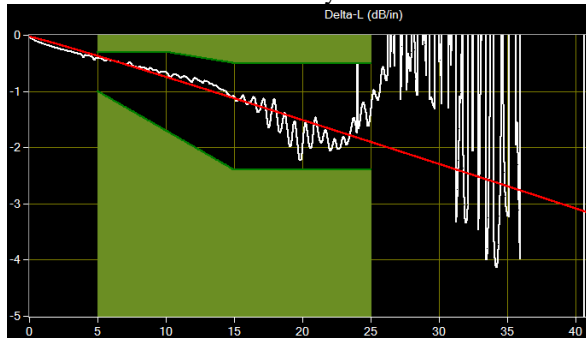Figure 21. Delta-L graph of minimized discontinuity design on 10 layer

Figure 22. Delta-L graph of minimized discontinuity design on 23 layer

For more accurate analysis, the results of extracting Loss values from raw data are shown in Table 3. The insertion loss of the 10 layer was not different, but the insertion loss of the 23 layer was the lowest with the minimized discontinuity design.

Table 3. Loss raw data from Delta-L 3.0 measurements

Loss	Layer	Coupon design	5GHz	10GHz	15GHz	20GHz	25GHz
Insertion Loss	10L	Conventional design	-4.26	-7.67	-10.94	-13.37	-17.12
		Via hole Plugging design	-4.27	-7.65	-11.22	-13.72	-17.56
		Minimized discontinuity design	-4.25	-7.53	-10.59	-13.42	-17.34
	23L	Conventional design	-4.05	-7.06	-10.94	-18.15	-18.99
		Via hole Plugging design	-4.02	-6.97	-12.11	-19.34	-19.90
		Minimized discontinuity design	-4.07	-7.03	-10.60	-16.40	-18.40
Return Loss	10L	Conventional design	-17.39	-13.42	-12.22	-19.89	-24.46
		Via hole Plugging design	-16.16	-11.41	-9.28	-14.32	-11.99
		Minimized discontinuity design	-16.01	-13.70	-13.46	-14.15	-11.72
	23L	Conventional design	-24.26	-27.11	-12.67	-13.99	-25.11
		Via hole Plugging design	-28.73	-20.27	-7.93	-9.82	-11.49
		Minimized discontinuity design	-18.17	-16.71	-21.36	-14.60	-13.04

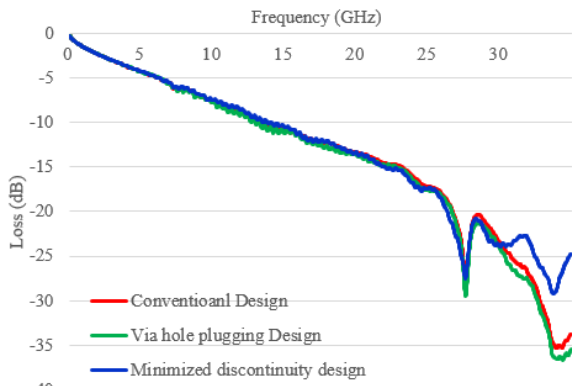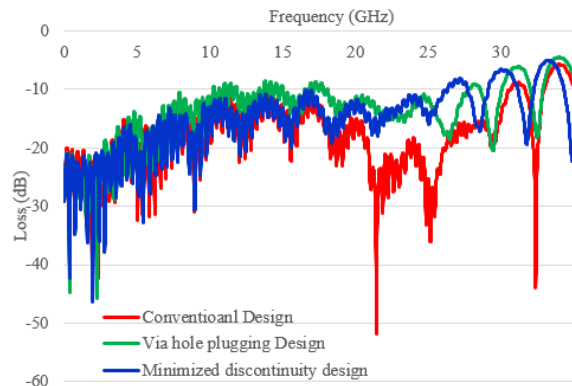Figure 17. Insertion loss of 10 layer from Delta-L

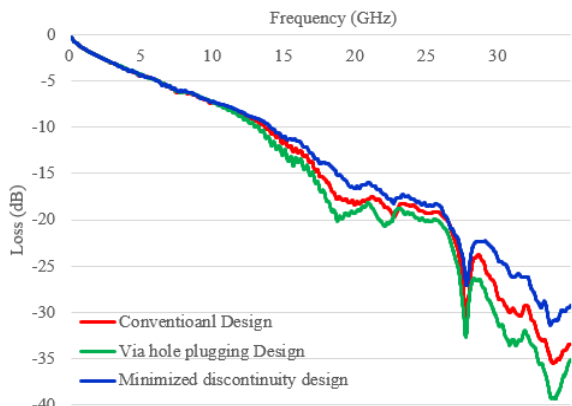Figure 18.Return loss of 10 layer from Delta-L

Figure 19. Insertion loss of 23 layer from Delta-L
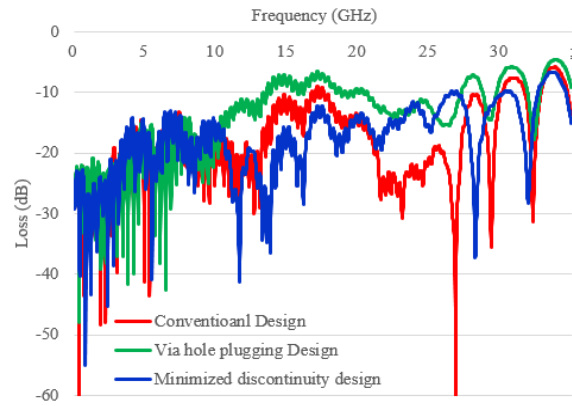

Figure 20. Return loss of 23 layer from Delta-L

Conclusion

As the speed of signals increases, the importance of signal integrity is emphasized. There are inherent components in the PCB structure that interfere with the signal quality, and how to remove them is also important.

In this study, the structure that minimized discontinuity using VIPPO method was applied to Delta-L coupon. The analysis showed that minimizing discontinuities reduced signal loss, improved accuracy in measuring SI coupons representing real products.

Small discontinuous paths also affect signal quality, and effort are needed to eliminate via and discontinuities to improve signal integrity.

Reference

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Solder Separation Failure Mode', Proceedings of SMTA International, Sep. 25-29, 2016, pp161-167

2) Jimmy Hsu, Thonas Su, et al., 'Delta-L Methodology for Efficient PCB Trace Loss Characterization', International Microsystems Packaging Assembly and Circuits Technology Conference (IMPACT), United States, 2014, pp113-116

3) Ji Zhang, Jane Lim, et al., 'PCB Via to Trace Return Loss Optimization for >25Gbps Serial Links', IEEE, 2014, pp619-624