Low Temperature Solder "Reverse Hybrid" Method to Simplify Tin-Bismuth Solder Conversions

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ABSTRACT
Several trends in the microelectronics industry are increasing the value of reducing the surface mount reflow temperatures from those currently required for tin-silver-copper (SAC) solders. Reflow temperatures more than 200 ˚C have been shown to reduce micro-via life performance, increase the risk of memory cell retention issues with high density memory components, as well as lead to solder joint quality defects such as non-wet opens and solder ball bridging caused by component warpage. A growing body of literature has been dedicated to understanding and enabling tin-bismuth (Sn-Bi) based low temperature solders (LTS). While LTS solders allow significant reductions in reflow temperatures, concerns with risks such as reduced mechanical performance and bismuth electromigration, have slowed industry adoption. This paper will review the implementation of LTS "Reverse Hybrid", also known as backward compatibility, which is the assembly of a ball grid array component with LTS solder balls to the motherboard using SAC solder paste. While the temperature reduction benefits of LTS are lost with this approach, "Reverse Hybrid" can provide SMT yield benefits comparable to full LTS processing. As well, this process can allow an interested party to assess the performance of a Sn-Bi based component without the risk of converting the full motherboard to LTS. SMT yield and solder joint reliability results will be discussed as will techniques for the control of increased solder joint voiding which is the most significant SMT process risk.

Key words: Tin-Bismuth, low temperature solder, reverse hybrid process, backward compatibility, reliability, void.

INTRODUCTION
The electronics industry benefits greatly with the widespread use of a common solder metallurgy. A standard solder material set ensures a robust supply base which maintains a favorable cost structure. Ball Grid Array (BGA) components from a diverse group of suppliers can be assembled on a single motherboard without consideration for SMT process compatibility. Validation of solder joint reliability can also benefit from an established material performance baseline and make it unnecessary to collect reliability data on every product generation. These benefits help speed time to market and improve industry efficiencies. Thus, when an industry-wide solder material change is required, it is very disruptive to system manufacturers, solder paste suppliers, and component vendors. The industry must agree on a common replacement metallurgy. Accelerated reliability testing protocols must be validated and potentially updated. New solder joint reliability failure mechanisms must be identified and characterized. As well, not all industry participants will convert to the new material set at the same time. Issues of SMT process compatibility between the old and new material sets must be addressed during the cross-over period which can last years.

The last major industry solder material transition was driven by a European Union (EU) mandate to eliminate the use of lead (Pb) in products manufactured or sold in the EU. Industry awareness of the likely restriction of Pb began in the mid- to late-1990's [1]. Research into alternate materials options was undertaken both by individual manufacturers as well as Industry-wide consortia [2]. For more than a decade, the industry worked to identify an appropriate replacement for eutectic Pb-Sn and collect the necessary data to support the transition. Tin-Silver-Cu (SAC) based solders were the agreed replacement and have been in widespread use since the late-2000's. One of the most dramatic changes to the surface mount technology (SMT) and component ecosystem was the increase in solder melting temperature. Eutectic Pb-Sn has a melting point of 183 ˚C while the now industry standard SAC305 solders melt at approximately 217 ˚C. The 30˚C+ increase in melting temperature has created challenges for component body materials, printed circuit board materials, and component reflow temperature warpage.
Recent trends in the electronics industry are making it more difficult to maintain the required SAC temperature reflow process. Very thin, fine pitch BGA packages have significantly less ability to use solder paste overprint to compensate for reflow warpage. BGA products designed for the server and artificial intelligence (AI) markets are growing so large that a SAC temperature SMT solution space may no longer exist. In both cases, the packaging trends lead to increased risk of solder joint yields not meeting requirements. Growing use of high-density interconnect (HDI) PCBs that utilize micro-vias are susceptible to reduced via life at SAC

temperatures [3]. Looking toward ever faster memory speeds, memory cell retention at SAC reflow temperatures is increasingly problematic [4,5]. While incentives exist to find a lower melting point alternative to SAC solders, without a government or other broad mandate for change, arriving at an industry consensus is daunting.

The most widely studied low temperature solder (LTS) alternative is the Tin-Bismuth (Sn-Bi) system with a eutectic melting point of 138 ˚C. The Sn-Bi system was extensively studied during the lead-free transition but was set aside in a favor of SAC primarily due to the risk of a very low melting point ternary (96 ˚C) when Sn-Bi is contaminated with Pb [6]. Interest in Sn-Bi LTS has been renewed in the last 10 years and much new research has been published [7, 8]. While the growing body of knowledge is helpful, industry reluctance to full motherboard LTS paste conversion persists. Much of the concern is related to the SMT complexity and associated potential for variable reliability performance of SAC balled BGA packages assembled with LTS solder paste (SAC-LTS or "traditional" hybrid solder joint construction) [9,10,11]. For a component supplier looking to exp oit the warpage benefits of Sn-Bi BGA balls, requiring customers to commit to full motherboard LTS use can create an insurmountable barrier to product adoption.

To address this "chicken and egg" conundrum, this paper explores the requirements for implementing an LTS "Reverse Hybrid" process. For Reverse Hybrid, the LTS BGA component is assembled to the motherboard using industry standard SAC solder paste. A similar challenge existed during the lead-free transition period and this scenario was termed "Backward Compatibility" where the higher melting point BGA material was assembled with PbSn paste. Results during that period demonstrated that with some additional care in SMT process development, high quality solder joints could be created that were capable of meeting or exceeding SAC reliability performance [12]. Some issues with increased post-SMT solder voiding were reported [12]. Overall, the ability to use backward compatibility as a bridge while full lead-free compliance was achieved did a great deal to reduce the adoption barriers. To understand if Reverse Hybrid is a feasible SMT process option for Sn-Bi-based solders, studies were completed on SMT process yield (with a particular focus on voiding), temperature cycle capability, and drop/shock capability. Guidance was also collected on SMT process optimization, and all results are compared with a full LTS solder joint baseline.

REVERSE HYBRID FUNDAMENTALS

The most obvious question regarding the feasibility of Reverse Hybrid processing is, if high temperature warpage is a driver for LTS BGA balls, how can processing at SAC temperatures be possible? In this case, the process uses the hierarchy of melting temperatures to provide a similar level of warpage benefit to a full LTS process. As the reflow temperature increases and reaches the melting temperature of the LTS BGA balls, the package collapses and the molten LTS solder contacts the still solid SAC solder paste on the motherboard. The molten LTS paste begins forming a traditional SAC-LTS hybrid solder joint. As the reflow temperature increases to the SAC melting temperature and package warpage increases, these hybrid solder joints stretch to accommodate the warpage without separating and causing open solder joints. Once at SAC peak reflow, the solder joints are fully homogenized and form high quality joints as the package cools back to room temperature. See Figure 1 for a graphic illustration of the Reverse Hybrid process.

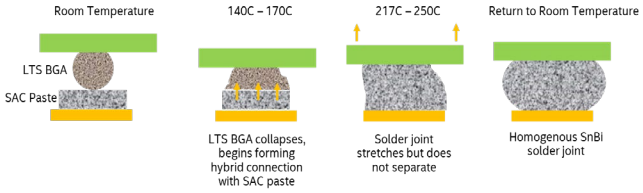


Figure 1. Schematic illustration of Reverse Hybrid solder joint formation

Reverse Hybrid SMT process development also does not require that solder paste to solder ball volume (P:B volume ratio) [13] be controlled as a critical factor as is the case for hybrid SAC-LTS solder joints. Instead stencil design can be optimized for package requirements like what is practiced currently with SAC SMT processes. Due to there being no Bi in the SAC motherboard paste, the resulting Reverse Hybrid solder joints will have a lower final Bi composition compared to full LTS solder joints (Table 1). As assembled solder joint appearance will be similar for Reverse Hybrid and Full LTS solder joints. At a microstructure level, the Reverse Hybrid joints will have a slightly finer microstructure. IMC thickness will be higher for the Reverse Hybrid solder joints as a result of the higher reflow peak temperature.

Table 1. Solder joint final Bi % vs. BGA Bi % and motherboard solder paste Bi %

Process	BGA Bi %	Motherboard Paste Bi %	Solder Joint Bi %
Full LTS	40	58	43
		37	39
Reverse Hybrid		0	34

The primary difference between the Reverse Hybrid solder joints and either Full LTS or Full SAC is the level of post-SMT solder joint voids. The molten LTS paste makes it more difficult for the SAC flux by-products to escape the solder joint. As a result, the baseline void quantity and area may be increased. However, it will be shown that the solder joint voiding results can be controlled to well below the < 30% IPC-A-610 acceptance criteria. Additionally, the overall void results will be shown to be relatively insensitive to the

choice of SAC solder paste and paste mesh size (Type 4 vs. Type 5).

Reverse Hybrid solder joints may also have an increased sensitivity to the Non-Wet Open (NWO) defect. High risk results if package warpage increases significantly during the portion of the reflow ramp where the molten LTS ball has formed a hybrid joint with the un-melted SAC paste, but the SAC paste has not established a metallurgical connection with the PCB pad. In this scenario, the SAC paste can be pulled off the PCB pad and may not re-connect on cool down, thus resulting in a NWO. This risk can be effectively assessed during SMT process development using dye and pull (DnP). Increased paste volume and/or a longer soak before ramp to peak during the profile can both mitigate this defect.

With any off-eutectic soldering process, hot tear defects may also be a risk with Reverse Hybrid. The lower Bi composition results in a larger pasty range compared to a full eutectic LTS solder joint. If the package sees a large change in shape during the period when the temperature is in the pasty range, the solder joint can be separated from either the package or PCB pad. If there is not enough liquid fraction of solder remaining in the joint, the tearing can not be repaired and a defect results. Increasing paste volume is the most effective mitigation for hot tear while reduced reflow peak temperature can also be beneficial [14,15].

REVERSE HYBRID SMT PROCESS CHALLENGES

Since the reverse hybrid process consists of merging LTS balls with SAC paste solder, voiding is unavoidable. This phenomenon occurs due to mixing of the flux in the SAC solder paste into the LTS package balls that melts at a low temperature. Figure 2 illustrates the formation of voids in the reverse hybrid process were the molten LTS traps, the SAC paste, and activators which are outgassing and forming voids. The large voids are increasing the solder joint size and causing shorts in the compressed area of the package at reflow temperature. Figure 2A shows the LTS balls placed on the SAC paste that was printed at the reflow oven entrance. Figure 2B showed the LTS ball melting ~140 ˚C and the flux and activators from the paste entering the molten ball. At the peak temperature ~240 ˚C the SAC and the LTS balls coalesce the trapped flux, expending the joint size creating a large void which could exceed the IPC 7095 [16] guideline of 30% or create a bridge to the adjustment joint Figure 2C.

Figure 3 shows large voids with oversize joints which can lead to a short during reflow. Figure 4 shows package center area with bridging on an unoptimized SMT process.

The SMT engineer's challenge is to reduce the voiding to eliminate bridging at risk areas and eliminate large voids exceeding the 30%.

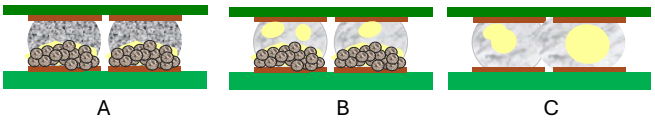


Figure 2. Illustration of process void development during Reverse Hybrid solder joint formation

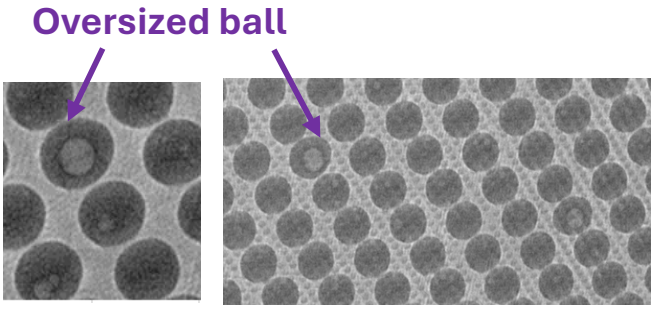


Figure 3. Image of very large solder joint void formed during Reverse Hybrid surface mount process

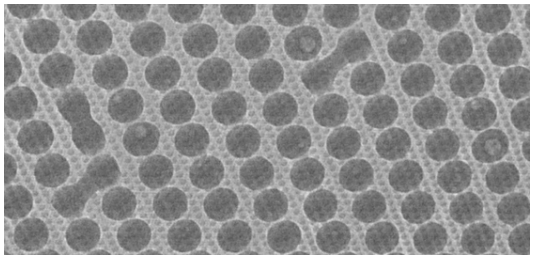


Figure 4. Package center solder bridging resulting from unoptimized Reverse Hybrid SMT process

Figure 5 is showing a large void of 44.3% which exceeds the IPC-A-610 guideline of 30%.

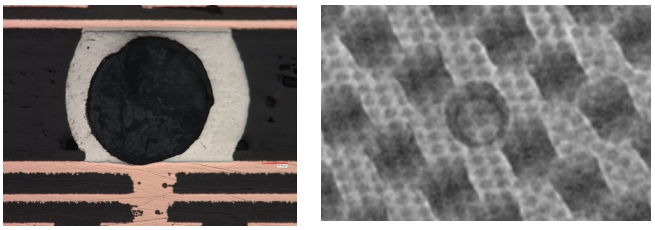


Figure 5. Example of very large solder void exceeding the 30% acceptance criteria

Solder Volume Optimization

Volume of paste was the first area to address since less volume of paste will reduce the amount of flux trapped in the LTS ball. Special reduction of paste was made in the center area where there is less impact of the warpage on the joint.

Figure 6 is showing the percentage voiding comparison between 4 mils thick stencil with full LTS (paste and ball are LTS) to reverse hybrid process (SAC Paste and ball LTS) using both a 3 and 4 mils thick stencil.

Figure 6. Impact of solder volume (modulated by stencil thickness) on Reverse Hybrid solder voids

The data indicates that full LTS SMT has much fewer voids than reverse hybrid as expected since paste and solder ball are melting at the same time. It also shows that reducing the amount of solder paste reduces the number of voids and their size.

Solder Paste Optimization

An experiment was conducted to evaluate different SAC paste suppliers with the same stencil (same paste volume) and study the impact on void size during the reverse hybrid process. The results are shown in Figure 7. Different SAC paste suppliers showed different levels of void occurrence and size. There was one Type 5 paste (Leg 6) while all others were Type 4. Type 5 paste had the most voids while Leg 2 paste had the least.

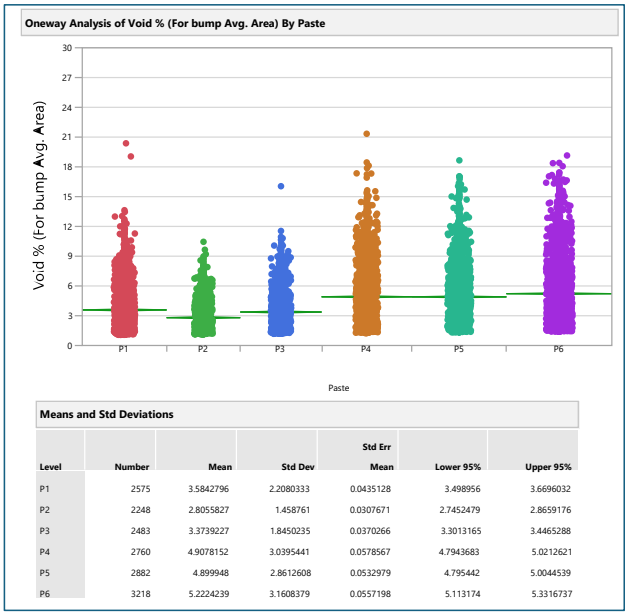


Figure 7. Solder void percent vs. SAC solder paste supplier and mesh size at the same solder volume

Reflow Profile Void Characterization

A study on the reflow parameters' impact on voids was conducted. Reflow was done in a heating stage under X-ray to study the temperature where voids are forming. Figure 8 shows that no voiding forms between 29-110 ˚C. A halo is observed around the pads at ~145 ℃ when the LTS balls begin to melt (Figure 8B).

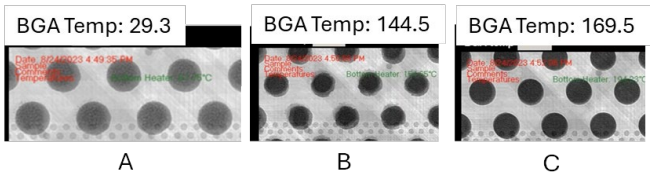


Figure 8. Solder void development between room temperature and approximately 170 ˚C

Figure 9 shows that voids start to form ~190 ˚C (A) and are more dominate in the 220 – 230 ˚C (B) and (C).

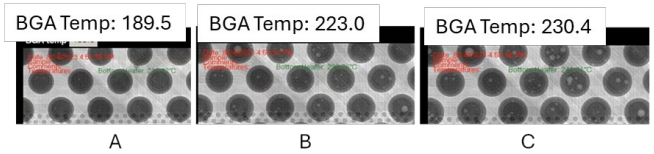


Figure 9. Solder void development between 190 ˚C and approximately 230 ˚C

An SMT reflow experiment was conducted to evaluate void level and void size with different profiles. Table 2 contains the experimental legs and Figure 10 shows the profile parameters that were modulated in the experiment.

Table 2. Reflow profile experimental legs

Leg	Profile Design
1	Baseline profile
2	Long TAL
3	Short TAL
4	Short Pre-heat/Long Soak
5	Long Pre-heat/Short Soak

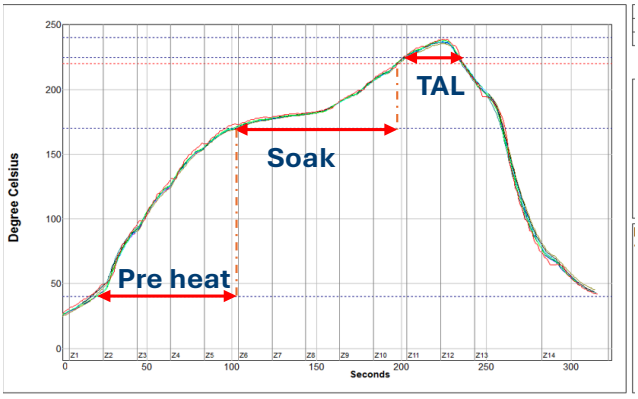
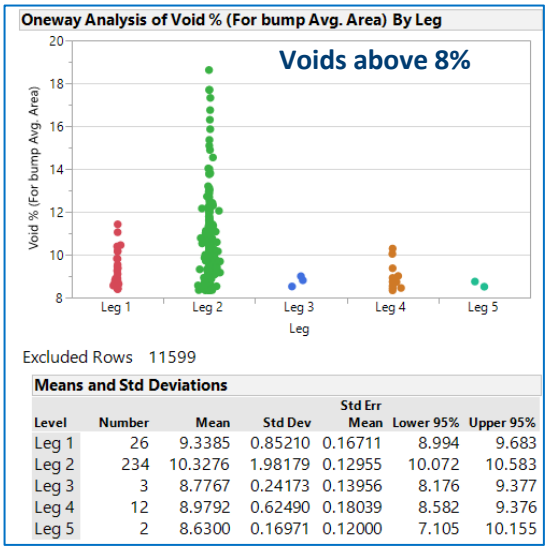


Figure 10. Reflow profile elements modulated in the characterization experiment

Five profiles were developed according to the specified legs and 12 BGA packages were mounted for each leg. The X-ray images were processed through an AI algorithm to measure the void size percentage. The comparison data is presented in Figure 11. All voids above 8% are shown.



Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
Leg 1	26	9.3385	0.85210	0.16711	8.994	9.683
Leg 2	234	10.3276	1.98179	0.12955	10.072	10.583
Leg 3	3	8.7767	0.24173	0.13956	8.176	9.377
Leg 4	12	8.9792	0.62490	0.18039	8.582	9.376
Leg 5	2	8.6300	0.16971	0.12000	7.105	10.155

Figure 11. Void percentage vs. reflow profile experimental leg

Time Above Liquidus (TAL) had the most significant impact on voiding where Leg 2 had the greatest number of voids with the largest size. Long Preheat/Short Soak (Leg 5) and Short TAL (Leg 3) had the best results with fewer number and size of voiding. In this experiment there was an attempt to change only one parameter at a time and keep all others constant to provide a cleaner signal. This is sometimes a very difficult task when creating a reflow profile. The actual profiles used through the study of reverse hybrid void characterization are shown in Figure 12.

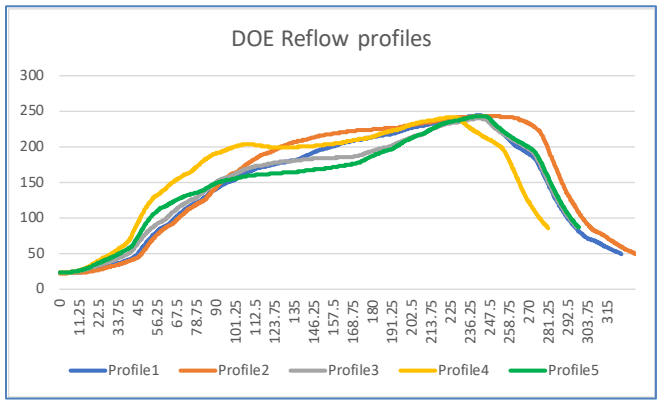


Figure 12. Summary of actual reflow profiles used by experimental leg

The results confirmed what was seen previously on the in-situ heating stage where voids were formed and grew above ~200 ˚C. Both short TAL and Long Preheat/Short Soak are reducing the total time above 200 ˚C which reduces voids.

As a result of this work, an optimized SMT process was developed and successfully enabled reverse hybrid assembly in high volume manufacturing. Although the void level is not the same as a full SAC or full LTS assembly, the reverse hybrid process was equivalent in SMT yield (Table 3) and solder joint quality.

Table 3. SMT yield comparison for Full LTS vs. Reverse Hybrid

SMT Process	Sample Size	SMT Yield (%)
Full LTS	889	100
Reverse Hybrid	2273	99.96*
* 1 unit failed for void > 30%		

REVERSE HYBRID SOLDER JOINT RELIABILITY

Temperature cycling (TC) was performed on samples with a). homogenous LTS solder joints, and b). reverse hybrid solder joints. The temperature cycle stress profile used in this study covered a temperature range from -40 °C to 100 °C, with a frequency of 60 minute per cycle. Ramp rate is not controlled in the testing profile, but a minimum 15-minute soak at both maximum and minimum temperatures were controlled.

Samples used in this study are daisy-chained test vehicles, and the same test vehicle was used for both homogeneous LTS and reverse hybrid experimental legs. All samples were monitored in-situ for electrical resistance on second level interconnect daisy chains (SLI DCs), with failure defined as 10 or more resistance spikes of 1000 Ohms or more within 100 consecutive temperature cycles. 12 samples were tested in each leg, and the final read out of this TC testing is 2500 cycles. Samples may also be pulled out from the TC chamber if all structures on them met failure criteria. In this paper, only the data of first failing SLI DC is presented for Homogenous LTS and Reverse Hybrid performance comparisons. Samples finishing stress were sent to failure analysis for more detailed inspection for failure modes and mechanisms analysis.

The first failures on the reverse hybrid samples occurred at approximately 1100 cycles, with all 12 samples failed on that SLI DC within 1700 cycles. In the meantime, first fail in Homogenous LTS DOE leg was observed in the same SLI DC structure at about 1000 cycles, with all samples failed within 1300 cycles. 2-parameter Weibull distribution was used to fit to the failure data, and the probability plot with one-sided 90% confidence interval is shown below in Figure 13. Calculated Weibull parameters for reverse hybrid and homogenous LTS are presented in Table 4. Weibull α (characteristic life) is 1239 cycles for Homogenous LTS and 1539 cycles for Reverse Hybrid, with a β (shape parameter) of 21 for Homogenous LTS and 13 for Reverse Hybrid. For both Homogenous LTS and reverse hybrid, cracks were found near the intermetallic layer, either near the board side or near the substrate side. It is also noticed more substrate-side solder joint cracks were found comparing to board-side solder joint cracking, and representative cross-section microscopic images are shown in the below Figure 14. The

in-situ data and cross-section images show that reverse hybrid solder joints perform better than homogenous LTS solder joint materials, and both showing solder joint intermetallic cracking failure mode. The improved performance of the reverse hybrid samples may be due to the presence of Ag contributed by the SAC solder paste. The homogeneous LTS solder joints did not have Ag as a constituent dopant. The beneficial impact of Ag on the reliability performance of Sn-Bi solder joints has been noted in the literature [17].

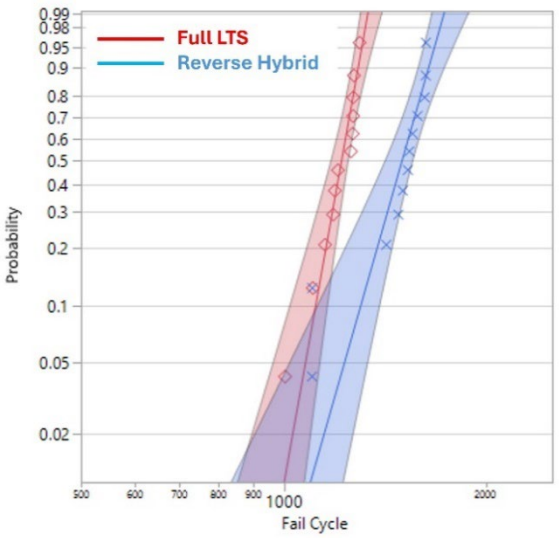


Figure 13. Weibull failure curve for Homogenous LTS and Reverse Hybrid samples in Temperature Cycling test (-40°C to 100°C).

Table 4. Weibull failure parameter estimates for both solder joint materials in Temperature Cycle condition (-40°C to 100°C).

Solder Joint Materials	Parameter	Estimate
Homogenous LTS	Weibull α	1239.0
	Weibull β	21.2
Reverse Hybrid	Weibull α	1539.4
	Weibull β	13.3

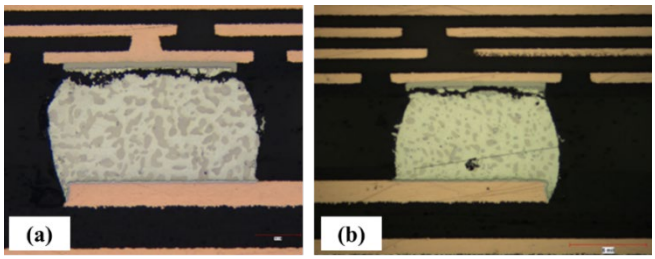


Figure 14. Cross-section images of representative solder joints after temperature cycling stress. (a) Homogenous LTS solder joint; (b) Reverse Hybrid solder joint. Joints shown are in different locations on the package and do not represent direct comparisons of cracking.

Mechanical shock was also performed on both homogenous LTS and reverse hybrid samples. The shock test was performed in a cliff-finding approach, with the same number of mechanical drops at each selected acceleration (G) level. Samples were in-situ electrically monitored in the shock testing and electrical fails (resistance spike at or above 1000 Ohms) were detected and recorded. The results of shock performances is presented in Figure 15 below, showing a numerically normalized failing G-level of first failing SLI DC in this test. Lognormal distribution was used to fit the failure data, and the shock performances were normalized using Median Time to Fail (MTTF) in G of reverse hybrid samples. Results showing better mechanical shock performances in reverse hybrid samples, with a 25% lower MTTF in homogeneous LTS samples comparing to reverse hybrid samples (Table 5).

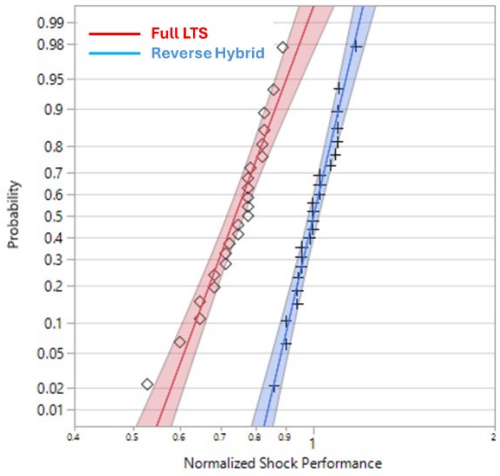
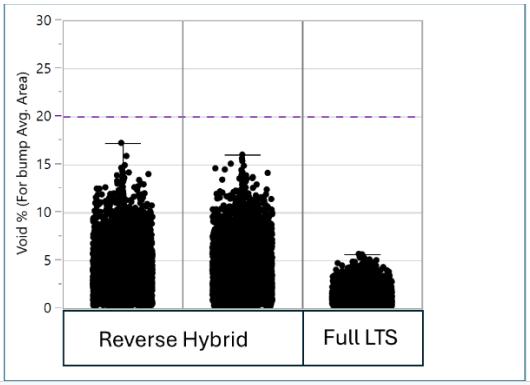


Figure 15. Relative shock performance of reverse hybrid and homogenous LTS samples.

Table 5. Weibull failure parameter estimates for both Full LTS and Reverse Hybrid in shock testing

Solder Material	Normalized Shock Performance (MTTF)	Lognormal σ
Reverse Hybrid	1.000	0.075
Homogeneous LTS	0.741	0.119

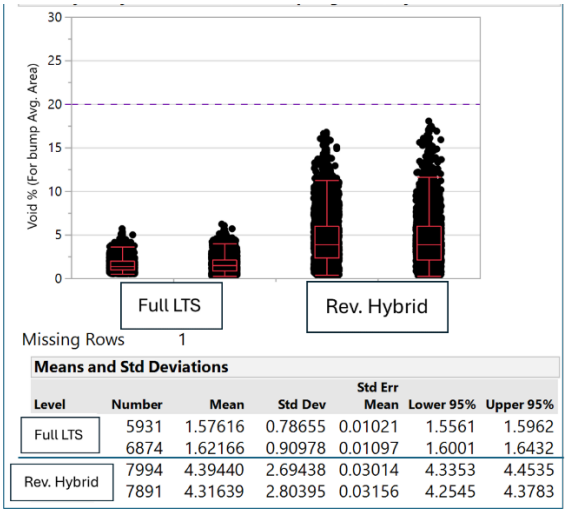
To determine if the expected increase in solder voiding for Reverse Hybrid samples had an impact on the reliability performance of the solder joints, solder voiding data was collected for both the temperature cycle and shock testing units. Figure 16 shows the void levels for both the Full LTS and Reverse Hybrid temperature cycle units. Figure 17 shows the void levels for Full LTS and Reverse Hybrid shock testing samples.



Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
Full LTS	6542	1.2762764	0.7991112	0.0098799	1.2569086	1.2956442
Rev. Hybrid	11694	3.8318026	2.4085743	0.022273	3.7881439	3.8754614
	7988	4.0383826	2.5517615	0.028551	3.9824152	4.09435

Figure 16. Void percentage results for Full LTS and Reverse Hybrid temperature cycle samples



Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
Full LTS	5931	1.57616	0.78655	0.01021	1.5561	1.5962
	6874	1.62166	0.90978	0.01097	1.6001	1.6432
Rev. Hybrid	7994	4.39440	2.69438	0.03014	4.3353	4.4535
	7891	4.31639	2.80395	0.03156	4.2545	4.3783

Figure 17. Void percentage results for Full LTS and Reverse Hybrid shock testing samples

In all cases, void levels met the acceptance criteria. Full LTS units showed significantly lower levels of voiding compared to the Reverse Hybrid samples. However, as illustrated previously, Reverse Hybrid units produced equivalent to better reliability results when compared to Full LTS solder joints.

CONCLUSIONS

Low temperatures solders (LTS) technology provides significant advancements in semiconductor package and system level process and reliability. Reverse hybrid LTS (RH-LTS) allows the already beneficial LTS technology to be easily integrated at system level by enabling a consistent SAC paste solution and reflow profile across all components on the system board. This paper demonstrates the compatibility and efficiency of RH-LTS SMT with advanced 2.5D and 3D package architectures. RH-LTS process fundamentals, failure mode analysis, as well as co-engineering dependencies such as package assembly materials, assembly process, package and board design, have been discussed. Key considerations observed for solder joint yield, quality and reliability, were identified to be optimum reflow profile, board paste material selection. Key challenges for RH-SMT process such as voiding and solder bump bridging (SBB) have been reviewed. Guidelines to overcome these fails modes during technology design, definition and certification have been elaborated on. Key areas of research for expanding the scope of RH-LTS becomes further relevant with increased drive for higher system level performances and use of heterogeneous and complex package and system designs. RH-LTS is expected to be a key technology building block to enable the next generation of advance packaging architectures such as hybrid bonding, multi-level wafer stacking, omni-directionally interconnected package complexes and co-package optics.

REFERENCES

1. Bill Trumble, "Get the lead out![lead free solder]." IEEE Spectrum, May 1998

2. C. Michael Garner, Vivek Gupta, Vivek Bissessur, Achut Kumar, and Raiyo Aspandiar. "Challenges in converting to lead-free electronics." Proceedings of the 3rd Electronics Packaging Technology Conference (EPTC), December 2000

3.Bill Birch, "Reliability testing for microvias in printed wire boards." Circuit World, November 20, 2009

4. Mark White, Jin Qin, and Joseph B Bernstein. "A study of scaling effects on DRAM reliability." Proceedings of the Annual Reliability and Maintainability Symposium, January 2011

5. Aya Fukami, Saugata Ghose, Yixin Luo, Yu Cai, and Onur Mutlu. "Improving the reliability of chip-off forensic analysis of NAND flash memory devices." Digital Investigation, 20, 2017

6. E.S. Shepherd, "Alloys of Tin, Lead and Bismuth." The Journal of Physical Chemistry, 2002

7. Aileen Allen, Helen Holder, Elizabeth Benedetto, "A Review of the Impact of Dopants in Sn-Bi Solder Alloys", Proceedings of the SMTAI Conference, Minneapolis, MN, 2022

8. Fengjiang Wang, Hong Chen, Ying Huang, Luting Liu, and Zhijie Zhang. "Recent progress on the development of Sn–Bi based low-temperature Pb-free solders." Journal of Material Science: Materials in Electronics, 2019

9. Chongyang Cai, Jiefeng Xu, Huayan Wang, and SB Park. "A comparative study of thermal fatigue life of Eutectic Sn-Bi, Hybrid Sn-Bi/SAC and SAC solder alloy BGAs." Microelectronics Reliability, 119, 2021

10. Haley Fu, Jagadeesh Radhakrishnan, Morgana Ribas, Raiyo Aspandiar, Kevin Byrd, Jimmy Chen, Shunfeng

Cheng, Qin Chen, Richard Coyle, and Sophia Feng, "iNEMI Project on Process Development of BiSn-Based Low Temperature Solder Pastes, Part III: Mechanical Shock Tests on POP BGA Assemblies", Proceedings of the International Conference on Electronics Packaging (ICEP), April 2018

11. Lee, Jihyun, Yongsung Park, Junho Lee, Kangjoon Lee, Hansung Ryu, JeeHyun Jung, and Kilsoo Kim, "Risk Assessment of Hybrid Low Temperature Solder on Surface Mount Technology and Board Level Reliability for BGA Packages", Proceedings of the IEEE 73rd Electronic Components and Technology Conference (ECTC), 2023

12. Henshall, Gregory, Robert Healey, Ranjit S Pandher, Keith Sweatman, Keith Howell, Richard Coyle, Thilo Sack, Polina Snugovsky, Stephen Tisdale, and Fay Hua. "Addressing Opportunities and Risks of Pb-Free Solder Alloy Alternatives", Proceedings of the European Microelectronics and Packaging Conference, June 2009.

13. Shubhada Sahasrabudhe, Scott Mokler, Mukul Renavikar, Sandeep Sane, Kevin Byrd, Eric Brigham, Owen Jin, Pubudu Goonetilleke, Nilesh Badwe, and Satish Parupalli, "Low Temperature Solder – A Breakthrough Technology for Surface Mounted Devices", Proceedings of the IEEE 68th Electronic Component and Technology Conference (ECTC), 2018

14. Todd Harris, Kevin Byrd, and Nilesh Badwe, "Root Cause and Solutions to Mitigate the Hot Tear Defect Mode in Hybrid SAC-Low Temperature Solder Joints", Proceedings of the SMTAI Conference, Chicago, IL, September 2019

15. Kevin Byrd, Satyajit Walwadkar, Jason Stafford, Pubudu Goonetilleke, and Raiyo Aspandiar, "Component Side Hot Tear Defect Root Causes and Control in Full LTS Solder Joints", Proceedings of the SMTAI Conference, Virtual, September, 2021

16. IPC-7095C, "Design and Assembly Process Implementation", IPC Ball Grid Array Task Group (5-21f), Assembly & Joining Process Committee (5-20) of IPC

17. M. McCormack, H.S. Chen, G.W. Kammlott, and S Jin, "Significantly Improved Mechanical Properties of Bi-Sn Solder Alloys by Ag-doping", Journal of Electronic Materials, Vol. 26, No. 8, August 1997ss