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Low Temperature Solder-SMT Manufacturability and Quality Considerations For BGA Components

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ABSTRACT
Low temperature solder (LTS) applications have been gaining momentum in the electronics industry offering major advantages compared to traditional Pb-free alloys, specifically, enabling advanced technology scaling combined with the value proposition of reduced carbon footprint. This study focuses on developing manufacturing & solder joint quality understanding for Sn-Bi based alloys. Investigation of Hybrid LTS process (defined as SAC305 ball-grid array (BGA) package reflowed to a printed circuit board (PCB) using LTS paste technology) with a focus on major challenges with surface-mount technology (SMT) assembly and key parameters to improve processability. Additionally, a preliminary manufacturing and solder joint quality assessment for Homogeneous LTS BGA interconnects will be reviewed, highlighting the full benefits of transitioning LTS technology.

Key words: Low Temperature Solder (LTS), Warpage, Hybrid LTS, Homogeneous LTS, Surface Mount Technology (SMT)

INTRODUCTION

A successful SMT manufacturing requires physical contact between paste printed on PCB and the package (PKG) BGA. Electronic assemblies are seldom flat and have inherent 'warpage' due to coefficient of thermal expansion (CTE) mismatch within the package stack-up and need to be controlled within an acceptable window. Figure 1 shows a typical flip chip package dynamic warpage trend during reflow. Note: The package shape can change from convex to concave and visa-versa, additionally, the overall shape can be non-symmetric due to design requirements for a specific BGA packaging architecture (i.e., process and assembly material differences) as shown by the contour images in Figure 2a for two different PKG designs. Additionally, as shown in warpage overlay image in Figure 2b, the package-board warpage interaction is a critical factor in understanding the SMT trends for healthy solder joint yields.

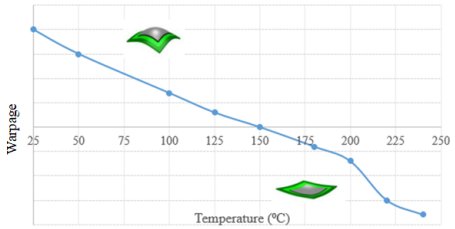
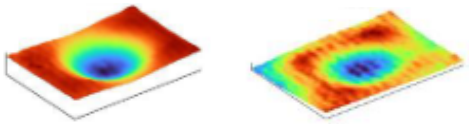


Figure 1. Example of a typical Flip chip BGA package dynamic warpage trends.



PKG A PGK B

Figure 2a. Example PKG warpage contour profiles due to different assembly processes & materials.

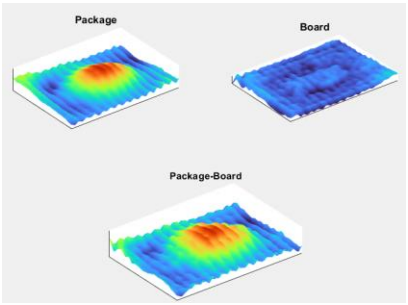


Figure 2b. Example PKG-PCB warpage overlay.

The excessive shape and magnitude warpage mismatch can lead several different defect modes as shown in Figure 3.

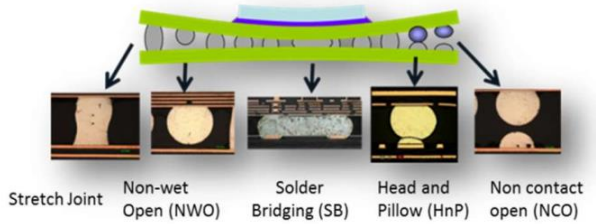


Figure 3. Typical SMT defect modes [1].

Sn-Bi based LTS alloys melting ranges from 138ºC ~175ºC (in contrast to ~217ºC for traditional SAC305), which allows for a lower SMT peak reflow profile, (Figure 4) translating to an overall reduced package warpage magnitude.

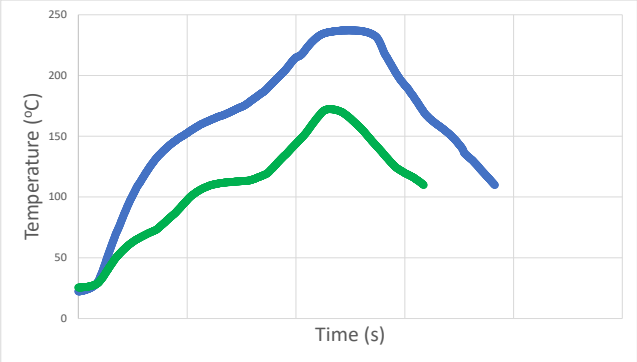


Figure 4. SAC305 vs LTS reflow profiles.

Sn-Bi pastes are categorized into near-eutectic (57-58wt%Bi) and off-eutectic (35-40wt%Bi) alloys which present different tradeoffs between manufacturability and reliability [1-4]. To maximize LTS SMT yields, it is critical to understand package warpage behavior in conjunction with PCB warpage to identify optimal material selection and corresponding process parameters. This paper focuses on establishing package warpage boundary conditions and identifying key process parameters for a successful LTS assembly [5-8].

While LTS process appears to reduce package and board warpage in general, there is an increased sensitivity to maximum dynamic warpage value and 'inversion' temperature range that increases risk, specifically for Hybrid LTS SMT. This arises due to lack of homogenization or 'collapse' of package solder ball (SAC305) into the LTS paste as shown in schematic in Figure 5. Shape inversion refers to the temperature at which package changes shape from 'crying' to 'smiling' or vice versa. For example, referring to Figure 1, shape change occurs at ~150ºC. As the package pulls away from board while the LTS solder is in the pasty range, another defect mode called 'hot tear' (Figure 6) is observed, typically under the stiffer die area. For homogeneous assemblies, requirements for warpage are well established under JEDEC standards, however, no such industry standard guidance exists for hybrid joints. This study focuses on understanding limitations with Hybrid LTS SMT and key parameters that need optimization to increase the manufacturing process window.

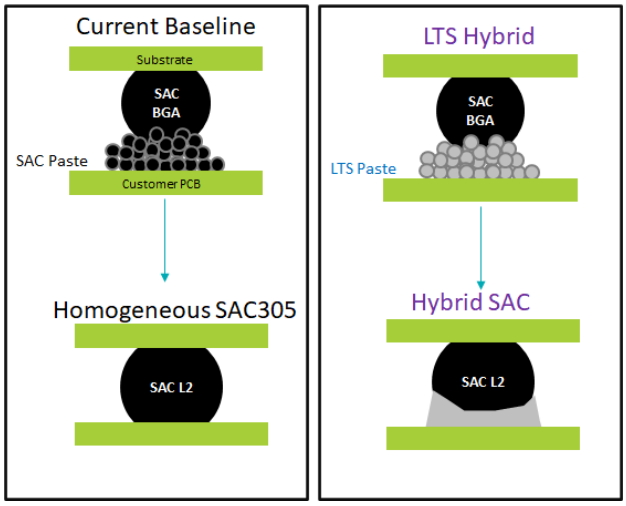


Figure 5. Schematic showing the difference in post SMT solder joint height between Homogeneous and Hybrid solder joints.

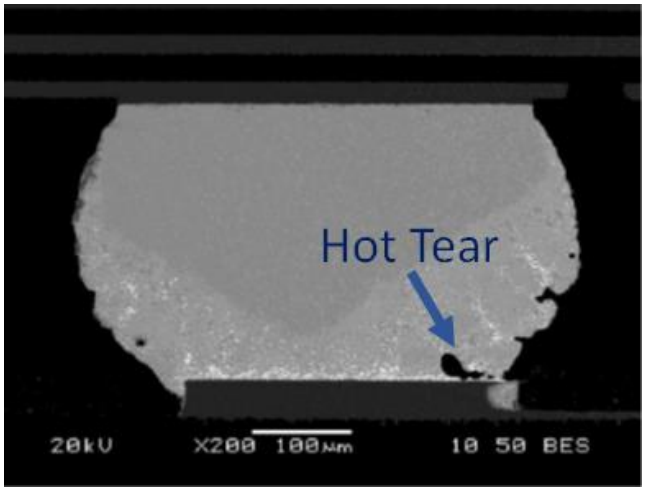
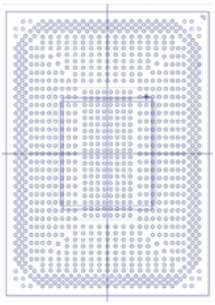


Figure 6. Example SEM image of a Hybrid LTS hot tear defect signature.

EXPERIMENTAL DETAILS

Package attributes for this study are listed in Figure 7, both PKG A and PKG B met JEDEC warpage requirements (-140um to 220um) with good margin for Pb-free SMT. Two LTS solder pastes were selected: Near-eutectic (NE) (MP: 137-142ºC) and Off-Eutectic (OE) (MP: 139-174ºC) alloys. The PCB used for this study was a 140mmx140mm, 1.04mm thick form factor with Cu-OSP surface finish as shown in Figure 8.



Package Attributes	
Package (A, B) Type	**FCBGA**
Package Size	**25 mm x 35 mm**
Pitch	0.64min
BGA pad design	SMD
BGA pad surface finish	ENEPIG

Figure 7. BGA Pin Map and general PKG test vehicles attributes.

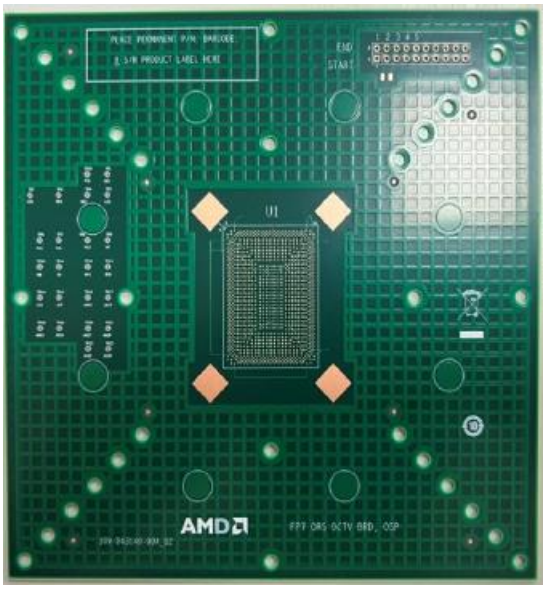


Figure 8. SMT PCB board design, 140mmx140mm-thickness 1.04mm/CuOSP.

A full investigation looking at overall process parameters was conducted. This included Paste Materials; Stencil Design; Pallet Design; Pick & Place Conditions; Reflow Profile. Figure 9 shows the two reflow profiles investigated as part of this study which complies with the IPC 7530 standard. Figure 10 shows the optimized stencil design with five different aperture zones. The paste volume was monitored for all SMT assessments to ensure uniform solder print quality as shows in Figure 11 for all five different aperature zones (A to E).

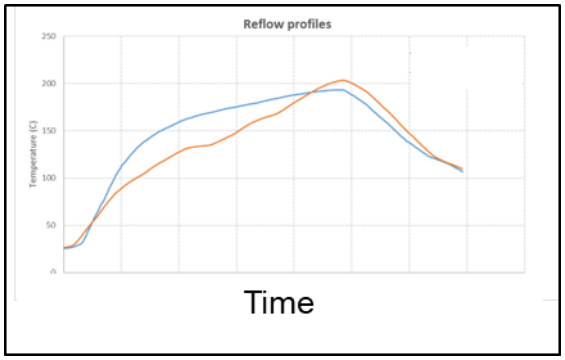


Figure 9. Example of the LTS Reflow profiles used in this study.

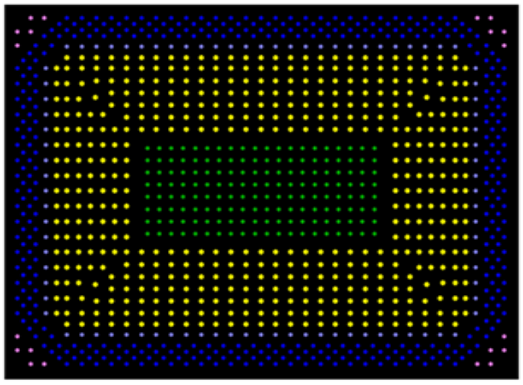


Figure 10. Example of the optimized stencil design.

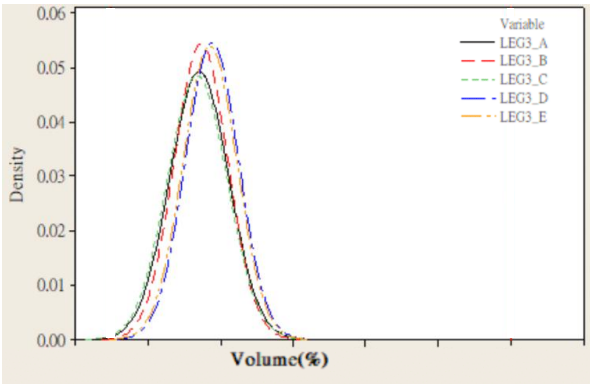


Figure 11. Example histogram plot of paste volume print uniformity within five aperature zones.

RESULTS

Hybrid LTS SMT

SMT baseline showed PKG A had higher sensitivity to head in pillow (HiP) defect mode at corners while PKG B primarily showed hot tear defect mode under the die area as shown in Figure 12 (a) and (b),

respectively. Also, for same package type, NE paste showed better resistance to HiP compared to OE paste. For hot tear, however, OE paste had superior performance.

Figure 12. (a) PKG A x-section view (HiP at corners).

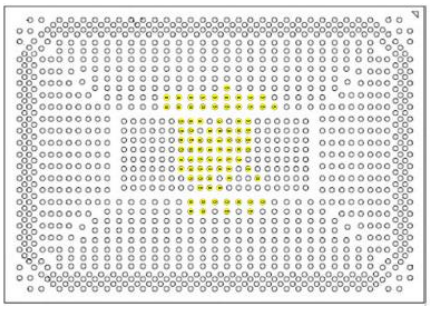


Figure 12. (b) Example of PKG B top view (Hot tear mapping) via dye and pry.

PKG A vs PKG B HiP performance indicates that dynamic warpage for hybrid LTS should be within given warpage window to ensure LTS paste wets the un-melted SAC305 ball, as shown in Figure 13. This is roughly half the capability of Pb free JEDEC acceptable warpage. PKG B showed higher propensity to hot tear defects due to higher delta warpage during solidification, where joints under die are pulled away from paste before it fully solidifies.

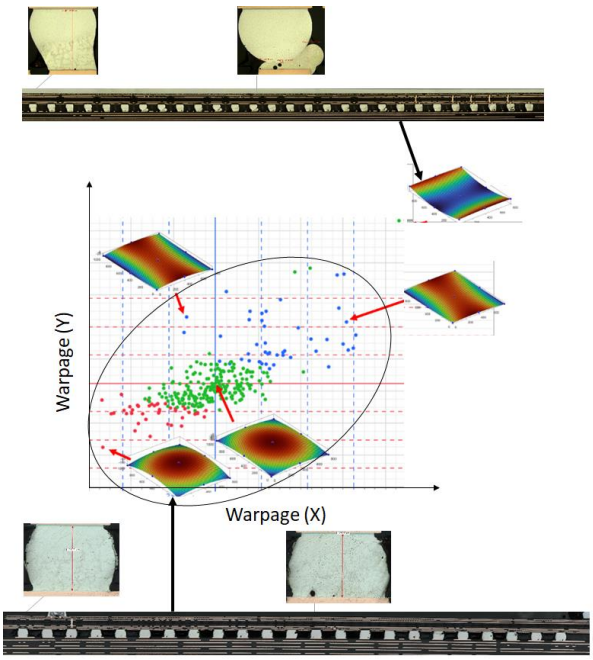


Figure 13. Hybrid LTS interaction with PKG warpage trends.

The key reflow and solder paste process parameters considered to improve both HiP and hot tear defect modes were increasing TAL, peak reflow temperature and paste-to-ball (P:B) ratio. Note: The P:B ratio is the volume of LTS paste divided by SAC305 BGA ball volume on package. Figure 14 illustrates the results/trends from multiple experiments conducted for process variables noted above.

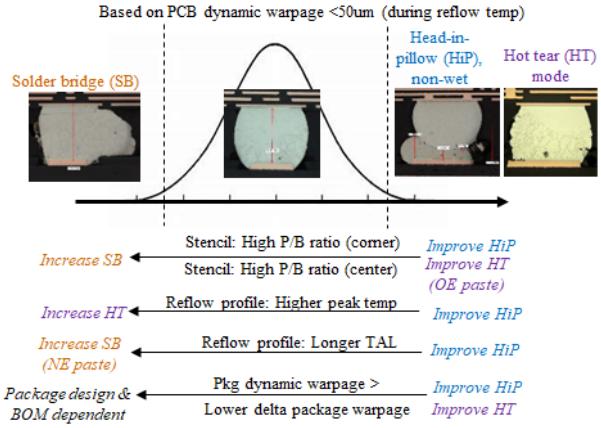


Figure 14. Impact of SMT variables on defect modes.

For HiP defect mitigation, higher peak reflow >190ºC temperature had a significant impact. A higher P:B ratio in affected corners improved HiP but shifted fail mode to solder bridge for PKG A. PKG A was determined more sensitive for hybrid SMT and further increasing peak temperature to >200ºC was the only knob for Hybrid LTS compatibility from a process standpoint. For PKG B, increasing P:B under die area helped mitigate hot tear due to higher liquid fraction solder volume reducing 'tearing'.

A study by Harris et al. [8] identified lower peak reflow as key factor to resolve this defect mode, but the current study shows this triggers HiP defects for certain package warpage shapes, thus needs to be carefully evaluated and optimized for any given BGA. OE paste showed higher resistance to hot tear compared to NE, opposite to the general theory of wider solidification range being worse for this defect mechanism. The dopant chemistry for the SMT paste used in this study may modulate this through the undercooling effect.

Homogeneous LTS SMT

Preliminary Full LTS SMT lookahead studies have demonstrated healthy package yields. Quality checks for ball pull and shear exceed SAC305 baseline as highlighted in Figure 15. Additionally, 100% SMT yield (On par with SAC305) was observed for all LTS ball alloys evaluated (Figure 16). This highlights the full benefit of using LTS technology for maximum warpage mitigation; during SMT unlike hybrid LTS process since we have both early melt and full solder joint collapse. This correlates well to the benefits of full LTS BGA interconnects for SMT quality demonstrated for across client and server like BGA PKGs by others research to date [9-12].

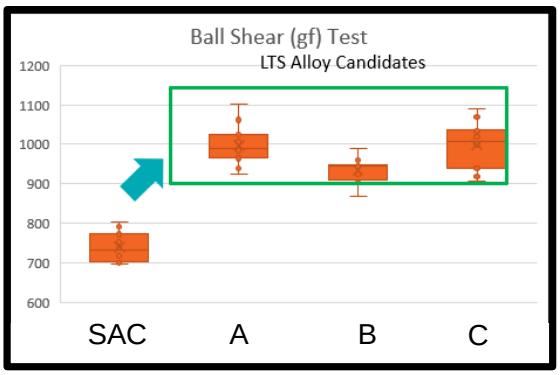


Figure 15. Ball Shear trend for LTS ball candidates vs. SAC305 baseline.

BGA Ball alloy	Ball Attach yield	SMT yield	T0 X-section
Alloy A (Off-Eutectic)			
Alloy B (Near-Eutectic)			
Alloy C (Off-Eutectic)			

Figure 16. Risk trends for full LTS ball attach and SMT assembly using key LTS candidates.

CONCLUSIONS

This study highlights the importance of component supplier LTS assessments to ensure smooth transition and overall readiness of future LTS industry conversions. To summarize, this study comprehends Hybrid LTS SMT limitations based on package warpage boundary conditions and narrow process window due to opposing defect modes. Unless there is a significant reduction in package warpage between 190ºC to 240ºC (e.g., Package A from Fig 6), risks outweigh benefits for Hybrid LTS. Based on extensive characterization, the team was able to establish package boundary conditions best suited for different HVM SMT conditions as shown in Figure 17. The transition to a homogeneous LTS BGA interconnect allows for a much wider warpage range and overall larger process window compared to both SAC305 and Hybrid LTS and would be the preferred overall path for enabling LTS system assembly.

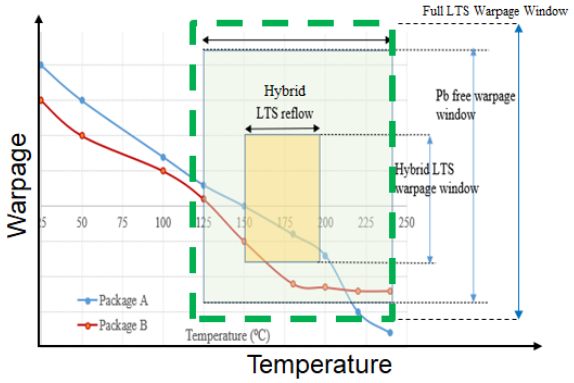


Figure 17. Hybrid LTS vs SAC305 homogeneous SMT: Package warpage window.

FUTURE WORK

Reliability studies corresponding to different paste materials for Hybrid LTS and Homogeneous LTS are currently in progress to understand tradeoffs compared to Pb free baseline. Continued engagement with ODMs/OEMs and paste suppliers for optimized use condition and material formulations will continue.

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