

Large Form Factor Surface Mount Technology Process Demonstration

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ABSTRACT

Electronic packaging form factors are increasing due to high performance computing and artificial intelligence needs. The resulting package coplanarity and dynamic warpage of these large form factor Ball Grid Array (BGA) packages at Tin Silver Copper (SAC) alloy reflow temperatures are trending to increase and push the limits of existing Surface Mount Technology (SMT) capabilities. Increase in package warpage and poor SMT yield is driving a need for new technologies to enable successful component soldering to the motherboard. This paper reviews the implementation of a multiple solder ball diameter (MDSB) strategy to increase the SMT warpage capability for a standard SAC BGA Package. SMT time zero solder joint quality (SJQ) and SMT yield results are presented along with key learnings and next steps.

Key words: Surface Mount Technology, Ball Grid Array, Server, CPU, GPU, Flip Chip, Warpage, Coplanarity, Flatness.

INTRODUCTION

Emerging technologies such as 2.5D and 3D silicon stitching are enabling substantially larger electronic BGA package dimensions [1][2][3][4][5]. Where historically packages were limited by the maximum reticle size, package sizes are now trending up to eight reticles worth of silicon (8xR) and 120 x 120 mm substrate size. This increase in silicon and substrate area results in an increased range of package dynamic warpage during the SMT reflow process and warpage ranges exceeding JEDEC standards [6]. Additionally, the increase in package footprint on the Printed Circuit Board (PCB) increases the PCB flatness of the solder pads on the PCB [7]. The combined effect of the increased package warpage and PCB flatness significantly increases the risk for SMT defects such as solder joint bridging and solder joint opens [8][9].

Low Temp Solder (LTS) is an existing solution to combat package warpage. LTS requires SMT reflow at a peak temperature up to 190°C vs SAC peak reflow temperatures of 245°C [10][11]. This temperature reduction significantly reduces package warpage and enables SMT soldering. However, LTS solder has physical limitations and

enablement challenges that can drive package design to require a SAC solder alloy [12].

To address this emerging packaging need, we have proposed and validated a multiple diameter solder ball technology (MDSB) BGA design that extends previously demonstrated ball attach capabilities to enable BGAs with multiple solder ball types and solder ball diameters [13]. This allows package designers to fine tune the BGA interface to extend the SMT package warpage capabilities and enable the SMT of large form factor BGAs. In this paper, we demonstrate the process by using test vehicle BGA 11026 and go through the steps of testing the SMT capabilities of a package with a MDSB BGA.

MULTIPLE DIAMETER SOLDER BALL STRATEGY OVERVIEW

The MDSB strategy optimizes the BGA solder ball diameters to the package and board warpage. Instead of using a single solder ball diameter across the whole BGA field, smaller solder balls are placed at high compression locations and larger solder balls are placed at high stretch locations. The small solder balls allow the substrate to be closer to the PCB without solder joint bridging occurring. The larger solder balls allow the substrate to be further away from the PCB without solder opens forming. This benefit is shown in Figure 1. The BGA in schematic A has a single solder ball diameter and solder joint bridges form at the high compression center location and solder joint opens form at the high warpage edge locations. The BGA in schematic B depicts a package with larger solder balls at the edges which prevent the warpage driven solder joint open defects from occurring and smaller solder balls at the center that prevent the solder joint bridging.

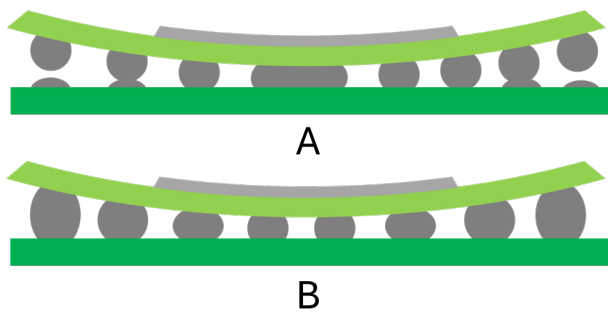


Figure 1: A) Single Solder Ball BGA package schematic. B) Mixed Diameter Solder Ball BGA package schematic

This enables successful soldered to the PCB in higher package and/or PCB warpage combinations than on a single solder ball diameter package.

COLLATERAL AND EXPERIMENT OVERVIEW

Collaterals

Two different flavors of BGA 11026 were used to validate the MDSB strategy. Details about the two different flavors are shown in Table 1. The MDSB pattern used on the package design is shown in Figure 2. In-house ball attach capabilities that allow for up to 4 different solder ball diameters and/or materials to be placed in high volume manufacturing was used to assemble the packages. The substrate solder resist opening (SRO) was skewed to match the solder ball diameter such that the 20 mil solder balls use a 480 μm SRO and the 24 mil solder balls use a 560 μm SRO. A close-up image of the transition zone from 20 mil to 24 mil solder balls on the package is shown in Figure 3. Copper core solder balls were also placed on the package at strategic locations to control the package collapse and prevent bridging. A cross section of a copper core is shown in Figure 4. In total, four different solder ball types were used on this package, two majority SAC solder balls with diameters of 24 mils and 20 mils and two minority copper core solder balls with diameters 14 mils and 10 mils.

Table 1: BGA 11026 Test Vehicle Key Attributes.

Attribute	BGA 11026 Lid	BGA 11026 Stiffener
Lid or Stiffener Thickness	Lid: 2mm Ni plated Cu	Stiffener: 2.5mm Stainless Steel
Package Weight	300 grams	140 grams
Package Length	115 mm	
Package Width	95 mm	
Die Area	5808 mm^2	
Pitch	1 mm	
# Solder Balls	11026	
Solder Ball Diameter(s)	24 mil / 20 mil / 14 mil Cu core / 10 mil Cu Core	
Solder Ball Type	SAC	

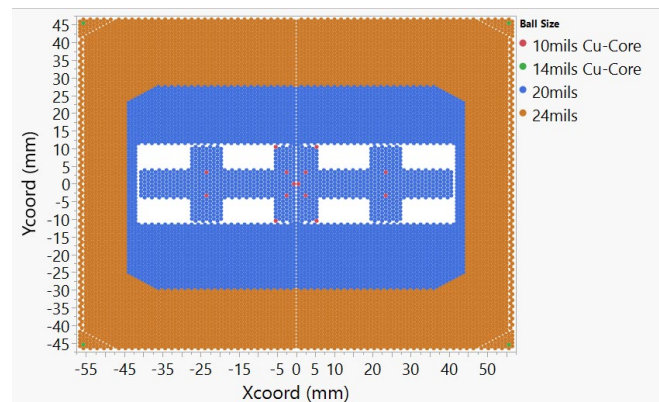


Figure 2: BGA 11026 MDSB pattern.

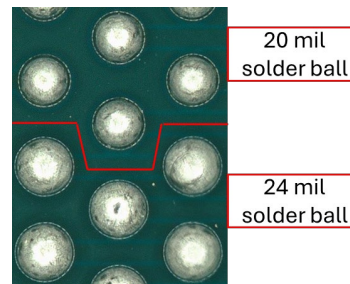


Figure 3: Image of 20 mil to 24 mil solder ball diameter transition zone.

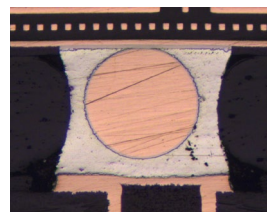
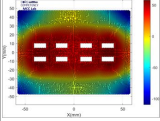
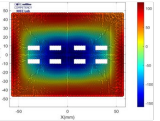
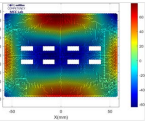
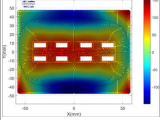
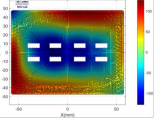
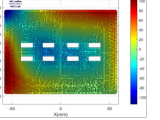


Figure 4: X-section of a copper core to prevent package collapse.

The package room temp coplanarity, 260°C warpage, and return (cooling) 200°C warpage was measured and is shown in Table 2. Where the positive sign convention is convex (frowny face) and the negative sign convention is concave

(smiley face). Specifically, blue regions are warping towards the PCB and red regions are warping away from the PCB.

Table 2: BGA 11026 Lid and Stiffener Room Temp Coplanarity and High Temp Warpage

Package	Room Temp COPL	260°C Warpage	200°C Return Warpage
BGA 11026 Lid	168um 	-276um 	-143um 
BGA 11026 Stiffener	299um 	-255um 	-217um 

Multiple PCB designs were used to evaluate the two different packages. The key factors of the different PCBs are shown in Table 3. The PCB pad diameters were skewed to match the solder ball diameters on the package such that the 20 mil solder balls used a 430 um pad diameter and the 24 mil solder balls use a 500 um pad diameter.

Table 3: PCB attributes.

Attribute	Value
PCB Length	160.4 mm
PCB Width	154.4 mm
Thickness	3.175 mm
Layer Count	28

The PCB room temperature coplanarity was measured and is shown in Figure 5. The high temperature warpage of the PCB was measured and found to be within 20 um of the room temperature coplanarity. Indicating that the PCB warpage during reflow is minor and can be considered noise.

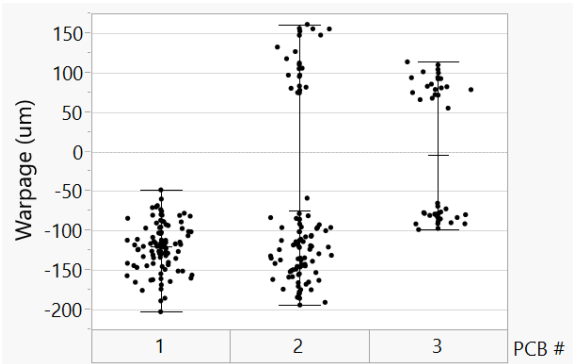


Figure 5: Room Temp PCB warpage.

The final assembly is shown in Figure 6.

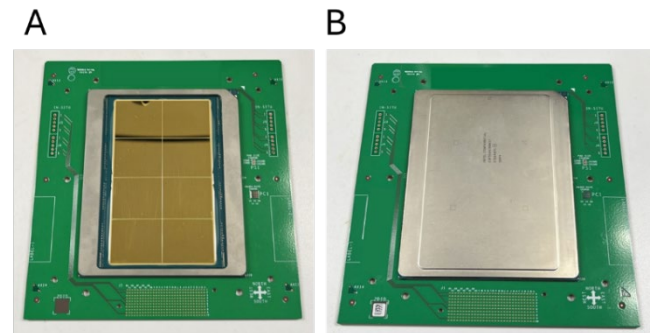


Figure 6: Final assembly image. A) Stiffener version. B) Lidded version.

Experiment

A standard SAC SMT reflow profile and process was used. The stencil design is shown in Figure 7. The stencil design was kept the same for both the lidded and stiffener version of the package.

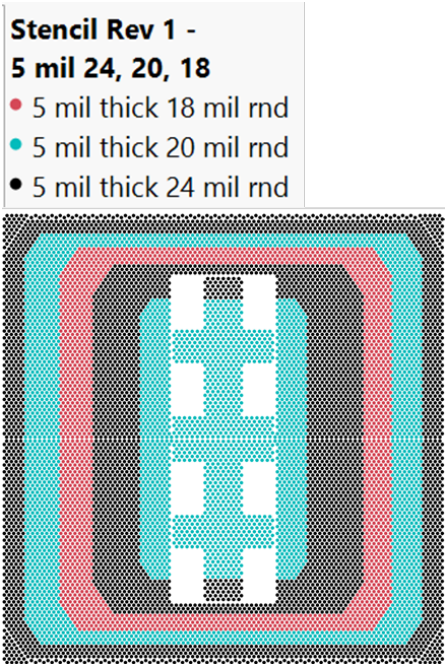


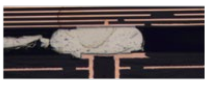
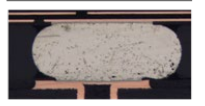
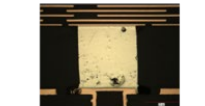
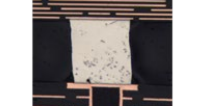
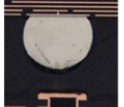
Figure 7: Stencil design.

Forty BGA 11026 lid units were assembled and sixty-eight BGA 11026 stiffener units were assembled. The PCB warpage was tracked to check for sensitivity to PCB warpage. All units went through X-ray inspection and dye and pry inspection to confirm the absence or presence of SMT defects. Additional hammer conditions were used to create solder bridge defects and open defects. To create the bridge defects, the Cu cores were removed from the packages and weight was applied to cause solder joint compression. To create open defects, the stiffener was removed from the package to increase package warpage.

RESULTS

The hammer leg results were used to determine solder joint height (SJH) values for when a 20 mil and 24 mil ball would bridge, bulge, have a column shape, and form an open. The results are shown in Table 4. SJH is defined as the distance from the top of the PCB pad to the bottom of the substrate pad.

Table 4: Solder joint shape based on solder joint height.

Solder Joint Shape	20 mil	24 mil
Bridge	SJH: 200 um 	SJH: 300 um 
Bulge	SJH: 250 um 	SJH: 350 um 
Column	SJH: 500 um 	SJH: 600 um 
Open	Not Observed	SJH: 700 um 

From these results, we conclude that the minimum SJH for a 20 mil ball is 250 um and the minimum SJH for a 24 mil ball is 350 um before the risk of a solder bridge forming is too high. This indicates that by using 20 mil solder balls at the center of the package we are able to achieve 100 um more collapse compared to the 24 mil solder ball. Translating to 100 um more warpage budget.

This warpage budget was further expanded to determine the maximum package and board warpage that could be tolerated. Figure 8 depicts the warpage budget breakout. Where A is the package warpage, B is the minimum solder joint height on the package, and C is the board warpage.

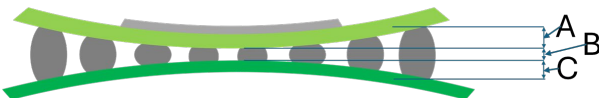


Figure 8: Warpage budget breakout.

For a single solder ball diameter package with 24 mil solder balls, we can conclude that the minimum SJH (B) before the bridge risk is too high is 350 um and the max SJH before an open risk is too high (A+B+C) is 600 um. Giving a total PCB + Package warpage budget of 600 um - 350 um = 250 um.

For a MDSB package with 24 mil and 20 mil solder balls, we can conclude that the minimum SJH (B) is 250 um and the max SJH before an open risk is too high (A+B+C) is 600 um. Giving a total PCB + Package warpage budget of 600 um - 250 um = 350 um. Indicating again that the MDSB package design increases the warpage budget by 100 um. It is also key to keep in mind that these warpage numbers are based off of cross section data which captures the package at SAC solidification temperatures of 217°C. A package and/or PCB could warp to some level beyond these values at peak reflow and still successfully form solder joints as long as the package and board warpage is below the budget at solder joint solidification.

The SMT results are shown in Table 5. Based off of the results, we were able to demonstrate successful SMT of a package with 260°C warpage of 276 um and 255 um for the lidded and stiffener version respectfully on a range of board warpage from -200 um to 150 um.

Table 5: SMT Results.

Package Skew	Quantity Built at SMT	SMT Yield
BGA 11026 Lid	40	100%
BGA 11026 Stiffener	68	100%

CONCLUSION

The increased SMT warpage capability for the MDSB strategy was proven through the SMT yield results. Indicating that the MDSB strategy can provide a SMT solution for high warpage BGA packages. The proposed SMT budget also highlights the balance between package warpage and PCB warpage and how controlling both is crucial to establishing a successful SMT process.

This new technology pushes the envelope in previously established SMT package room temperature and high temperature coplanarity and warpage standards and highlights a need for the revision of these standards to enable future large form factor packaging being designed to fulfill future computing needs. We see this as an area where new definitions and standards will be required within the industry to allow for these increasing warpage trends and new technologies being developed to enable them. We also see an increase in PCB warpage within the BGA PCB pad field playing a crucial role in SMT success where historically PCB warpage was not a primary focus. We see this as another area where the industry will need to develop new ways to reduce the range of PCB warpage and warpage variation to enable future package SMT.

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