Investigation of Overprinting BGA Pads: It Should Print Better Than This!

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ABSTRACT
Stencil apertures for BGA components are traditionally round shaped to match the land pad geometry, and when spacing permits, it is common to enlarge the aperture size relative to the pad to achieve an overprint condition. The added benefit of using overprinting stencil design strategy is that this should compel further improvement in paste transfer efficiency and uniformity by raising its area ratio. In this study the circle shape overprint apertures were designed for 0.5mm pitch BGA land patterns that measured to an area ratio value of 0.70. While such sized apertures should produce quite acceptable print quality, the resulting print volumes for a customer application were unexpectedly non-uniform and lower in solder paste transfer efficiency despite using a well setup stencil printing machine and process. Deeper investigation identified pad design factors interacting with stencil aperture gasketing thought to be the main factors contributing to inhibited paste transfer performance. This body of work ultimately serves to improve stencil design logic applied to BGA printing applications.

Key words: Aperture, area ratio, BGA, overprint, printing, solder mask, solder paste, stencil, transfer efficiency.

INTRODUCTION

A successful SMT printing process entails depositing the correct volume solder paste material through a template of aperture holes in a stencil foil to form reliable solder joints that connect electronic components to a circuit board. Design rules for stencils are well known and must be obeyed. Selection of stencil foil thickness can be simply specified as the thickest foil that will provide adequate paste transfer through the smallest aperture holes in the stencil. The stencil area ratio guideline defined by Eq. (1) clarifies acceptable aperture size and foil thickness. Note the minimum area ratio value of 0.60, which has been changed in recent years from the more restrictive and traditionally well-known value of 0.66, reflecting improvements in today's printing capability [1].

$$\text{Area Ratio (AR)} = \frac{\text{Aperture Opening Area}}{\text{Aperture Wall Area}} \geq 0.60 \qquad (1)$$

Stencil design for printing BGA circuit board pads is also straightforward and follows the above stated logic. A simple strategy often used is to just copy the size and shape of the BGA pad in stencil design, known as making a 1:1 design. If the stencil thickness complies with the area ratio guideline, then no other stencil design adjustment is required (in theory). However, there are reasons one may choose to make the stencil aperture size larger or smaller than the pad. Figure 1 shows three stencil design conditions defining aperture size relationships to pad. This research is focused exclusively on studying the behavior of solder paste printing for stencil apertures designed to overprint the pad.

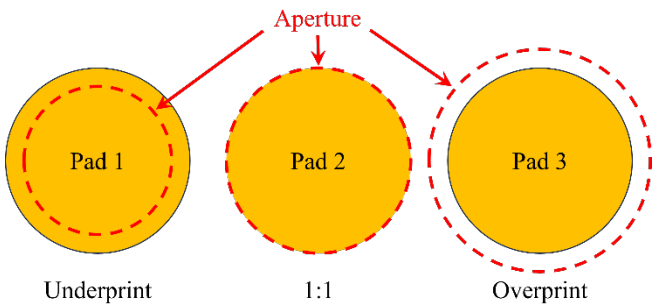

Figure 1. Aperture size strategies for same pad size.

The strategy to overprint BGA pads is practiced for any of the following reasons:

- Selection of stencil thickness may require a large aperture size to maintain a compatible area ratio.
- The pad sizes are too small to accommodate 1:1 or underprint apertures that still comply with a compatible area ratio level.
- More solder paste print volume per pad is desired to ensure yield and/or reliability [2].

A comprehensive discussion of BGA design and assembly process guidelines can be found here [3].

CHALLENGE

A stencil printing test was conducted at a customer site using a supplied nano coated stencil and circuit board containing a variety of land patterns. The print deposit volume transfer efficiency measurements on targeted 0.5mm pitch BGA pads showed statistically acceptable scatter levels at or slightly below 10% standard deviation, but better results were considered possible through print process optimization. Further visual investigation of the solder printed boards revealed some unexpected observations:

- The solder mask opening registration varied from board to board.

- The overprint design aperture size was frequently under printing the pad as shown in Figure 2.

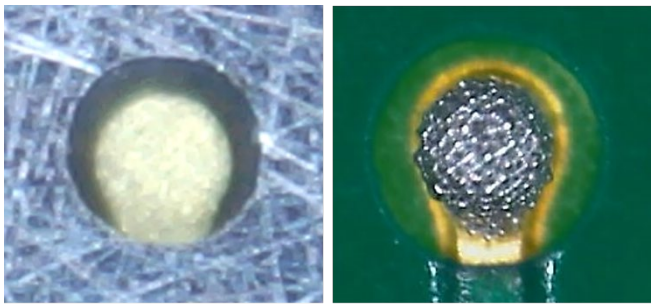

Figure 2. Smaller than expected print volume result.

In Figure 1 the left image shows a single stencil aperture in aligned contact to the underlying BGA pad. The right image represents an example solder print deposit bounded by the non-solder mask defined BGA pad. The expectation was not to see much of any metal pad in the print photo since the aperture size is so much larger. In this case the pad is designed at 254µm (10 mil) diameter. The stencil aperture is designed at 279.4µm (11 mil) using a 101.6µm (4 mil) stencil thickness giving an area ratio of 0.7, which should permit full paste transfer and well-formed paste deposits. Another observation with the solder paste inspection (SPI) data was that the use of a non-nano coated stencil tended to raise the print volume transfer efficiency standard deviation level above 10% for this application, revealing the importance of using the coating. A test to further investigate this under printing result was conceived using non-customer materials.

TEST STRATEGY

A fixed stencil design matched to the 0.5mm pitch 84 I/O BGA customer application was created using the same 279.4µm (11 mil) circle apertures with 101.6µm (4 mil) stencil thickness in a dual image 29x29 mesh mount frame. Figure 3 shows the stencil artwork for one BGA aperture footprint group. The BGA aperture footprints were stepped and repeated across several rows and columns for both front and rear stencil images. The font stencil image had stencil apertures nano coated and the rear image was not nano coated.

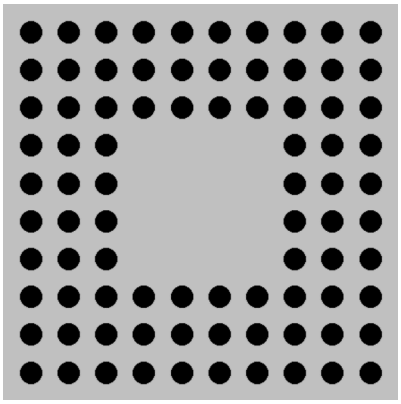

Figure 3. 84 I/O BGA stencil aperture group (AR = 0.7).

Circuit boards of several types and sizes from available stock using 0.5mm pitch BGA land pattern designs were investigated to identify candidates that could accommodate alignment using the overprint BGA stencil design referenced in Figure 3. A method of accurately printing non-stencil matched boards to this stencil using a unique video-model fiducial function was devised. This opens opportunities to use the same stencil on all sorts of different boards. Figure 4 shows a BGA aperture footprint group (grey color is stencil) that is well-aligned to component pads (red color is PCB features) using this strategy.

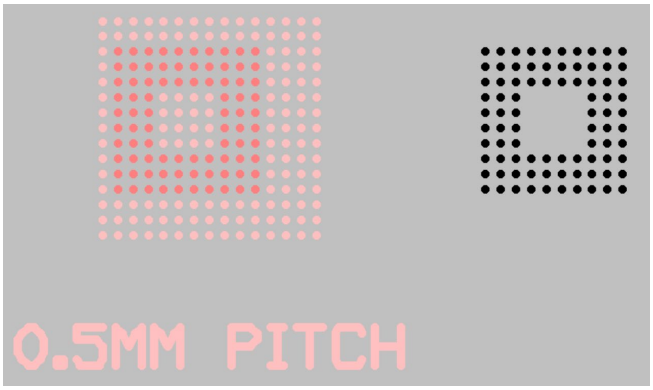

Figure 4. Custom stencil alignment example.

A set of boards containing 0.5mm pitch BGA square array pads on a 15x15 grid was located that could accommodate the overprint test stencil as shown in Figure 4. The 0.5mm pitch BGA footprints on this board used similar feature sizes as the originally tested customer application and it was also observed that the non-solder mask defined pad openings were variable size and registration. With careful screening, this offered a unique opportunity to isolate and investigate the variable of solder mask registration itself on influencing print volume transfer in addition to the original plan to explain the origin of the under printed overprint. Table 1 provides a list of print test variables. Printing on a featureless bare surface with no solder mask was added as a baseline condition.

Table 1. Experiment variables.

Stencil Nano Coating	No, Yes
NSMD Mis-Registration	No Solder Mask, <10µm, 25µm, 75µm

The 3 levels of solder mask mis-registration are shown photographically in Figure 5. This print test only required four circuit boards. Each board representing a unique board topography condition was printed, measured by SPI, cleaned thoroughly, and then printed again in the same routine to obtain a series of repeat solder paste transfer efficiency measurements to characterize the print volume trend.

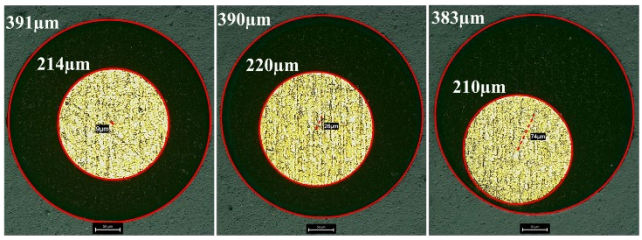

Figure 5. Three non-solder mask defined pad registrations.

It was somewhat surprising to locate a BGA pattern with solder mask so severely offset by 75µm, as referenced in Figure 5, but this was found to be an acceptable result based on the discovery of a clause provided by the PCB manufacturer stating acceptability for the solder mask opening to touch the etch profile of the pad [4]. A word of caution to the PCB designer, unless otherwise specified it may be assumed by the PCB manufacturer to permit solder mask misregistration up to tangency with the pad.

PROCESS SETUP

The key production line equipment utilized to complete this test comprised a fully automatic programmable stencil printing machine and adjacent solder paste inspection machine, both shown in Figure 6.

Figure 6. SMT line equipment used for testing.

Two different printing machine setups were used to complete this experiment, each being tailored to the specific board type being printed. The main difference between printing machine setups is that the bare board print on a featureless gold finish surface used magnetic pin supports with OTT (over the top) board clamping and printed 20 repeats per test. The 3 boards with varied solder mask alignment used dedicated vacuum tooling with foil-less board clamping in the printing machine and printed 10 repeats per test. A list of other print and SPI process parameters are listed in Table 2.

Table 2. Print process parameters.

Stencil Printer	Programmable Fully Automatic SMT Line Machine
Clamping	Bare PCB: OTT Foil, NSMD PCB: Foilless
Tooling	Bare PCB: Pins, NSMD PCB: Dedicated Vacuum
Squeegee	170mm, 60deg, 15mm Overhang Metal Blade
Print Speed	50mm/sec
Separation Speed	3mm/sec
Print Pressure	4.2kg
Underwipe	Not Used
Temp (C)	23.7
Humidity (%)	57
Solder Paste	Std Product, SAC305, NC, Type 4, 88.5% Metal
Paste Bead Load	130g
Stencil	29x29x1.5 Mesh Mount, 100µm Foil, Laser Cut
Stencil Apertures	280µm Circle (0.70 Area Ratio)
Stencil Option	Dual Image: Front Nanocoat, Rear Not Coated
SPI Tool	Programmable Fully Automatic SMT Line Machine
SPI Threshold	30µm

PRINT RESULTS

Boards With Bare Surface

Printing on a solder mask free non-patterned surface represents the ideal stencil gasket print condition and is expected to deliver the optimum paste print volume control. The data plotted in Figure 7 shows all individual paste volume transfer efficiencies across 20 prints for both the non-nano coated stencil and nano coated stencil images. From this view all data looks well controlled, and it is difficult to distinguish differences between the stencil coatings.

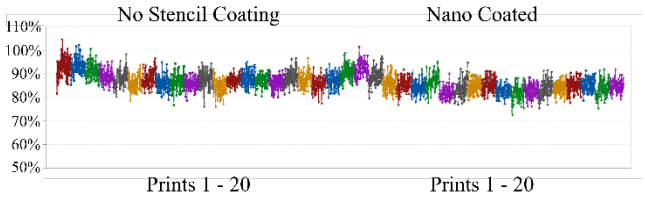

Figure 7. Individual deposit volume transfer efficiencies.

Charting the average paste volume transfer efficiency per print from the same data set results in the plot shown in Figure 8. From this view it is easier to see the nano coated stencil paste transfer trends just slightly lower than the non-nano coated stencil.

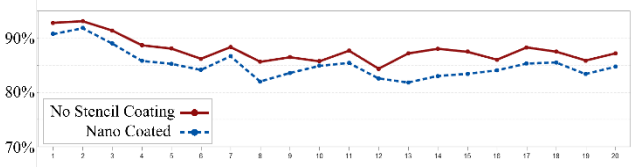

Figure 8. Average deposit volume transfer efficiencies per print.

Charting the standard deviation volume transfer efficiency per print from the same data set results in the plot shown in Figure 9. The nano coating influence is quite absent in this comparison as both stencil images produce very similar results with excellent standard deviation values at around 3%.

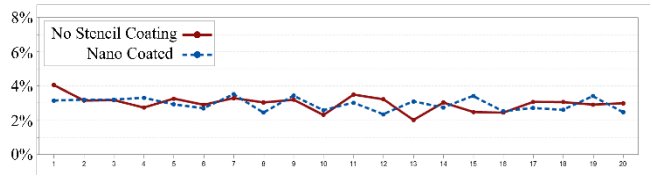

Figure 9. Standard Deviation of deposit volume transfer efficiencies per print.

A visual comparison between printed solder paste deposits from non-nano coated and nano coated stencils is shown in Figure 10. While it is difficult to identify differences in paste transfer, there's compelling visible differences in flux spread. The nano coated stencil contains the flux well within the deposits while the non-nano coated stencil allows flux to pervasively spread and bridge across the whole aperture group. This may explain the slight reduction in print volume transfer efficiency for the nano coated stencil as the solder paste ingredients are better contained within the apertures. The presence of a heavy flux stain on the substrate surface without the stencil nano coating also suggests there is a level of flux residue that is soiling the bottom of the stencil, which may require more frequent stencil under wiping to maintain cleanliness.

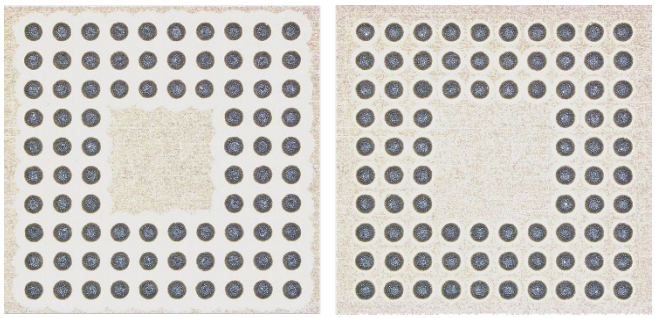

Figure 10. Example prints on bare surfaces, print #20.

Boards With NSMD Pads

Introducing boards with solder mask opening and pad surface topography is expected to produce more scatter in the print volume results compared to the previous bare surface prints as such board features introduce unevenness that have consequences on stencil gasketing. This aspect can be better understood with reference to Figure 11, which models the alignment of a 280µm white circle simulating the overprint aperture and 3 levels of topography, explained as follows. The thickness dimension of the pad (topography level 1) may cause it to intrude somewhat into the stencil aperture hole and this could reduce the capacity of the aperture to hold solder paste particles. The black space between the pad and the aperture wall represents the lowest topographic elevation (topography level 2) which may not actually firmly seal (or gasket) against the stencil since the stencil foil level is flush against the solder mask. The solder mask is the tallest topography level (topography level 3) and is the region outside of the largest red circles in Figure 11. At the largest solder mask misregistration level of 75µm the overprint aperture is expected to directly overlap onto solder mask. This represents a situation of imbalanced stencil gasketing which could contribute to destabilizing print quality, as has been reported elsewhere [5].

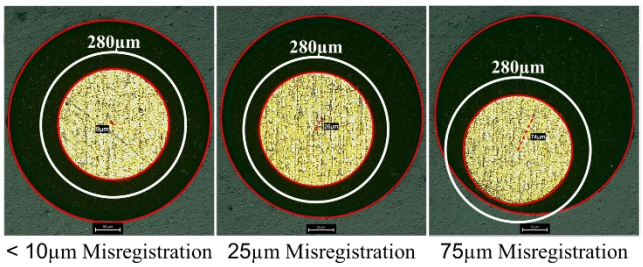

Figure 11. Individual aperture alignment to pad across three non-solder mask defined pad registrations.

The proper alignment of the stencil over the metal pads at the three solder mask opening registration levels is shown in Figure 12. Viewed this way the stencil effectively conceals any of the pad variations that were highlighted in Figure 11 and making these pictures appear quite indistinguishable from one another. The overprint aperture design is clearly apparent as the BGA pads are completely encircled by the larger stencil holes. The thin black regions between the pad and aperture walls are the key locations under scrutiny here to identify any evidence of poor solder particle transfer relating back to the original concern of paste underprint performance observed on the customer test board.

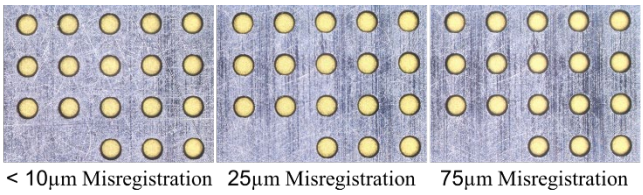

Figure 12. Stencil aperture alignment across three non-solder mask defined pad registrations.

The visual results of print quality across the three non-solder mask defined pad registrations and two stencil coating conditions is shown in Figure 13. From this view the differences in print quality is difficult to detect and all printed pads appear to be well covered with paste particles.

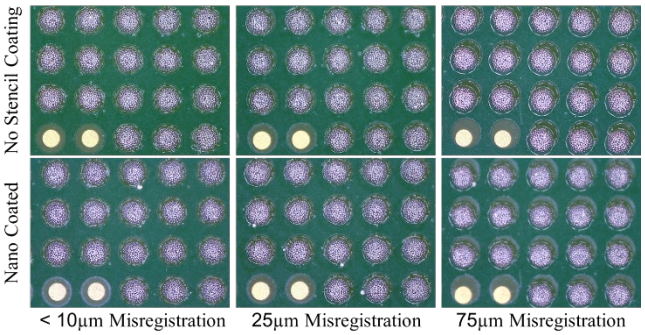

Figure 13. Example prints on three non-solder mask defined pad registrations.

The data plotted in Figure 14 shows all individual paste volume transfer efficiencies across 10 prints comparing the three non-solder mask defined pad registration levels for both the non-nano coated stencil and nano coated stencil images. Compared to the same scatterplot for prints on a bare surface, the topography created by pads and solder mask leads to a wider data scatter in Figure 14. It is interesting that the solder paste volume tends to increase noticeably at the largest solder mask misregistration level, likely caused by the poor stencil gasket condition which allows more paste particles to escape the bounded dimensions of the aperture holes. Like the previous comparison, solder paste transfer differences between the stencil coating conditions in this view are not obvious.

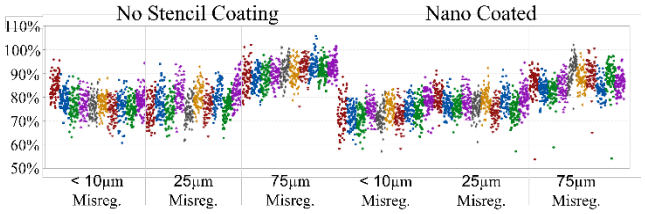

Figure 14. Individual deposit volume transfer efficiencies.

Charting the average paste volume transfer efficiency per print from the same data set results in the plot shown in Figure 15. From this view it is more apparent that a poorer stencil gasket from misaligned solder mask permits a larger volume print. But again, here it is difficult to identify a consistent trend for realizing a print transfer improvement attributed to the presence or absence of a stencil nano coating.

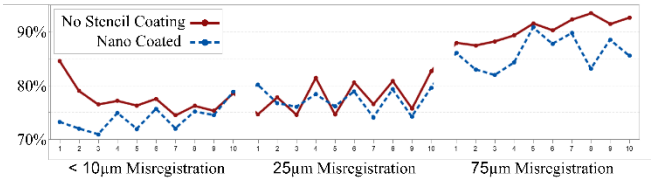

Figure 15. Average deposit volume transfer efficiencies per print.

Charting the standard deviation volume transfer efficiency per print from the same data set results in the plot shown in Figure 16. Surprisingly, the level of solder mask opening misregistration does not negatively shift the print volume scatter trend as was expected. The nano coating also does not appear to strongly influence print scatter, except in the case of the middle level solder mask opening misregistration of 25µm where the stencil nano coating is consistently demonstrating a slightly more positive effect. Upon further review of test variable insensitivities, there are two things that may explain that outcome. Firstly, the limited number of prints conducted may not have exercised the print process enough to expose degrading stencil gasket conditions that lead to changes in print volume transfer efficiency. Secondly, this just may be an unlucky scenario where the selected boards do not present a large enough level of board topography in the copper and solder mask layers to negatively impact the stencil gasket condition severely enough.

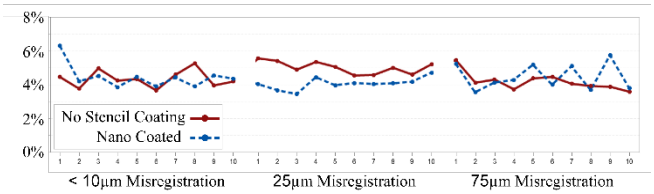

Figure 16. Standard Deviation of deposit volume transfer efficiencies per print.

CONCLUSIONS

Based on the series of simple print tests conducted here, an aperture designed at 0.7 area ratio has been demonstrated to achieve an average print volume transfer efficiency level of 85% at a standard deviation level of 3% on a bare featureless substrate. This test condition offers the greatest opportunity to achieve the best possible print results. When including proper board topography using the same stencil apertures to overprint 0.5mm pitch BGA non-solder mask defined pads, a similar level of print volume transfer efficiency performance was achieved, but with more scatter in the volume distribution (i.e. larger standard deviations). The largest misregistration of solder mask openings was found to raise the printed average volume transfer as expected, but without widening the print scatter. It is recognized that making a general conclusion on stability of print scatter under this severe level of solder mask misalignment is ignorant without due consideration to influences of outer layer copper thickness and solder mask thickness variables that were not specifically measured and tested in this work. Although the influence of a stencil nano coating in this test was not strongly detected to affect print quality, the overwhelming positive track record attached to using stencils with a nano coating warrant recommending its application to all solder paste printing stencils.

FUTURE WORK

The test that was conducted here failed to re-create the customer application result referenced in Figure 2, where a restricted paste volume and higher volume scatter was observed. Future work will build on the knowledge gained from this test and employ the use of the same stencil to explore print quality trends on other candidate boards that have:

- Heavier outer layer copper (thicker pads)
- Inclusion of surface traces
- Thicker solder mask
- Tighter solder mask opening to pad

Investigation of solder paste particle clustering and adhesion on the stencil aperture walls during and after print testing can also be added to support documenting key visual clues to help characterize paste transfer behavior.

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REFERENCES
[1] Stencil Design Task Group 5-21E, "Stencil Design Guidelines", *IPC-7525C*, IPC International, Inc., November 2021.

[2] H. Zhou, R. Aranda, I. Daguio, J. Chen, J. Huang, "The Impact of Component Warping to Assembly Process Resulting to Head In Pillow and Non Wet Open Defects", *iNEMI Workshop on Board Assembly & Test Technology*, Shenzhen, China, August 2014.

[3] Ball Grid Array Task Group 5-21F, "Design and Assembly Process Implementation of BGAs", *IPC-7095D*, IPC International, Inc., June 2018.

[4] M. Kastelic, "Design Rules & Capabilities", AT&S Austria Technologie & Systemtechnik Aktiengesellschaft Presentation, Loeben, Austria, April 2018.

[5] J. Chow, H. McCormick, C. Hamilton, M. Berry, R. Cortero, G. Facchini, "DFM Rules for Smartphones: An Analysis of Yield on Extremely Dense Assemblies", *Proceedings of IPC APEX Expo*, San Diego, CA, USA, February 2012.