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Innovative Panel Plating for Heterogeneous Integration

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Abstract
The migration to large panel substrates in advanced packaging applications is principally motivated by cost considerations. However, it is occurring at a time when package processing is becoming more complex and demanding. New package architectures featuring heterogeneous integration (HI), such as Intel's EMIB, TSMC's INFO, and many others, present challenging new requirements in the fabrication process. With feature sizes less than 10 microns, increasing number of patterned layers, and vias between layers, these demanding process steps must be realized on wafer and panel substrates alike.

The traditional equipment set for large panel substrates typically uses bulk processing and is not designed for wafer-like process requirements. Thus, a new class of process tool is required to bridge this technology gap, maintaining the economy of scale of large panel tools while meeting the requirements of current and future package architectures. For electroplating process steps, a vertical tool architecture running a single panel per process cell makes it possible to directly apply advanced wafer plating technology to panel substrates.

Individual panels are loaded in a rigid holder to minimize warpage and provide the large currents necessary for plating large areas. An overhead transport conveys the loaded panels to a series of cells which carry out the necessary steps in the deposition process. The initial step is a vacuum prewet, which prevents the occurrence of air bubbles in deep features when the panel is introduced into a plating bath. A series of plating cells allows a stack of different metals to be deposited in a single pass through the tool. Each cell is customized for a particular metal and, with features such as multiple anode zones and pattern-specific shields, can be customized for each device. Efficient agitation is also adapted from wafer plating tools to provide the fastest and best quality deposition processes.

This paper will show that the improvements in feature density, deposition uniformity and void free via filling that are required for heterogeneous integration can be achieved in large panel processing, providing the desired cost reduction relative to wafer processing for interposers and other package structures.

Introduction
Historically, microelectronics has progressed by incorporating more functions on a single chip. The ability to do this by shrinking CMOS transistor dimensions has made this the preferred method for achieving higher levels of integration for many years. However, the expectation of faster clock speeds and lower cost per function with each shrink in minimum feature size may have reached a limit at the 7-nanometer node.

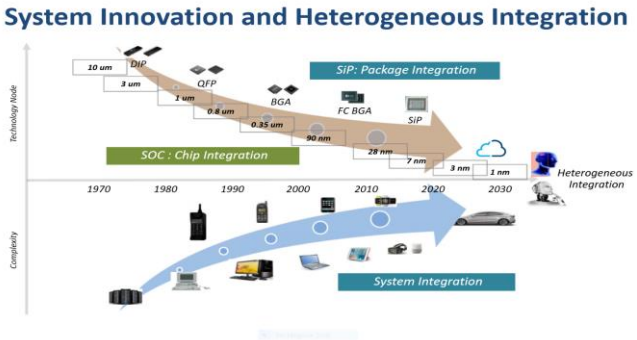

Figure 1. IEEE Roadmap for Heterogeneous Integration

Heterogeneous integration, or the incorporation of multiple chips (which may be manufactured with different technologies) in a single package, is an alternative method for continuing the progress in system speed and integration. Packaging multiple chips together in a single package has always been an available option, but to satisfy the needs of current systems, the package must now incorporate a high density of signal connections among the different chips. Some of the package

architectures for achieving this, including TSMC's INFO (Integrated Fan-Out), are illustrated in Figures 1 and 2 [1]. Intel has developed a package architecture called EMIB, using a silicon embedded bridge, shown in Figure 3.

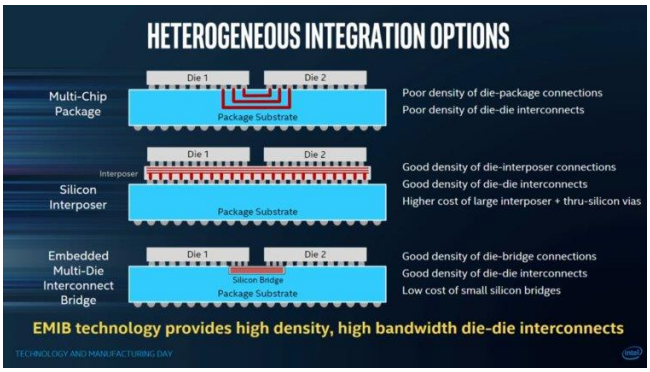

Figure 2. Options for Heterogeneous Integration

All of the proposed heterogeneous integration architectures require considerably more patterned layers, finer features, and different substrates compared with traditional IC packaging. For several years much of this processing has been done using non-silicon substrates, of the same size and thickness as standard Si wafers, in order to make use of wafer-based process equipment. While this can reduce the materials cost somewhat, considerably greater cost savings can be achieved by performing these manufacturing processes on large rectangular panels. Process equipment for such large substrates exists, for PC board, flat panel display and other manufacturing. However, such tools are typically not clean room compatible, or capable of carrying out processes to the demanding specifications of wafer processing. A new class of process tools is required in order to meet the ever more challenging requirements of advanced packaging fabrication, and to do this on large panel substrates. This paper will review a new panel plating tool designed for these process requirements. This tool is capable of depositing metal in features down to 2 microns in width, with deposition uniformity better than 5% across the panel surface.

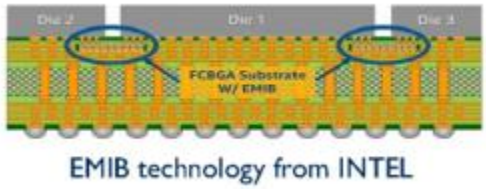

Figure 3. Intel's Embedded-Die Multi Interconnect Bridge (EMIB)

Substrate materials and structures for advanced packaging

For interposers and other substrates used in advanced packaging, silicon wafers offer the advantage of an existing set of tools and processes. However, they are an expensive choice, and some processes (such as through-substrate via formation) are particularly expensive and time-consuming. For advanced packaging applications, many manufacturers have turned to materials other than silicon, such as molding compounds or other polymers, but maintaining the form factor of standard silicon wafers. These substrates, while offering cost advantages, introduce new problems such as outgassing and deformation, which pose challenges to processing.

Ultimately, the reduction in manufacturing cost required to maintain the "Moore's law" progress in electronic devices requires a substrate larger than a 300mm wafer. Increasing silicon wafers to 450mm diameter has been discussed but has not been realized in manufacturing. And, since the substrate material need not be silicon, the substrate size does not have to be restricted to the attainable diameter of silicon boules.

Roadmaps for advanced packaging point to increasing package sizes, to allow more functions to be performed within the package. As interposer sizes become larger, with sizes up to 100mm being discussed for some 5G applications, it becomes increasingly inefficient to manufacture them in a 300mm wafer format.

In parallel with the development of process technology on wafers, a mature set of tools and processes has been developed for printed circuit board manufacturing. Processing of PC board substrates is much more cost-effective than silicon wafers. However, the existing technology is limited in interconnect density and speed, as illustrated in Figure 1. Linewidths as small

as 10 microns can be achieved, while linewidths of 2 microns and smaller are needed for advanced packaging (Figure 4) [2].

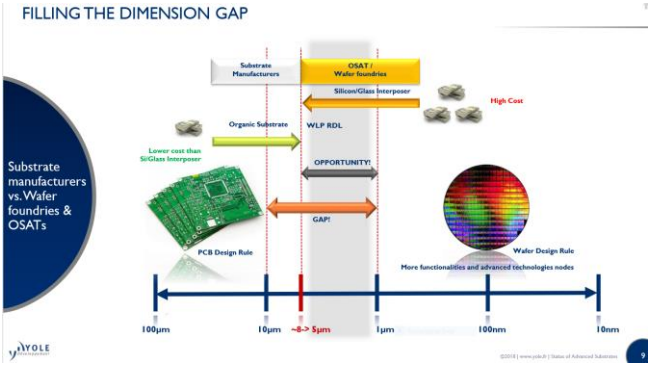

Figure 4. Bridging the linewidth gap

Intel's EMIB architecture is one approach to bridging the gap. PCB manufacturers have also developed approaches to achieving higher interconnect density using semi-additive processes (SAP) and substrate-like PCB (SLP) architectures as seen in Figures 5 and 6 [3]. These processes still have compatibility issues with standard PC board fabrication, such as alignment and thermal expansion matching, and introduce additional costs which offset the benefits of using PCB substrates.

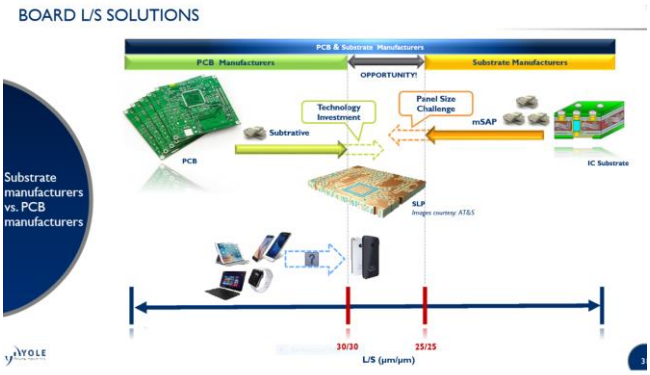

Figure 5. PC board approaches to bridging the linewidth gap

Figure 6. Substrate-like PCB (SLP) structure

Process tools: the best of both worlds

In order to fully realize the cost benefits of large PCB substrates in advanced packaging, a new set of process tools is needed, which can adapt the more demanding, smaller linewidth processes (such as INFO and other fanout architectures) from wafers to the larger panel format. Such tools must be cleanroom compatible and include the process controls needed to meet the requirements of 2 micron and smaller interconnects. The needed improvements are shown in Figure 7 [4].

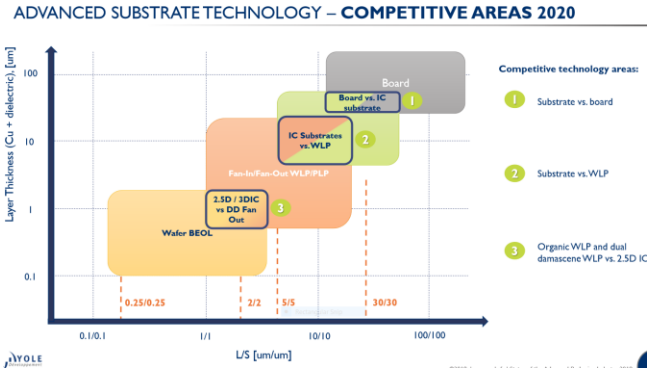

Figure 7. Bridging the gap with process technologies

Vertical single-panel plating

One of the critical process steps which must be addressed in this tool set is electrochemical deposition (ECD), or electroplating. Some of the key process specifications which must be transferred from wafers to panels include deposition uniformity, substrate throughput, and flexibility for depositing multiple metal stacks. Bulk plating, which is used in traditional PCB manufacturing, is not well suited to meeting these specifications.

A new panel plating tool, shown in Figure 8, was designed to address the needs of advanced packaging on a panel substrate. In place of bulk processing, the tool was designed with a compact series of cells which process a single panel at a time. Using a vertical orientation in the plating cell allows high throughput in a small footprint and, just as important, enables the inclusion of a set of features which are required for advanced packaging plating applications. The large number of cells, and an optimized overhead transport system, allow flexible processing with different metals, and a throughput of up to 60 panels per hour. The panels are gripped in a rigid holder during transport and processing, minimizing any issues arising from panel warpage.

Figure 8. Panel plating tool configuration showing the series of vertical process cells

The following sections describe the features which allow the panel tool to carry out wafer-like processes, including features developed especially for the panel application.

Shear plate agitation

Deposition of metal from a bulk solution involves the transport of metal ions across a hydrodynamic boundary layer at the active surface. The effective thickness and uniformity of this boundary layer is a critical factor in the deposition rate and the quality of the deposit. The vertical cell architecture of the panel plating tool allows the direct application of shear plate agitation used in wafer plating tools. This style of agitation uses a reciprocating grating (Figure 9) in close proximity to the panel, to generate turbulence at the surface and maximize transport efficiency of metal ions and other critical reactants.

Vacuum prewet

When the part to be plated includes deep or high aspect ratio features, it is possible for air bubbles to become trapped in the feature when it is inserted into the plating bath. These air bubbles, held in place by surface tension, can delay or event prevent plating from occurring in those features by preventing the plating solution from making contact with the active surface. The most effective method for eliminating air bubbles is to bring the part under vacuum, and fill the chamber with degassed, deionized water (Figure 10). With no air present, the water fills all of the recesses, and now surface tension acts to exclude air as the part is transported to the plating cell.

This feature is particularly critical for deep vias, as shown in Figure 11.

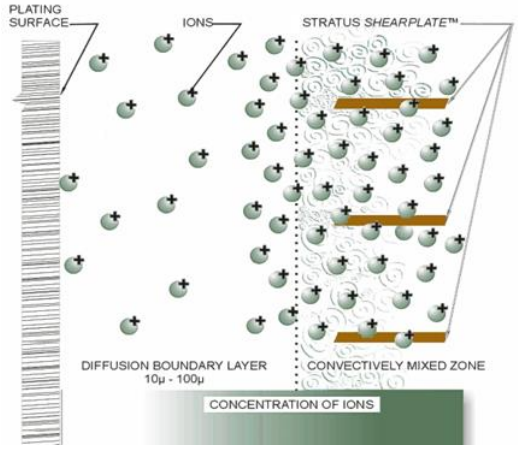

Figure 9. Shear plate agitation to minimize boundary layer thickness

Figure 10 Vacuum prewet module in panel plating tool

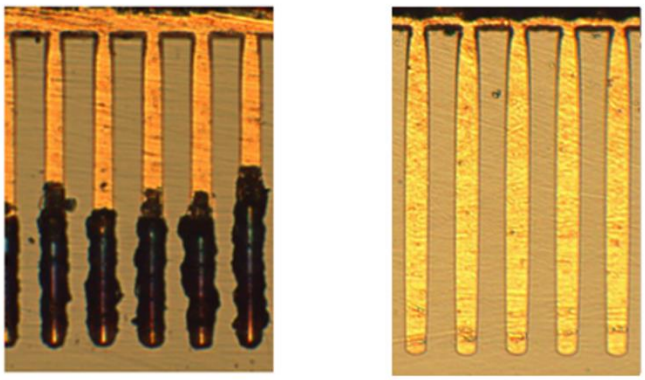

Figure 11. The impact of prewet on filling 10 x 100 micron vias: no prewet (left), vacuum prewet (right)

Membrane cell

For advanced packaging applications, many of today's plating chemistries require the presence of ion-exchange membranes in the plating cell. These membranes separate the fluid volume into a region in contact with the anode, and a region in contact with the panel. One motivation for this separation is to reduce the cost of the organic additives in the plating bath, which are broken down over time by contact with the anode. Another is to maintain precise control over the bath constituents.

Membrane cells are implemented in the vertical panel tool. This allows the use of the widest range of available plating chemistries, including some which are formulated for controlled, flat and uniform plating on patterns that include features of different shapes and densities (Figure 12). The ability to run these chemistries is critical, for example, in patterns including multiple redistribution layers and vias between layers, where the plated RDL feature must be planar over the via.

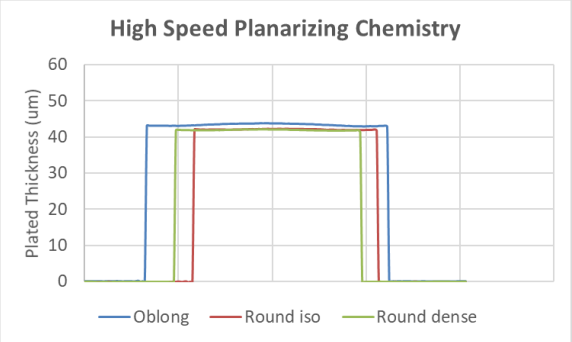

Figure 12. Profiles of plated features of different density and shape

Multizone anode

Electroplating requires a thin seed layer of Cu or Au on the substrate to carry the current to the edge contacts as metal ions are deposited. Since the seed layer is necessarily very thin, the sheet resistance to this current can result in potential variations across the substrate which can affect the deposition uniformity. This is called the "terminal effect". This is a more critical issue for panels than for wafers, since larger surfaces and currents are involved.

As interconnect linewidths become smaller, there will be a corresponding reduction in the thickness of the seed layer that is used for plating. This is because plating is followed by photoresist strip, and then a wet etch of the seed layer. The wet etch can introduce an undercut of the plated features, which is controlled by scaling the seed layer thickness with the linewidth. This has the side effect of increasing the sheet resistance. The impact of the terminal effect on uniformity is illustrated in Figure 13.

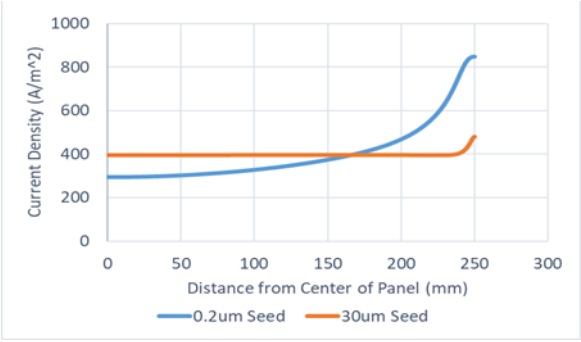

Figure 13. Simulation of terminal effect for different seed layer thicknesses

For the panel tool, a multizone anode (Figure 14) is used to compensate for the potential variation induced by the current through the seed layer. Since contact is made on the left and right sides of the panel, the primary variation to be dealt with is in the horizontal direction. The variation in current supply across the panel is adjusted to compensate for the potential drop through the seed layer. Uniformity across the panel of better than 5% has been demonstrated for Cu and Ni plating.

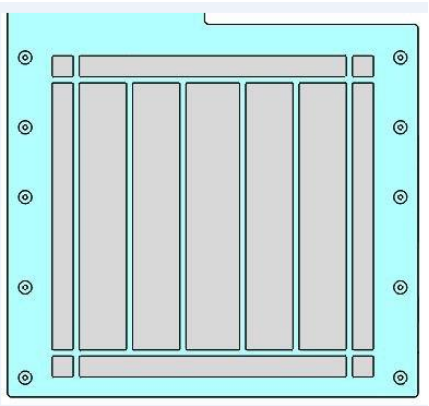

Figure 14. Multizone anode used for panel plating

Proximity shield

As mentioned above, interposer sizes for some package designs have become fairly large. The patterns to be plated on these interposers can often include wide local variations in feature density, which can be another challenge for deposition uniformity. This a different nonuniformity mechanism from the terminal effect, and must be dealt with differently. A proximity shield methodology has been developed for the panel tool. This uses a plate in close proximity with the shear plate, with openings that correlate with the variations in pattern density on the panel itself. Significant improvements in coplanarity, or the deposition uniformity within a die, have been achieved using this feature.

Conclusion

As traditional monolithic integration is being replaced by heterogeneous integration in electronic packaging, both silicon interposers and printed circuit boards (PCBs) are being considered. Silicon interposers exist today but are expensive (35- 40 cents per cm^2 per layer). PCBs are less expensive but do not quite have the technology for the required interconnect density. We have demonstrated how a wafer plating tool can be reinvented to plate panels while achieving high density circuitry to reduce the costs and obtain unparalleled plating uniformity.

Acknowledgements

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