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Impact of PCB Manufacturing, Design, and Material to PCB Warpage

A. Caputo[2], S.R. Aravamudhan[2], H. Fu[1], N. Hubble[3], C. Olson[3], M. Huang[4], A. Hsieh[4], J.W. Cai[5], Y. Li[5], D. Li[5], P. Vernhes[6], B. Feit[6], P.L. Toussaint[6], CC. Chang[7], L.L. Qin[7], C.Y. Hsu[7], C. Lin[8]

[1]iNEMI, [2]Intel Corporation, [3]Akrometrix, [4]Wistron Corporation, [5]Shengyi Technology, [6]Insidix, [7]Unimicron, [8]HannStar Board Corporation
antonio.caputo@intel.com

Abstract
Customer demands for smaller form factor electronic devices are driving the use of thinner electronic components and thinner printed circuit boards (PCB) in the assembly process. The use of thinner components and thinner multi-up panel PCBs (≤ 1 mm) has led to PCB warpage issues in the surface mount (SMT) assembly process, which in turn impacts the PCB assembly yield. PCBs with excessive warpage impact paste print quality in the print process, and solder joint formation during reflow soldering leading to SMT assembly defects. Lack of industry standard for PCB warpage at reflow temperature further compounds the PCB warpage risk to SMT assembly yield. This paper will use high temperature warpage metrology to evaluate the impact that PCB manufacturing, design, and material has on ball grid arrays (BGA) and panel area PCB warpage by varying the PCB post processing (Bake vs. No-Bake), panel location (corner vs. center), PCB thickness (0.8 mm vs. 0.6 mm), Material (Mid T_g vs. High T_g), and processing (i.e. lamination at condition A vs. B).

1.0 Introduction

The current trend in the electronic industry for finer pitches and smaller form factors is driving smaller components and thinner PCBs [1-3]. The current trend in PCB technology is to develop lower CTE materials with high glass transition temperature (T_g). This results in added expansion and contraction between dielectric and copper layers, and hence greater PCB warpage [4]. The warpage creates potential reliability risks during the SMT process when the PCB experiences peak SAC soldering temperatures in excess of 240 °C, and hence potential solder joint reliability issues. Design is one way to control PCB warpage. PCB material, thickness, post manufacturing bake, and supplier can also influence PCB warpage. To the best of the authors knowledge, very little work has been published evaluating the impact of PCB fabrication on PCB warpage. More work needs to be done. The project was evaluated in three phases: Phase 1 DOE: Metrology matching study. Phase 2 DOE: The effect of post PCB manufacturing bake on PCB warpage (i.e. Legs 1 & 2). Phase 3 DOE: The effect of PCB manufacturing, thickness, and material on PCB warpage.

2.0 Experimental Set-up

The manufacturing panel was ~620 mm x ~460 mm and consisted of eight shipping panels with each shipping panel having a dimension of ~79 mm x ~64 mm. In Figure 1, shipping panels 1, 2, 7, & 8 are corner panels, while locations 3 – 6 are center panels.

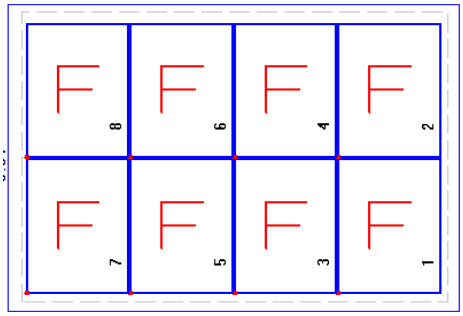

Figure 1: PCB manufacturing panel layout

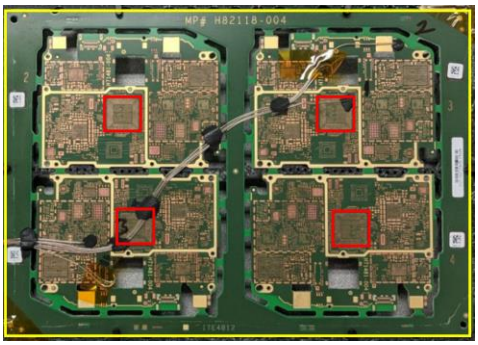

Figure 2: Example of one shipping panel

Figure 2 is an example of one 4-up shipping panel where the yellow outline represents the warpage area measurement for the shipping panel, while the 4 red boxes represent the local BGA warpage area measurements (i.e. ~13 mm x 13 mm) per shipping panel.

2.1 PCB design and stack up

A single 10 layer PCB design with less than 10% copper balance across layers and solid outriggers was used in this work. PCBs with 2 different stack-ups were constructed to vary the PCB thicknesses (i.e. 0.6 mm & 0.8 mm). Refer to Table 1, and Figure 3 respectively.

Table 1 - Summary of Copper Densities

≤ 10% Copper Balance, Solid Outrigger Copper Balance		
Layer	**Percent Layer Copper Density**	**Percent Outrigger Copper Density**
1	72.9	≥ 95
2	84.4	≥ 95
3	89.2	≥ 95
4	73.1	≥ 95
5	77.9	≥ 95
6	77.3	≥ 95
7	74.1	≥ 95
8	82.9	≥ 95
9	86.1	≥ 95
10	82.6	≥ 95

		thickness (um)
S/M		15
L1	1/3oz+plating	25
prepreg	PP1037	40
L2	1/3oz+plating	15
prepreg	PP1037	40
L3	1/3oz+plating	15
prepreg	PP1037	40
L4	1/3oz+plating	15
prepreg	PP1037	50
L5	1/3oz+plating	15
Core	2.6mil	65
L6	1/3oz+plating	15
prepreg	PP1037	50
L7	1/3oz+plating	15
prepreg	PP1037	40
L8	1/3oz+plating	15
prepreg	PP1037	40
L9	1/3oz+plating	15
prepreg	PP1037	40
L10	1/3oz+plating	25
S/M		15
	overall board thickness	605

(a)

		thickness (um)
S/M	SolderMask	40
L1	Copper(Base+Plating)	30
prepreg	Prepreg/1-1067	55
L2	Copper(Base+Plating)	25
prepreg	Prepreg/1-1067	55
L3	Copper(Base+Plating)	25
prepreg	Prepreg/1-1067	55
L4	Copper(Base+Plating)	25
prepreg	Prepreg/1-1067	55
L5	Copper(Base+Plating)	25
Core	Core	60
L6	Copper(Base+Plating)	25
prepreg	Prepreg/1-1067	55
L7	Copper(Base+Plating)	25
prepreg	Prepreg/1-1067	55
L8	Copper(Base+Plating)	25
prepreg	Prepreg/1-1067	55
L9	Copper(Base+Plating)	25
prepreg	Prepreg/1-1067	55
L10	Copper(Base+Plating)	30
S/M	SolderMask	40
	overall board thickness	840

(b)

Figure 3: Stack up for (a) 0.6 mm, and (b) 0.8 mm thick PCBs

2.2 Design of Experiments (DOE) Set Up

The DOE was a two level experiment that evaluated multiple factorial conditions as outlined in Table 2. The panel dimension was not varied in this work. The partial factorial DOE legs are summarized in Table 3.

Table 2 – Summary of DOE Factorial Conditions

DOE Factors	**Level 1**	**Level 2**
PCB fabrication house	Supplier A	Supplier B
PCB fabrication process	Condition A	Condition B
PCB location within manufacturing panel	Center	Corner
PCB thickness	0.6mm	0.8mm
PCB material	Mid Tg	High Tg
Post processing	Yes	No

Table 3 – Summary of DOE Legs

DOE Leg	PCB Fabrication Process	PCB Material	PCB Thickness (mm)	Post Processing
1	Condition A	Mid. Tg	0.8	No
2	Condition A	Mid. Tg	0.8	Yes
3	Condition B	Mid. Tg	0.8	No
5	Condition A	High Tg	0.8	No
7	Condition B	High Tg	0.8	No
9	Condition A	Mid. Tg	0.6	No
11	Condition B	Mid. Tg	0.6	No
13	Condition A	High Tg	0.6	No
15	Condition B	High Tg	0.6	No

For legs 1 & 2, the post processing bake was 150 °C on the shipping panel. The press/lamination conditions A & B for each PCB supplier are summarized in Table 4.

For the sample size, 12 shipping panels were used in order to achieve an 80% confidence level, 50 µm technical coplanarity delta, and 85% power. The PCB location within the manufacturing panel (corners and centers) were captured in the DOE.

Table 4 – Summary of Press/Lamination Conditions

Attribute	**PCB Supplier A**				**PCB Supplier B**	
	Condition A		**Condition B**		**Condition A**	**Condition B**
	Mid. Tg	**High Tg**	**Mid.Tg**	**High Tg**	**Mid. Tg & High Tg**	**Mid. Tg & High Tg**
Lamination Temp. (curing) °C	>170	>190	>170	>190	170	175
Heating Rate (°C/min)	1.77	2.85	1.43	2.28	1.58 (inner layer) 1.62 (outer layer)	2.4
Cold Press Time (minutes)	40	40	70	70	40	70
Cure Time (minutes)	77	110	103	122	96	70

2.3 Metrology Matching Study

A high temperature measurement warpage metrology was used to characterize PCB warpage. The absolute warpage value was used to represent the PCB warpage or coplanarity in this study. In order to ensure that the PCB warpage measurements across all sites were technically equivalent, a metrology match study was performed across four sites. The test sites are designated B, C, D & E.

The metrology matching study was divided into the following parts:

1. Step Block for Accuracy evaluation at room temperature
   - Precision machined steel block with steps of ~25 µm, ~140 µm, and ~265 µm for linearity check in accuracy measurements was used
   - The block was ISO certified by third party
   - Test site C provided the step block for this matching study

2. Lens for thermal repeatability
   - Optical flat lens from fused silica with known radius of curvature
   - 16 measurements at Room Temp, 150 C & 250 C using J-STD-020 peak reflow temperature specification called out in IPC 9641 specification (section 5.4 and section 6)
   - A flat surface was ensured at the edge of lens

3. Thermal performance comparison

a. Compare thermal performance of the various tools following J-STD-020 peak reflow temperature specification
b. PCB with thermocouples were attached and measurements were performed by external data logger
c. Maintained a lower reflow max temp to avoid degradation

It should be noted that realistic grating or field of view (FOV) settings was used for tests 1 & 2 above. The success criteria for each part of the matching study is summarized in Table 5.

Table 5 – Matching Study Success Criteria

Part	Metrology Matching Tests	Success Criteria
1	Step Block for Accuracy evaluation at room temperature	± 2% from target value
2	Lens for thermal repeatability	± 5% from target value
3	Thermal performance comparison	Technical equivalency

3.0 Results

3.1 Phase 1: Metrology Matching Study

The matching study results are summarized in Tables 6, 7, & 8. For the lens thermal repeatability study, sites B & C used an optical flat lens from manufacturer M, while sites D & E used a lens from Manufacturer N. It must be noted that for the step 1 measurements for sites D & E, the small area right next to the step was ignored because it impacted the measurement, hence this is why site D fell out of range for step 1, but still met the matching study criteria and was included as a test site in this DOE.

Table 6 – Results Summary of Step Block Matching results

Block Step Heights	Success Criteria	Site B (µm)	Site C (µm)	Site D (µm)	Site E(µm)
Step 1 (24.384 µm)	±2% (23.9 µm – 24.9 µm) or Tool Resolution (± 5 µm)	Mean: 23.0 STDEV: 0	Mean: 24.2 STDEV: 0.05	*Mean: 21.9 STDEV: 0.62	*Mean: 23.6 STDEV: 0.07
Step 2 (139.192 µm)	±2% (136.4 µm – 142.0 µm) or Tool Resolution (± 5 µm)	Mean: 136.3 STDEV: 7.32	Mean: 138.5 STDEV: 0	Mean: 139.5 STDEV: 1.27	Mean: 139.0 STDEV: 0
Step 3 (265.43 µm)	±2% (260.1 µm – 270.7 µm) or Tool Resolution (± 5 µm)	Mean: 258.6 STDEV: 0.51	Mean: 264.6 STDEV: 0.05	Mean: 266.8 STDEV: 0.92	Mean: 267.0 STDEV: 0

* **Step 1 measurements from sites D & E, small area right next to the step was ignored because it impacted the measurement**

Table 7 – Results Summary of Lens Thermal Repeatability

Temperature (°C)	Success Criteria	Optical Lens – Manufacturer M		Optical Lens – Manufacturer N	
		Site B (µm)	Site C (µm)	Site D (µm)	Site E (µm)
24	±5% from Target Optical Lens M Target 372.8 to 388.0um, Optical Lens N Target 671.3 to 698.7um	Mean: 398.69 STDEV: 2.57, CV = 0.006	Mean: 381.03 STDEV: 0.52, CV = 0.001	Mean: 686.0 STDEV: 0.62, CV = 0.001	Mean: 684.94 STDEV: 0.77, CV = 0.001
150		Mean: 398.38 STDEV: 4.41, CV = 0.011	Mean: 380.93 STDEV: 0.80, CV = 0.002	Mean: 685.0 STDEV: 3.5, CV = 0.005	Mean: 683.88 STDEV: 1.63, CV = 0.002
250		Mean: 397.13 STDEV: 1.02, CV = 0.003	Mean: 380.93 STDEV: 1.13, CV = 0.003	Mean: 686.0 STDEV: 4.4, CV = 0.006	Mean: 682.0 STDEV: 1.5, CV = 0.002

Table 8 – Results Summary of Lens Thermal Accuracy

Temperature (°C)	Success Criteria (°C)	Delta Temperature (°C)				
		Reflow Oven	Site B	Site C	Site D	Site E
24	≤ 10 ºC	0.33	0.44	2.00	0.30	1.20
150	≤ 10 ºC	6.67	17.96	7.40	6.50	4.70
200	≤ 10 ºC	4.61	15.78	7.40	4.20	4.60
Peak^{++}	≤ 10 ºC	3.34	12.10	6.40	4.40	4.20
Time to 220 (sec)	NA	152	245	336	400	404

Based on the metrology matching study, all sites except site B met the success criteria, thus testing at site B was not performed in this study.

3.2 Phase 2 DOE: Impact of post PCB fabrication processing – Bake vs. No Bake on BGA and Panel Warpage

The Phase 2 DOE evaluated the impact of post processing bake on PCB warpage. In this portion of the DOE, the press/lamination cycle, PCB thickness and material were held constant. For leg 2 the PCB shipping panel was exposed to a post processing bake – refer to Table 9. Testing was only performed at sites C and E for both Legs 1 & 2. Test Site C measured ~12 shipping panels for both vendors A & B. Due to time constraints, test site E only measured 8 shipping panels for vendor A.

Table 9 – Summary of Phase 2 DOE Parameters

DOE Leg	PCB Fabrication Process	PCB Material	PCB Thickness (mm)	Post Processing
1	Condition A	Mid. Tg	0.8	No
2*	Condition A	Mid. Tg	0.8	Yes

*Post processing bake was 150 °C on the shipping panel

3.2.1 BGA Coplanarity at 240 °C

For the BGA area coplanarity it was found that post processing had very little effect on the BGA coplanarity. Figure 4 shows that although the data is statistically different, it is technically equivalent since the standard deviation is less than 5 µm, which is well within the 3-sigma noise of the tool resolution. Figure 5 shows that there is no impact on shipping panel location within the manufacturing panel (i.e. centers vs. corner locations are statistically equivalent). The key takeaway is that post processing during the PCB fabrication process has little impact on BGA coplanarity.

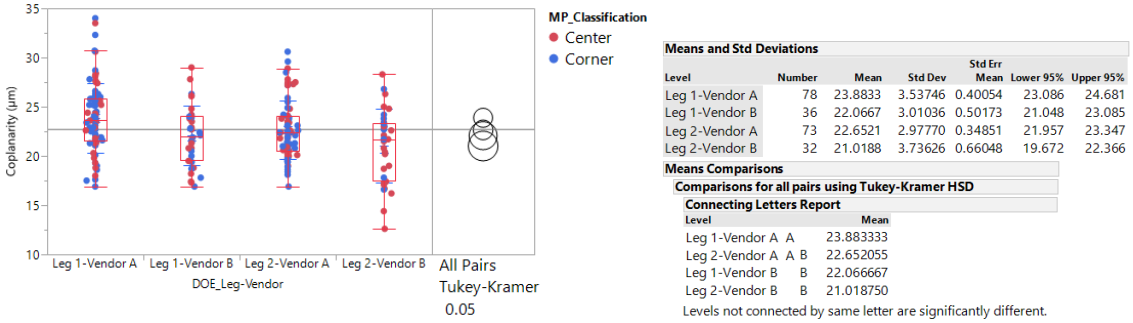

Figure 4: BGA area coplanarity for an area of ~13 mm x ~13 mm vs. DOE leg and vendor.

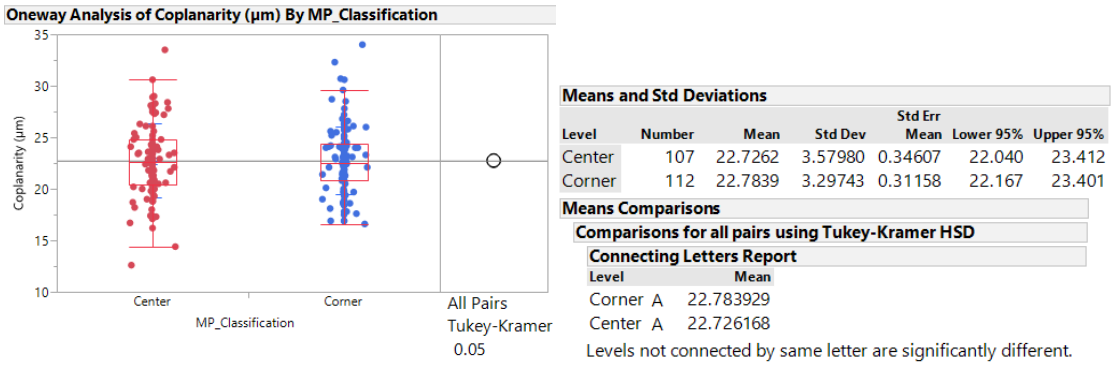

Figure 5: BGA coplanarity vs. the shipping panel location within the manufacturing panel is statistically equivalent

3.2.2 Panel Area Coplanarity at 240 °C

For the shipping panel, it was also found that post processing had very little effect on the coplanarity. Figure 6 shows that the data is statistically equivalent. Figure 7 shows that there is no impact on shipping location within the manufacturing panel (i.e. centers vs. corner locations are statistically equivalent). The key takeaway is that post processing during the PCB fabrication process has little impact on panel area warpage.

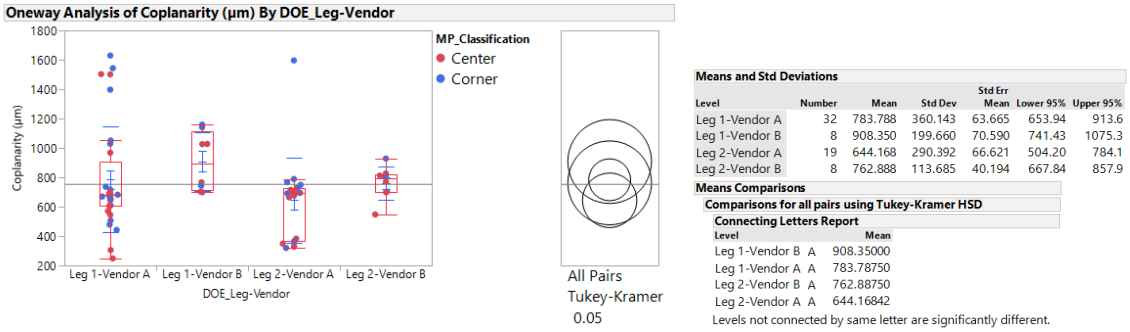

Figure 6: Shipping panel coplanarity versus DOE leg and vendor

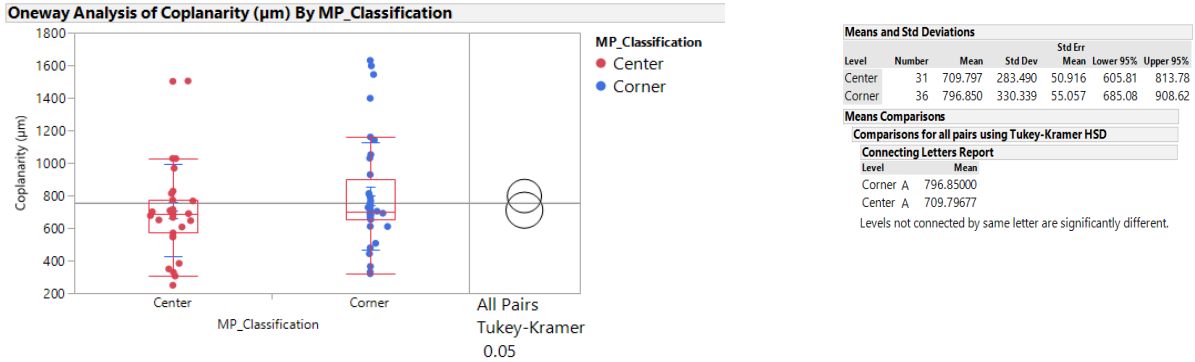

Figure 7: Panel area coplanarity vs. the shipping panel location within the manufacturing panel

3.3 Phase 3 DOE: Impact of PCB Processing, Material, and Thickness

The Phase 3 DOE test parameters are summarized in Table 10. Testing was performed across test sites C, D, & E. Due to lab capacity constraints, each test site measured ~5 shipping panels for each DOE leg. For the purposes of this section, since shipping panel location within the manufacturing panel was statistically equivalent for both BGA and panel area coplanarity, this will not be discussed.

Table 10 – Summary of Phase 2 DOE Parameters

DOE Leg	PCB Fabrication Process	PCB Material	PCB Thickness (mm)	Post Processing
3	Condition B	Mid. Tg	0.8	No
5	Condition A	High Tg	0.8	No
7	Condition B	High Tg	0.8	No
9	Condition A	Mid. Tg	0.6	No
11	Condition B	Mid. Tg	0.6	No
13	Condition A	High Tg	0.6	No
15	Condition B	High Tg	0.6	No

3.3.1 BGA Coplanarity at 240 °C

Figure 8 shows that more variability is observed in the BGA coplanarity for vendor A (i.e. based on the connection letter report highlighted in red for 0.6 mm vs. 0.8 mm thick PCBs), but although the coplanarity is statistically different between vendors, it is technically equivalent (i.e. falls within ~3-sigma). For vendor B, the coplanarity is statistically equivalent across all legs, and minimal variability between 0.6. mm vs. 0.8 mm thick PCBs is observed.

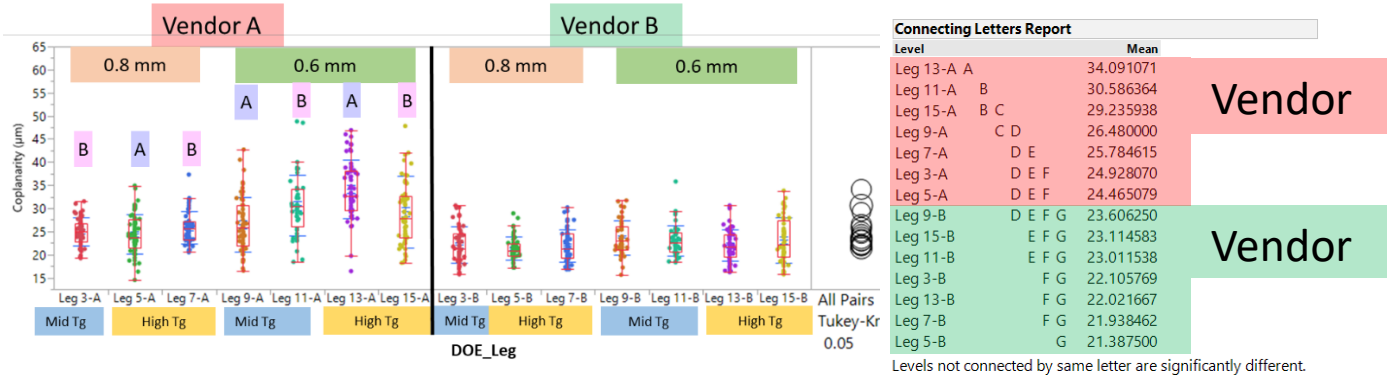

Figure 8: BGA coplanarity versus DOE leg by vendor

3.3.2 Panel Area Coplanarity at 240 °C

Figure 9 shows that shipping panel coplanarity for vendor A showed more variability for 0.6 mm vs. 08 mm thick PCBs. For vendor B, it was also found that the shipping panel coplanarity across all legs was statistically equivalent (minimal variability across all legs).

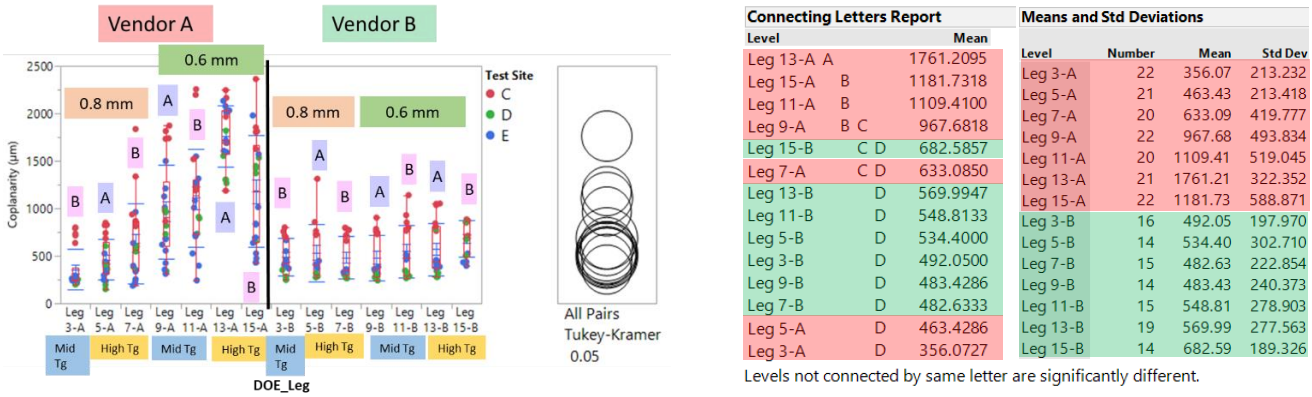

Figure 9: Shipping panel coplanarity versus DOE leg by vendor

4.0 Conclusion

As PCB designs become smaller and more compact to meet current industry trends, PCB thickness will shrink, thus resulting in greater PCB warpage during the SMT process. The key finding from this DOE is that PCB manufacturing and processing (i.e. press/lamination) has the greatest impact on PCB warpage, with thinner PCBs showing greater variability in coplanarity (i.e. Vendor A) vs. thicker PCBs (0.8 mm). However, PCB processing can reduce the variability in coplanarity between thinner (0.6 mm) vs. thicker (0.8 mm) PCBs as was observed with vendor B. Based on the findings of this work, it is believed that PCB post processing (i.e. post processing bake), material, and shipping panel location within the manufacturing panel have less impact on PCB warpage.

5.0 Next Steps

The key finding of this work is that PCB manufacturing and processing has the greatest impact on PCB warpage. Based on the key finding, the iNEMI team is currently trying to better understand the repeatability of the PCB manufacturing process for both vendors A & B, and whether or not the manufacturing process for vendor A can be optimized to reduce the variability in PCB warpage. Due to testing and manufacturing constraints, both vendor A & B will only repeat legs 9 & 11 of the DOE using the same Mid T_g material, 0.6 mm PCB stack-up and design, and processing conditions (i.e. the same press/lamination conditions A & B). Based on the repeatability of the PCB warpage results, the processing conditions A & B will be optimized for a final round of testing in order to see if vendor A can produce PCB warpage results similar to vendor B.

6.0 References

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