Impact of BGA Escape Trace Design on Thermo-mechanical Performance of Solder Joint

Cheng-Hao Chin, Gnyaneshwar Ramakrishna Cisco Systems Inc. ON, Canada chenchin@cisco.com

ABSTRACT

High performance computing application in recent years drives the development of Ball Grid Array (BGA) components to higher I/O count and greater power level. With demand on higher power consumption raise, to mitigate joule heating, current crowding and even to meet more strict power integrity requirement, usage of trace that has same width as non-solder mask defined (NSMD) pad or even usage of copper pour have gradually become viable design options. This change turns some of NSMD pads in the BGA footprint into partial solder mask defined (SMD) pads due to their wider BGA escaping trace and their exposure of greater solderable areas. It is important to understand how this kind of partial SMD would affect solder joint reliability when used in real application.

In this paper, a comprehensive study is presented to demonstrate the impact of different BGA escaping trace design cases on solder joint reliability by performing board level thermal cycling test on 3.2-mm 16-layer thick test vehicles. Various PWB layout variations such as pure SMD and pure NSMD pads with different trace width, trace count, routing direction and mix of different variations are studied. Two different daisy-chained components with 0.5 mm pitch and 0.8 mm pitch were used to understand their correlation with the type of package. The results showed design using wider trace would have longer solder joint fatigue life and this phenomenon becomes more significant when using component with smaller pad size. In addition, design using SMD pad showed the least performance among this study. Design using pad connecting to single wide trace showed similar characteristic life to those connecting to two wide traces. Moreover, it seems design using two wide traces have the benefit of extending its time to failure of first few wearouts. Finally, the outcome of design using mixing of 2 variations is also analyzed and discussed in this study.

Key words: reliability, TCoB, partial SMD, trace width, layout

INTRODUCTION

Solder mask defined (SMD) pad has been reported to have better resistance against dynamic loading than non-solder mask defined (NSMD) pad on the PWB side for ball grid array components [1,2]. However, when it comes to resistance against solder joint fatigue, NSMD pad shows superior performance compared to SMD pad. The usage of SMD and NSMD on the PWB pad design is highly dependent upon design requirement and end-use conditions. In network industry, for ball grid array (BGA) components with pitch greater than 0.5 mm, NSMD design is usually recommended due to advantages such as better solder joint reliability and increased clearance for routing between pads. Unlike SMD design, there is a gap of 2 mils at least between the NSMD copper pad and its solder mask edge, which is reserved for registration tolerance in SM printing, and thereby causing a small area for the escaping trace of the pad to be exposed under solder mask opening (SMO) area. This exposed portion increases the real solderable area and alters the solder joint effective shape geometrically. On the other hand, it's common to find a BGA escape routing using more than one trace width due to different purposes. Take routing of power as an example, a much wider trace is usually designed that connects the copper pads. Inevitably, the presence of wide trace will change the pad from its originally round shape.



Figure 1. Typical NSMD and partial SMD

With increasing power consumption of a single BGA component in high performance computing applications, usage of trace that has same width as NSMD pad or even copper pouring gradually become options for routing strategy to mitigate joule heating, current crowding or to meet power integrity requirement. In these schemes, some power pads in the land pattern are turned into partial SMD pads, as shown in Figure 1, while the rest of pads remains the per original definition. This leads to the mix of NSMD pads and partial SMD pads in the same BGA land pattern that can impact the life of the component in terms of the solder joint reliability.

Over the decades, temperature cycle on board (TCoB) or board level thermal cycling has been used to evaluate the performance of solder joint reliability of components mounting on printed wiring board (PWB). Various publications have investigated key factors that might degrade or enhance solder joint reliability [3-6]. To obtain quantitative TCoB result, implementation of daisy-chain circuit design, shown in Figure 2, is one of the key setups to examine and monitor solder joint integrity in real time during the temperature cycling test. Currently, this methodology has been widely adopted in electronic industry as one of the critical indices in package qualification. Among the completed TCoB tests, it is common to see the widths of escape trace being designed to be around 0.3 to 0.5 times of the pad diameter across the board regardless of if the pads are assigned for power or signal interconnects. Although the escape trace in TCoB test is only to form a closed loop connection for continuity, the difference from the real design brings an uncharacterized gap between TCoB results and the actual board level reliability.



Figure 2. Daisy Chain Circuit

Many studies have been published regarding to the effects of different trace design on solder joint reliability. [7] Malatkar et al mentioned using trace as wide as the pad diameter could significantly reduce the risk of trace crack in vibration test, but there is a lack of discussion on its impact on thermalmechanical performance. [1] Ma and Lee showed a particular escape trace design, round NSMD pad with 3 extra thin copper legs connected, has superior TCoB performance compared to the original design with trace count of 1. By finite element modeling, [8] Zhang et al studied the effect of PWB design on TCoB using wafer level chip scale package (WLCSP) which has pitch less than 0.4 mm. They observed that solder on a pad with two traces connected would have shorter solder joint lifetime than on a pad with only one trace connected, and even much shorter than pad without any trace. Although the trace width is not specified in their study, the appearance of traces showed considerable impact on solder joint fatigue life. [9] Noh et al showed the thermo-mechanical stress on the solder joint tends to decrease as the trace width increases in their simulation result. Although there is no discussion on its impact on reliability, the result still sheds light on the connection between trace geometry and solder joint reliability. To obtain a comprehensive understanding on this topic, this study uses various BGA land pattern design cases, including pure SMD, pure NSMD, different trace width, trace count, routing direction, and mixing of different trace width, in the test vehicle design. Post assembly of the component these test vehicles were temperature cycles with insitu measurements uses a datalogger. For each case, solder joint integrity was monitored, and the life data is presented using Weibull plot. After thermal cycling test, dye-and-pry and cross-section were performed to identify the failure modes.

EXPERIMENT SETUP Test Vehicle

In this study, 0.5 mm pitch and 0.8 mm pitch daisy-chained components were used to understand the consistency across

all design cases. For 0.5 mm pitch component, ChipArray Thin Core Ball Grid Array (CTBGA) with 228 pins was used, and for 0.8 mm pitch component, ChipArray Ball Grid Array (CABGA) with 192 pins was used. The body size of CTBGA is 12 x 12 mm and 14 x 14 mm for CABGA. The die size was 10.06 x 10.06 mm for CTBGA and 12.1 x 12.1 mm for CABGA. The ball alignment style of CTBGA and CABGA were both perimeters where 3 rows and 4 rows of solder balls are placed along the perimeters respectively. A16-layer 125mil thick PWB board with organic solderability preservative (OSP) surface finish was fabricated. Each board carried 15 BGA footprints (Figure 3). SAC305 solder alloy was used for both solder ball and solder paste, and the board level assembly was done using standard lead-free reflow process.



Figure 3. TCoB Test Vehicle

Design Matrix

The design cases used in this study are listed in Table 1. Cases that are blank in the matrix are routed along the package diagonal lines as shown in Figure 4. For these cases the entire ball map is partitioned into 4 areas which are in a manner of 90-degree rotational symmetry of each other about the center point. On the other hand, perpendicular routing scheme means to rotate all escape traces in the clockwise by 90 degrees for each site. Pad size of CTBGA 228 was shrunk to 9 mil to allow traces to have sufficient space while routing between 0.5 mm pitch BGA pads. All the daisy chain routings were completed on the surface layer and the second layer and the interconnects between layers are formed by microvias. Each component is assigned one independent closed-loop chain to monitor its continuity in this study.

Figure 5 shows all the escape trace design variations used in this study. The trace width of 3.5 mil is the baseline for both the components, CTBGA 228 and CABGA 192. The trace widths of 9 mil and 16 mil, which have the same width as the pads of CTBGA 228 and CABGA 192 respectively, are the group of wide trace cases. Aside from groups using single trace, two different cases were discussed in design using two wide traces as shown in Figure 5. The 2-traces-90-degree indicates two wide escape traces routed in two directions perpendicularly. Similarly, 2-trace-180-degree indicates a long wide escape trace routed to the pad and elongated from the other end of the pad. Finally, in the SMD case, SMO was designed to be the same size as CABGA 192 NSMD pad. However, the measured diameter after fabrication of the PWB is around 16.8 mil.

Figure 6 shows the concept of mixing different variations in the footprint for CTBGA 228 and CABGA 192. For the CTBGA 228, 3 corner-most pads are replaced with pads using wide trace and they were followed by two rows of pads using normal trace, and so on. On the other hand, for the CABGA 192, the arrangement of pads using normal and wide trace followed the typical x32 ball-out of graphic double data rate (GDDR) memory [10] where the normal trace is used for signal pad and the wide trace is used for either power or ground pad. The pads not able to match DDR ball-out around the upper and lower middle area are assigned normal trace.







Figure 5. Summary of escape trace design variations



Figure 6. Ball-out of design cases of mixing 2 different variations: (a) CTBGA 228; (b) CABGA 192; (c) ball-out of x32 GDDR

Table 1. Test Matrix

Component	CTBGA 228	CABGA 192
Pitch	0.5 mm	0.8 mm
Body Size	12 x 12 mm	14 x 14 mm
Die Size	10.06 x 10.06 mm	12.1 x 12.1 mm
Package Pad Size	0.3 mm	0.4 mm
PCB Pad Size	9 mil	16 mil
TEST MATRIX		
SMD		O
NSMD – Normal Trace	O	O
NSMD – Wide Trace	O	O
NSMD – Wide Trace - Perpendicular		O
NSMD -2 Traces -90°		O
NSMD – 2 Traces – 180°		O
NSMD – Mix Wide + Normal	O	O

Temperature Cycling on Board (TCoB)

TCoB was performed based on IPC 9701 at temperature ranged from 0C to 100C with 10 minutes of dwell time and 10 minutes of ramp time. The daisy chain resistance of each component was recorded every time the high or low temperature extreme was reached. Failure was recorded once 20% resistance change was detected, and Weibull plots were generated accordingly.

RESULT AND DISCUSSION Trace Width Effect and SMD

The TCoB test data of groups using different trace widths and SMD are shown in Figure 7 and Figure 8. The data indicates design using wide trace have longer solder joint fatigue life. The characteristic life of CTBGA 228 using wider trace

shows 30% increase as against the baseline normal trace. Similarly, the characteristic life of CABAG 192 using wide trace shows 10% increase than its baseline normal trace design. Based on the above results, the groups using wide trace outperforms normal trace in terms of reliability. This trend is consistent across two different types of components. It is worth noting that the rate of improvement drops when component has increase in pitch and size of pad. This is because the pad area increase is limited by constant clearance of SMO. In other words, 9 mil pads will benefit more from this 2-mil clearance than 16 mil pads due to their smaller size. Therefore, it is believed the impact of wider trace will not be significant on design using pad size greater than 16 mil as there is only 11.7% boost left.



Figure 7. Trace width effect on solder joint reliability of CTBGA 228



Figure 8. Trace width effect and SMD effect on solder joint reliability of CABGA 192

On the other hand, design using SMD pad shows 20% less fatigue life than baseline normal trace which is attributed to the shape of the joint with the SMD pad. Considering a SMD pad, the place where copper meets solder mask has a nearly right-angle outline locally. When a solder joint formed its shape along such outline, this abrupt change gives this region a higher stress concentration factor than the NSMD cases and makes the SMD location the weakest link for the entire solder joint. Although a part of this geometry (similar to SMD) appears on both normal trace and wide trace groups at where escape traces meet solder mask, the vulnerable regions of each group are still way less than that of a SMD pad which is the entire copper pad edge. In addition, instead of this vulnerable geometry, the increasing solderable area seems to dominate the performance of solder joint reliability in this case if we look at the performance of groups using NSMD pad. Therefore, the interaction between these two factors are associated from partial SMD to full SMD is still an area that needs to be explored further.

Design using Two Traces

Figure 9 shows the TCoB test result of two different groups that use 2 wide traces. The result from the group using single wide trace is also included for easy reference. Based on the result, the direction of the extra trace has no significant effect on the solder joint fatigue life. Likewise, compared to the group using single trace, groups using 2 traces have less than 5% of improvement on their characteristic life. Even so, it is still worth noting their time to failure of first few failures are longer than the group using single trace by 30% and it makes their Weibull slopes steeper. The slightly better solder joint performance might be attributed to greater solderable area. But the most important observation is that, even with twice the length of the SMD edge in single trace case, the trend of drop in fatigue performance due to closer to full SMD is not observed.



Figure 9. Two traces effect on solder joint reliability of CABGA 192

Effect of Routing Direction

Figure 10 and Figure 11 show the Weibull plot of groups using different trace routing direction. The results indicate routing perpendicularly has slightly negative effect on the performance of solder joint reliability in both CTBGA 228 and CABGA 192 cases. Among these two cases, the group using CABGA 192 shows a relatively more significant difference. This might be associated with the orientation of the final shape of the pads. However, the true mechanism remains unclear. Despite the negligible effect of routing direction, it is still suggested to follow the same fanout direction as the real application when doing TCoB test vehicle design.



Figure 10. Routing direction effect on solder joint reliability of CTBGA 228



Figure 11. Routing direction effect on solder joint reliability of CABGA 192

Effect of Mixing of difference variations

Figure 12 and Figure 13 show the Weibull plot of group cases that were designed with mixing of wide and normal trace. To better understand the effect of mixing, data from the groups using purely normal and wide trace are included. The result indicates the groups using mixing of two variations have its reliability performance fall between those of groups using purely one variation. In the case of CTBGA 228, the life data from the mixed group is almost positioned in the middle of those from groups using normal and wide trace alone. Similarly, the life data from the mixed group using CABGA 192 are also bounded, and they are positioned much closer to the group using wide trace. To understand how these life data drift between two extremes, finite element analysis is suggested for more insight. Even though a theory from a microstructure perspective is not yet available, this finding still suggests a way to evaluate the solder joint reliability in real application without needing to understand the complex interaction among joints.



Figure 12. Effect of mixing of difference variations on solder joint reliability of CTBGA 228



Figure 13. Effect of mixing of difference variations on solder joint reliability of CABGA 192

Failure Analysis

Dye-and-pry and cross-section are the two common methods to understand the failure modes in this study. Figure 14 and Figure 15 show a dye-and-pry failure map and magnified optical images of a CTBGA 228 component from the group using wide trace. This component was pried after 659 cycles of TCoB test, and the pads with dye penetration are mainly observed at the outermost rows as well as the corners. From Figure 15 (d) and (e), the initiation of crack can be identified from the pads with partial dye penetration which is where the traces meet solder mask. This observation could be confirmed by cross-section SEM images as shown in Figure 16 where the crack is only halfway of its path. As a result, the inspected failure modes show a good level of consistency to the previous discussion regarding to the weakest link of a solder joint in this study. In addition, regardless of CTBGA 228 or CABGA 192, most of the cracks are found on the PWB side of the joints. Although some minor cracks are found on the component side, considering their crack lengths, they are not sufficiently severe to be marked as critical as the root cause of their continuity failure. This finding supports the existence of the correlation between the reliability of the solder joints and how land pattern is designed.



Figure 14. Figure 14 Dye-and-pry failure map of CTBGA 228



Figure 15. Dye-and-pry failure map of CTBGA 228



Figure 15. Cross-section of CTBGA 228

CONCLUSION

A comprehensive study is presented to demonstrate the impact of different BGA escape trace design cases on solder joint reliability. The result showed longer characteristic life for design using wider trace and this phenomenon becomes more significant when using component with smaller pads. It is also believed that the effect of wide trace will be less effective on design using component with pads greater than 16 mils. Besides, design using SMD pad gives the worst solder joint reliability performance among all the cases.

When comparing design using single trace and design using two traces, the latter has less than 5% of improvement on characteristic life and it's time to failure of first few failures has an improvement in cycle by about 30%. It is believed that design using this kind of partial SMD pad would still get completely different reliability characteristic from that of a full SMD pad.

Routing perpendicularly has slightly negative effect on the performance of solder joint reliability compared to routing diagonally. The cause of this phenomenon requires further investigation. Thus, it is suggested to keep the same fanout direction as the real application when design TCoB test vehicle.

Design using mixing of two variations in a single footprint would have its reliability performance bounded by those of design using each variation alone. The detailed mechanism should rely on finite element analysis for more insight.

From the failure analysis perspective, the inspected failure modes show a good level of consistency of the weakest link of a solder joint. Besides, most of the cracks are found on the PWB side in this study and it supports the existence of the correlation between the reliability of the solder joints and how their underneath land pattern is designed.

ACKNOWLEDGEMENTS

We gratefully thank Jennifer Oliver and Dr. Tae-Kyu Lee for their guidance and suggestion of this work.

REFERENCES

- 1. H. Ma and T. -K. Lee, "Effects of Board Design Variations on the Reliability of Lead-Free Solder Joints," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 3, no. 1, pp. 71-78, Jan. 2013.
- D. Yap, K. S. Wong, L. Petit, R. Antonicelli and S. W. Yoon, "Reliability of eWLB (Embedded Wafer Level BGA) for Automotive Radar Applications," 2017 IEEE 67th Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2017, pp. 1473-1479.
- H. Qi, M. Osterman and M. Pecht, "Design of Experiments for Board-Level Solder Joint Reliability of PBGA Package Under Various Manufacturing and Multiple Environmental Loading Conditions," in IEEE Transactions on Electronics Packaging Manufacturing, vol. 32, no. 1, pp. 32-40, Jan. 2009.
- A. C. P. Lim, Lee Teck Kheng, A. Alamsjah and Happy, "The effect of ball pad designs and substrate materials on the performance of second-level interconnects," Proceedings of the 5th Electronics Packaging Technology Conference (EPTC 2003), Singapore, 2003, pp. 563-568.
- B. Singh et al., "Board-Level Thermal Cycling and Drop-Test Reliability of Large, Ultrathin Glass BGA Packages for Smart Mobile Applications," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 7, no. 5, pp. 726-733, May 2017.

- Wei Sun, W. H. Zhu, E. S. W. Poh, H. B. Tan and R. Te Gan, "Study of five substrate pad finishes for the codesign of solder joint reliability under board-level drop and temperature cycling test conditions," 2008 International Conference on Electronic Packaging Technology & High Density Packaging, Shanghai, China, 2008, pp. 1-8.
- P. Malatkar, Shaw Fong Wong, T. Pringle and Wei Keat Loh, "Pitfalls an engineer needs to be aware of during vibration testing," 56th Electronic Components and Technology Conference 2006, San Diego, CA, USA, 2006, pp. 6 pp.-.
- 8. H. Zhang et al., "45RFSOI WLCSP Board Level Package Risk Assessment and Solder Joint Reliability Performance Improvement," 2020 IEEE 70th Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2020, pp. 2151-2156.
- H. Noh, K. Lee, J. Bae, Y. Hwang, H. Kim and S. Pae, "A Parameter Study for the Design Optimization to Relieve Pattern Stress of PCB under the Temperature Cycling Condition," 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2022, pp. 1754-1758.
- 10. "Jedec Standard JESD250D", "Graphic Double Data Rate(GDDR6) SGRAM Standard", May 2023.