As originally published in the SMTA Proceedings.

Homogeneous Low Temperature Soldering Technology Quality, Reliability and Manufacturability

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ABSTRACT

There is a shift in the microelectronic industry towards low temperature soldering (LTS) technology that incorporates a bismuth-based chemistry in Sn-based solder alloys. These chemistries are attractive due to their benign environmental impact and their capacity to keep warpages under control during the reflow process. However, enabling this technology requires investigating the quality and reliability of LTS ball grid array (BGA) mounted packages vs that of traditional Sn-Ag-Cu (SAC) BGA packages. This paper presents key findings of enabling LTS technology on AMD's Client BGA Packages using surface mount technology (SMT). It will highlight the thermal cycling performance of SAC and LTS assemblies are comparable, while in the mechanical shock testing the SAC assemblies performed significantly better than LTS assemblies. We recommend using adhesives (i.e. edge bond) to bridge the gap in mechanical shock performance of the two material technologies. In conclusion, LTS assemblies offer a viable alternative to traditional SAC under client-use conditions.

Keywords: Low Temperature Solder (LTS), Surface Mount technology (SMT), Board Level Temperature Cycling (BLTC), Mechanical Shock Testing (MST)

INTRODUCTION

Surface Mount Technology is used to mount packages by printing solder paste on the printed circuit boards (PCB) and then reflowing through a conventional oven. The success of this technology depends on robust joint formation between the ball grid array (BGA) interconnects on the package and the paste applied on the PCBs. During the SMT reflow process, the plane of the PCB board and the package BGAs are seldom in perfect parallel configuration. In fact, there is an inherent warpage due to the differences in coefficient of thermal expansion (CTE) of the package and PCBs. During the reflow process, this 'dynamic' warpage can manifest itself by a change in the shape of the package and PCB typically going from convex to concave and vice versa in reverse, see Figure 1. Mismatch in the shape of the package and board during the reflow and ramp down stages can lead to defects in the joint formation process such as head and pillow (HnP) and non-contact opens (NCO). The most common SMT defect modes are shown in Figure 2.

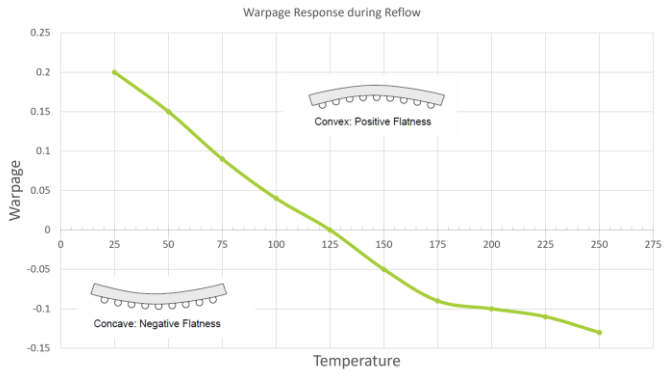


Figure 1. Dynamic warpage response of a package showing package inversion around 150C

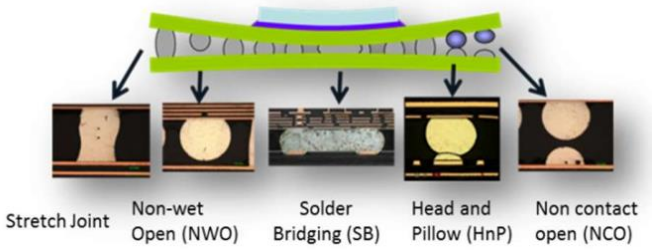


Figure 2. Common Defect modes in SMT [1]

These defects can be mitigated through various techniques such as stencil optimization or controlling warpage during the reflow process. One method of keeping the warpages low is to reflow the assembly at a lower peak reflow temperature. A lower temperature results in a smaller absolute warpage change of the package during the reflow process. This can be enabled by using tin-bismuth based low temperature solder alloys.

Currently majority of SMT in the client market is performed using Sn-Ag-Cu (SAC) based paste materials, however, Sn-Bi based LTS alloys are a promising alternative to the traditional SAC based processes. These LTS alloys require lower reflow temperatures that can lead to reduced energy consumption during the ball attach assembly and the SMT processes by up to 40% [2]. This reduction in CO_2 emissions and manufacturing costs is an environmentally friendly and "green" alternative to the traditional SAC processes which typically require a reflow peak temperature of 260 °C. LTS conversion for microelectronic assembly potentially saves 35K -50K metric tons of CO2 which is equivalent to 33-55 million pounds of coal burned. These Sn-Bi based LTS alloys have melting ranges from 138ºC to 175ºC which allows for a lower SMT peak reflow profile, (Figure 3) translating to an overall reduced package warpage magnitude during the reflow process. Sn-Bi pastes are categorized into near-eutectic (57-58wt%Bi) and off-eutectic (35-40wt%Bi) alloys which present different tradeoffs between manufacturability and reliability [3, 4].

There are two ways to use low temperature reflow process to mount packages on boards: 1) Hybrid LTS, where the package uses SAC BGAs and the paste on PCB is LTS paste, and 2) Homogeneous LTS, where both the package and the PCB paste are LTS. Both can be assembled at a reflow peak temperature of 180 °C – 195 °C. While hybrid LTS assemblies circumvent the need to enable LTS processes at the ball attach assembly level, they require much more involved process optimization for SMT due to their own unique defects [5]. This is due to the non-melting and non-collapse of SAC BGAs at <210 °C reflow temperatures. This typically results in a joint with higher stand-off height that are more prone to hot tearing defects [6]. Hybrid assemblies also pose an additional challenge of having a narrower allowable warpage spec than homogeneous assemblies, and generally perform worse in temperature cycling and mechanical shock testing than homogeneous LTS assemblies [7]. In contrast, homogeneous LTS exhibit full solder joint collapse during the lower peak reflow temperature, have a lower stand-off height and show better reliability performance [8, 9]. Therefore, homogeneous LTS assemblies offer a viable solution of allowing for using low temperature reflows while keeping warpage under control. In this paper, we are reporting our work on homogeneous LTS assemblies with SAC assemblies as our control. Currently, in the absence of regulatory imperative to derive the LTS based technology development most ODM/OEMs are enabling this technology on a case-by-case basis. A more concerted industry wide effort would be needed to standardize material selection, reflow profile selection and benchmark the reliability performance of the multiple flavors of LTS material available for SMT.

EXPERIMENTAL SECTION

LTS Metallurgy

In this study, the Sn-Bi metallurgy with the off-eutectic composition of Sn-37Bi-Sb-Cu and a melting temperature range of 139°C – 174 °C was utilized. Table 1 summarizes the material and peak reflow temperatures of the material used. The optimized reflow profile for our package assembly is shown in Figure 3, with the peak reflow temperature range of 190°C – 195 °C. The SAC reflow profile is also shown on the same plot for reference. Material details for SMT paste and BGA balls are shown in Table 1.

Table 1. SMT Materials details

	SAC	LTS
SMT Paste Alloy	SAC305	Sn-37Bi-Sb-Cu
Reflow temperature	217-220 °C	139~174 °C

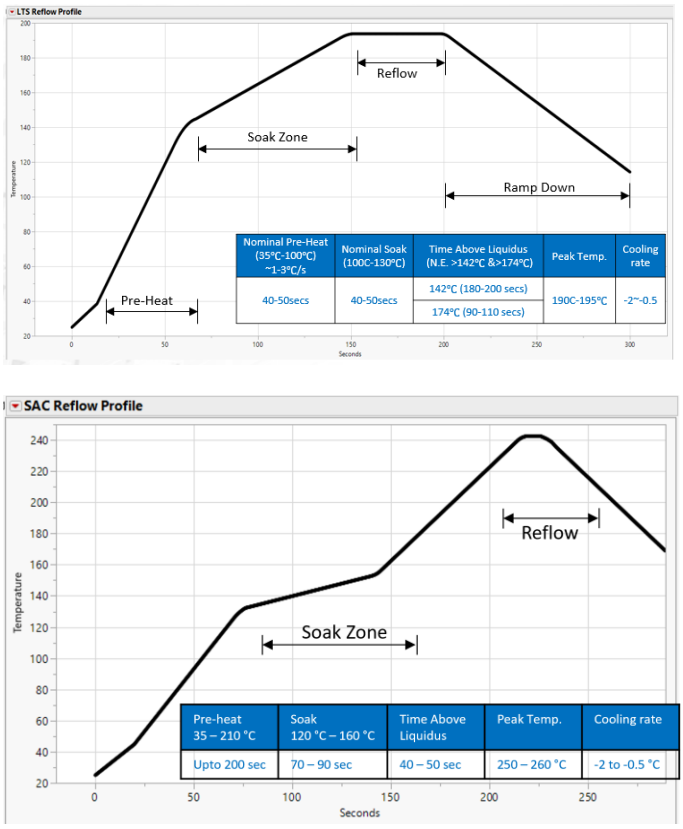


Figure 3. Typical LTS and SAC Reflow Profiles

Assembly and SMT Processes

The ball attach manufacturing flow does not change between LTS and traditional SAC systems, thus another benefit is that no incremental tooling costs are required for

industry conversion. Assembly and test was demonstrated healthy (on par to SAC) BGA yields using the optimized LTS ball metallurgy selected. All packages were subject to the full interaction within the high-volume manufacturing flow Test Package Interaction (TPI) studies to look for any incremental warpage or ball damage due to the material being softer at higher temperatures. To verify the solder joint quality ball shear testing as well ball pull testing was conducted, and both were found to be better than SAC baseline, which is very promising.

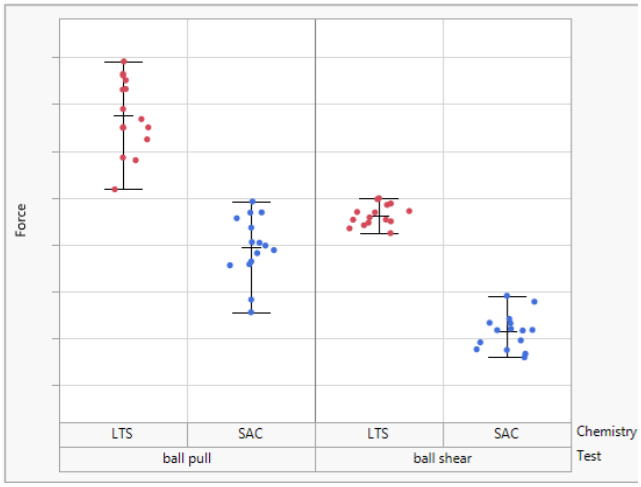


Figure 4. Ball Pull and Shear Comparison between LTS and SAC

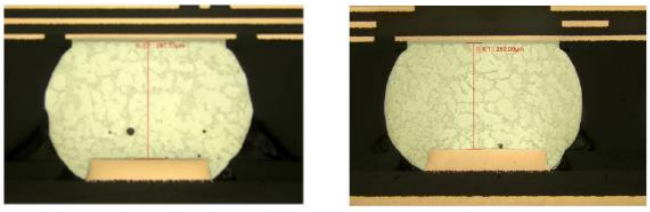
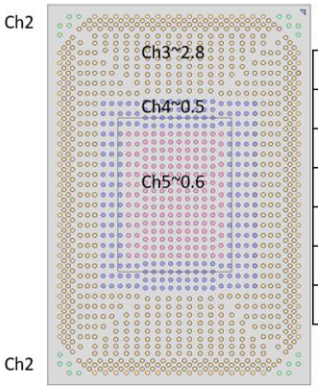


Figure 5. Cross section of LTS joints for different ball attach and SMT reflow profiles.

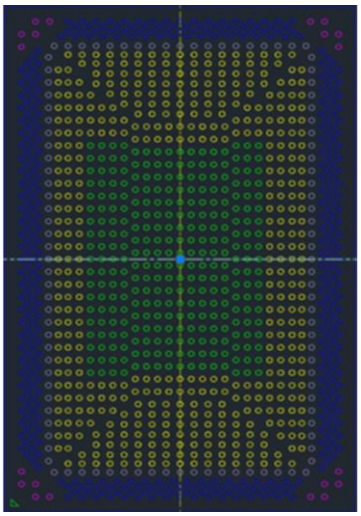
The lower boundary conditions for peak reflow temperature during the ball attach (BA) process. We found that peak reflow temperatures of 185°C and 195°C both yield equally healthy solder joints post reflow and SMT as shown in Figure 5. For the experiments reported in this paper, the peak reflow temperature of 195°C was selected to ensure that the flux is fully activated to create a robust joint between the ball and the paste.



Package Attributes	
Pkg Type	FCBGA
Size	25 mm x 40 mm
Pitch	0.64 mm
BGA pad design	SMD
Pad surface finish	ENEPIG
Board finish	OSP

Figure 6. Daisy Chain Test Vehicle and mean R values.

For reliability testing, units are pre-baked at 100°C for 48hr, so that degradation related to moisture exposure time (MET) would not confound the results. The structural integrity of the solder interconnect is monitored in-situ by daisy-chain resistance (DC R) measurement during the test. All BGA interconnects are daisy-chained and grouped into 5 channels according to different regions of interests as shown in Figure 6. For PCB, a 10-layer stacked PCB configuration at 1.2 mm thickness was designed based on system reference designs. The board surface finish was Cu-OSP. For SMT, a variable stencil was used for both thermal cycling and mechanical shock testing as shown in Figure 7.



Ball region	Aperture Size
0.35mm pad dia	0.49 mm
0.3mm pad dia	0.41mm
0.3 mm pad dia	0.41mm
0.3mm pad dia	0.45 mm
0.4 mm pad dia	0.5 mm

Figure 7 Optimized stencil used for this study.

RESULTS & DISCUSSION

Temperature Cycling (TC)

Due to the nature of the low homologous temperature of LTS BGA, TC profile of -40/105°C is used instead of standard JEDEC TCG condition (-40/125°C). This TC profile is also more representative of several client-based use conditions (i.e. laptop and desktop systems). This testing was performed with a dwell time of 10 min and ramp

rate of 10°C/min, using a failure criterion of >20% change of resistance per daisy chain (DC). During this test, failed units are taken out for dye-and-pull (DnP) and/or cross-sectioning, where optical inspection is then performed to define the failure mode and locations within the BGA array. The test is terminated once it has reached either 3000cyc or when 63% of the total sample has DC R failure within Ch 3, 4 or 5, whichever comes first. Weibull characteristics for SAC and LTS legs are reported to be within 1% of each other, which is statistically equivalent performance as shown in Figure 8.

Dye and Pry (DnP) of the failed boards after thermal cycling indicates that most of the cracks observed were in the die shadow region, with type 2 cracks that form between the package and solder joint (Figures 8 and 9). The total number of solder joints that have partial cracking is higher in LTS assemblies as compared with SAC. The extent of cracking on LTS joints is typically between 50 – 75% of the joint width, while the SAC joints cracks ranged from 25 – 50 % of the joint width. Cross section data reveals that the failures was due to solder crack near component side on both control and LTS legs as shown in Figure 9. Also, it was observed that over time the bismuth in the LTS joints becomes coarser during the thermal cycle. This coarsening of the bismuth and the brittleness of bismuth eventually lead to crack propagation and fracturing over time. This phenomenon is observed in, Figures 10, 11. The crack signature is similar between SAC and LTS within the bulk solder but near the package interface of the joint.

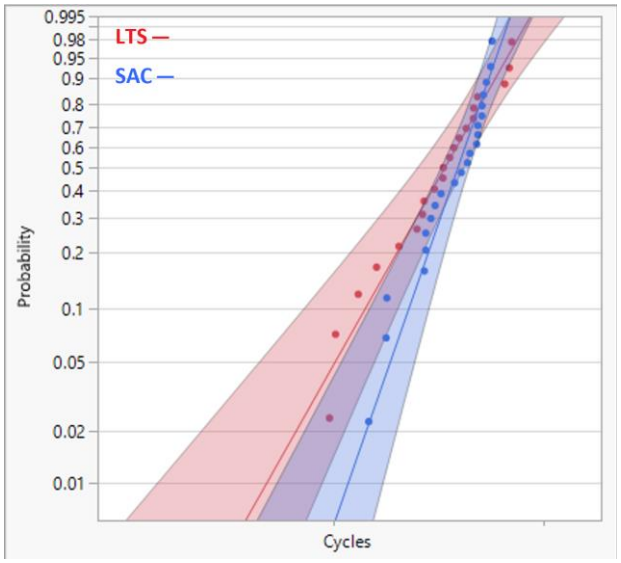


Figure 7. Weibull Analysis based on in-situ DC R failures for LTS and SAC305 show statistically equivalent performance for Temperature cycling.

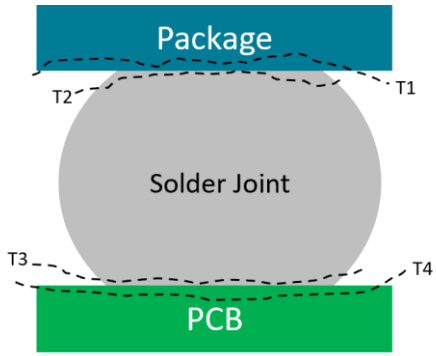


Figure 8. Fracture types based on the crack locations.

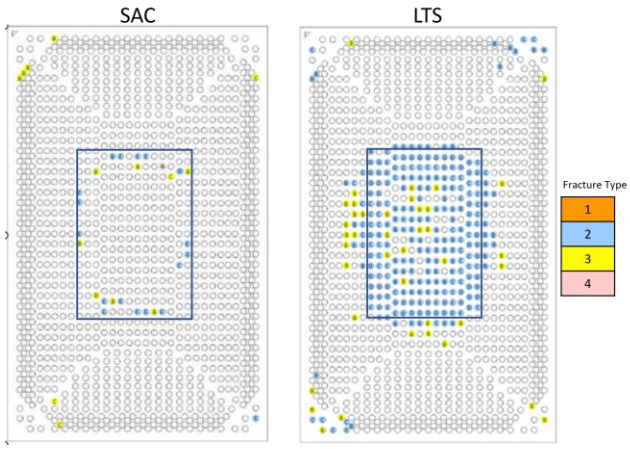


Figure 9. Dye and Pry failure analysis after temperature cycling shows solder joint cracks, the blue rectangle indicates the die shadow region.

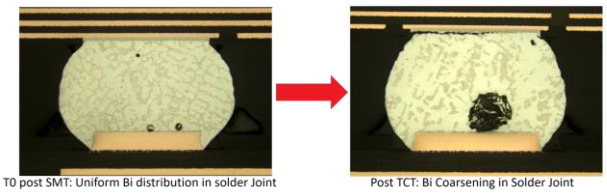


Figure 10. Bismuth Coarsening and solder joint cracking comparison of pre/post thermal cycling.

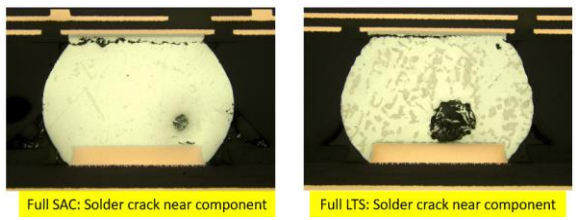


Figure 11. Failure Analysis shows similar defect mode propagating in SAC and LTS packages.

Mechanical Shock Test

In mechanical shock testing, cliff finding is performed to obtain the critical input g-level from a total of 6 drops at -Z board orientation (package dead bug). Next, drop-to-failure

testing is conducted to obtain the characteristic drop-life. For mechanical shock test, hybrid assemblies comprising of SAC packages and LTS paste were also included in the experimental matrix for comparison. Test conditions of 500g and 900g were run separately as shown in Table 2.

Table 2. Mechanical Shock Testing Results

Test cond.	Leg	Normalized MTTF	DnP analysis (Major failure mode observed)
500g	SAC	100 %	Pad cratering (<50% crack area size)
	SAC-LTS	15 %	Solder crack near PCB side
	LTS	87 %	Solder crack near package side
900g	SAC	100 %	Pad cratering
	SAC-LTS	4 %	Solder crack near PCB side
	SAC-LTS (EB)	137 %	No ink penetration

With the 500g test conditions, homogeneous SAC assemblies performed the best, followed by homogeneous LTS and hybrid SAC-LTS assemblies respectively. Data for the SAC-LTS assemblies can be used to provide an enveloping scenario for the homogeneous LTS assemblies. Referring to the fracture types in Figure 8, the main defect mode observed in SAC assemblies was pad cratering a type 4 defect, whereas in homogenous LTS or hybrid assemblies it was type 2 or type three solder cracking as shown in Figure 13. The LTS system contrasts with what is typically observed in mechanical shock testing failures in traditional SAC packages. This could be due to the brittleness of Bi that is more sensitive to the high strain rate loading especially at the interface of solder joint and package and is consistent with the literature of LTS shock/drop[10]. On SAC packages, the cracks observed were between the Cu pads on the PCB and the PCB laminate, indicating the fractures were not in the solder joint body.

A subsequent test with 900g was performed using the SAC and hybrid assemblies (with and without edge bond adhesives) to obtain any mechanical shock improvement with adhesives. The 900g test shows that edge bond adhesives significantly enhance the mechanical shock reliability of the hybrid assemblies, and results in a better performance than the SAC assemblies. Comparing the 900g results with 500g results, data shows that any improvements in hybrid assemblies will envelope the performance of homogeneous LTS assemblies. Hence, homogeneous LTS assemblies with EB adhesives are expected to perform on par with SAC assemblies.

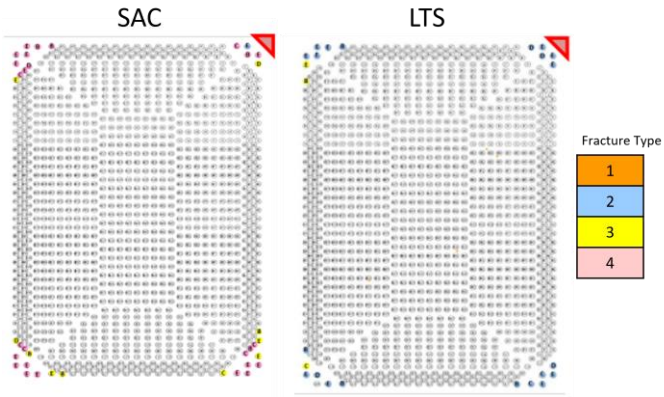


Figure 13. DnP results of the mechanical shock tests, showing majority of the fractures at the package corners.

FUTURE WORK

There is a need to establish more baseline data for packages that use LTS SMT. While the temperature cycling on LTS mounted packages is on par with SAC packages, the mechanical shock performance clearly lags that of SAC packages. To improve the mechanical shock reliability of LTS assemblies by incorporating edge bond adhesives and exploring optimized use conditions for these assemblies.

CONCLUSION

LTS assemblies on AMD's client packages and their temperature cycling and mechanical shock testing reliability with SAC assemblies were compared. Results indicate that thermal cycle reliability performance of LTS packages is comparable with SAC packages, whereas the mechanical shock performance lower. Given this, edge bond processes are recommended to improve the mechanical shock performance of the LTS assemblies and bring it on par with SAC interconnects to enable future LTS assembly's opportunities in the client segment.

ACKNOWLEDGEMENTS

The authors would like to thank Dekra iST Reliability Services, Rahul Joshi, Eng Is, Yongbo Yang, Junping Han, Key-kiat Yeo and Himanshu Bal for their contributions.

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