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Heterogenous Integration using Fan-out Wafer-level Packaging (FOWLP) Technology to Produce High Performance and Low-Cost Multi-Chip Modules

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ABSTRACT
There are numerous market drivers that are achieved using fan-out wafer-level packaging (FOWLP), such as: reduced form factor, improved electrical performance due to shorter interconnects, lower packaging costs, chiplet integration, and lower power consumption. FOWLP is a platform that is projected to have one of the highest growth rates for advanced packaging [1] and is very well suited to address a wide range of applications, including high-performance multi-chip modules that have through mold vias (TMVs) and double-sided build up layers. To achieve these goals, the Deca M-series™ fan-out technology is a leading contender. The novel features of this technology are mask-less laser direct imaging, Adaptive Patterning, and the capability to do 2µm Lines/Spaces (L/S). In this paper, an overview of packages having multiple die along with double-sided build up layers will be presented. The process flow will be discussed to show how this technology can provide high module yields, fine L/S and accommodate 20µm die pitch.

Key words: Fan-out wafer-level packaging (FOWLP), chiplet, through mold vias (TMVs), mask-less laser direct imaging, Adaptive Patterning, and multi-chip modules (MCMs).

INTRODUCTION

Growth of advanced FO-WLP (fan-out wafer level packaging) or simply fan-out, is upon us as the industry moves from historical monolithic SoC (system on chip) scaling to multi-die architectures using chiplets. The emerging multi-die devices can be either homogeneous or heterogeneous or combinations of both and are being driven by today's most advanced applications including 5G, AI, autonomous driving as well as the Internet of Things. In this paper, we will explore the use of Laser Direct Imaging or LDI with Adaptive Patterning® as a platform for photolithography in support of this ever more complicated package integration in multi-die integration. LDI is not for substrates only and was introduced to wafer level packaging many years ago. Driven mainly by digital micro-mirrors, newer systems on the market are imaging 2µm with roadmaps down to 1.5µm.

The industry describes FO-WLP technology as a solution that uses epoxy mold compound (EMC) to embed the die and either protect a fan-in device or fan-out the chip area. FO-WLP utilizes the massively parallel processing capability of wafer or panel level to create the interconnect layers. M-Series™ is a chips-first, face-up FO-WLP technology with the semiconductor devices active surface and vertical sidewalls fully encapsulated within the EMC. The device interconnect is enabled by Cu studs through the EMC as shown in the protected fan-in cross section in Figure 1.

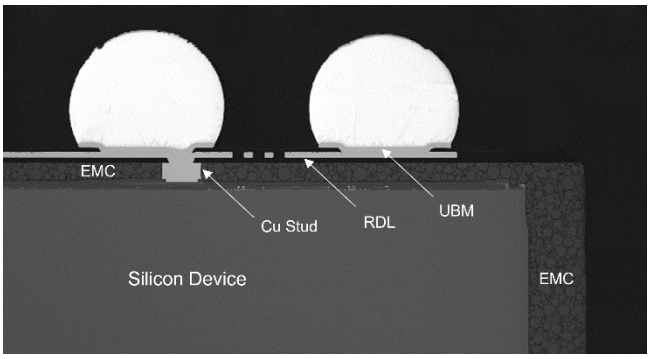


Figure 1. Cross-section of M-Series™ structure

II. Adaptive Patterning®

Adaptive Patterning (AP) was developed in conjunction with Deca's Chips-first, Face-up FO-WLP structure to overcome the inherent inaccuracies associated with creating a composite wafer or panel consisting of individual devices embedded within EMC or alternate materials from die drift or shift. This patented lithographic patterning technology includes the high-speed measurement of each die location within the panel and real-time creation of a design which perfectly fits the as-built panel by applying a unit specific pattern to each device. Through AP, simple devices to complex heterogeneous multi-chiplet systems can be constructed cost-effectively with assurance of high yields in manufacturing.

Multiple techniques are available to adjust the unit layout in response to die-shift. The first, Adaptive Alignment, allows the RDL and first via layer pattern to be dynamically aligned to match the measured lateral die shift and rotation for each device. Another technique, Adaptive Routing, regenerates portions of traces to accommodate die-shift. Often, Adaptive Routing is combined with Adaptive Alignment to regenerate connections between two or more die to account for the much larger combined die-shift.

Figure 2 summarizes the lithographic patterning technology flow. At the end of the 'Panelization' process, a high-speed optical scanner is used to inspect the exposed Cu stud on the surface of the mold compound for each die to determine the position on the panel with respect to its nominal design position. A proprietary real-time design tool optimizes the fan-out unit design for each package on the panel so that the first via layer and fan-out RDL patterns are precisely aligned to the Cu studs on the die. The design files for each panel are imported to an LDI lithography machine which uses the unique design data to dynamically apply a unit-specific, adaptive pattern to every device on each panel.

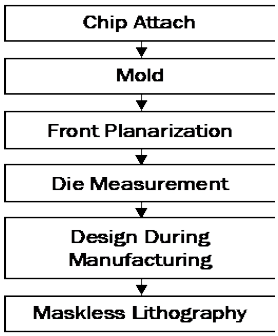


Figure 2. AP Process Flow

Figure 3 shows an example of a two-die device, one die on the left (DIE 1) and one on the right (DIE 2). The Cu studs connect through the mold to the die bond-pads. The visible RDL pattern was applied without lithographic patterning technology, and significant misalignment of the first via layer to the Cu studs due to die-shift is visible in the black areas [3].

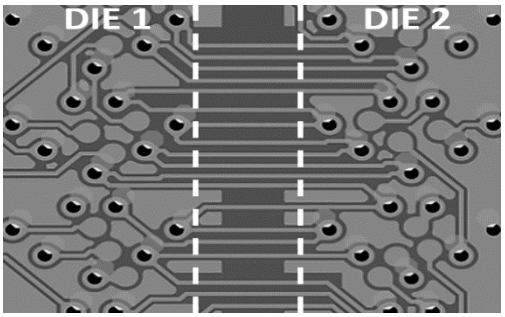


Figure 3. Example of RDL and Via opening not aligned with the Cu studs. The dark circles show missing Cu studs underneath. Dotted lines represent the area between the two die.

In Figure 4, the same manufacturing process is used, but the Adaptive Alignment technique was applied to dynamically align the RDL for DIE 1 and DIE 2 to their respective Cu stud locations. DIE 1 and DIE 2 have independent shift variations, so their regions of the RDL pattern are aligned separately. For the die-to-die connections, the Adaptive Routing technique dynamically regenerates the RDL connections (the area between dotted lines).

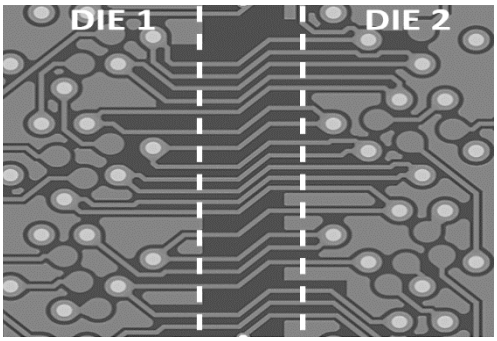


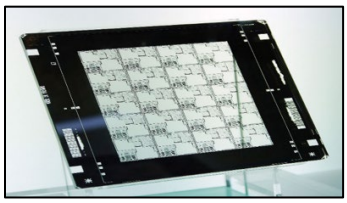
Figure 4. Example of Deca's lithographic patterning technology aligning the RDL with the Cu studs. Since no dark circles are present, Cu studs underneath the RDL are perfectly aligned. Dotted lines represent the area between the two die with Adaptive Routing.

III. Mask-Less Lithography

FO-WLP can provide a solution to front-end scaling limitations. Large die area is increasingly undesirable in the front-end due to low yield and high cost. For these reasons, the industry is trending away from traditional monolithic SoC toward designs that are partitioned into multiple smaller chiplets and integrated using fan-out technologies.

In addition, a key limitation for such complex designs has been the reticle limit of lithography tools, typically around 850mm^2. Customers are now asking for packages from 36mm x 36mm (1,296mm^2) to 85mm x 85mm (7,225mm^2). In a stepper environment, reticle stitching is required, which brings its own challenges that affect throughput and routing density, see Figure 5 [10].

a.



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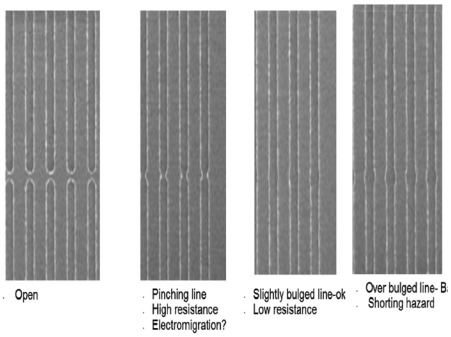

Figure 5. (a) A key limitation for such complex designs has been the reticle limit of lithography tools, typically around 850mm^2. (b) Reticle stitching challenges reported in literature.

With these tools of Deca's lithographic patterning technology and LDI, creation of boundless heterogenous packages can be realized. This allows seamless interconnects between the dies and the LDI allows packages size up the to the formats in use in the fabs, for example 300 or 600 mm.

IV. Aspect Ratios

Key to the building of advanced packages is the creation of Through Mold Vias (TMV) approaching aspect ratios of 4:1.

The latest generation of 3D PoP being co-developed by Deca and SkyWater requires this 4:1 aspect ratio process (creating through mold Cu posts with a 150µm pitch). To create this integration, Deca required a resist thickness of > 240µm and with CD imaging performance of < 60µm.

One application for these processes is shown in Figure 6 below called Embedded Active Die Interposer. This is an active customer design that includes one active embedded die (chips first) in an organic mold compound surrounded by through mold Cu posts with four die (chips last) on top. The Cu posts allow interconnect of two RDL layers from the backside (solder ball side) with the three RDL layers on the topside. The chips last is mounted at the end of the process flow followed by a lid cover (not shown).

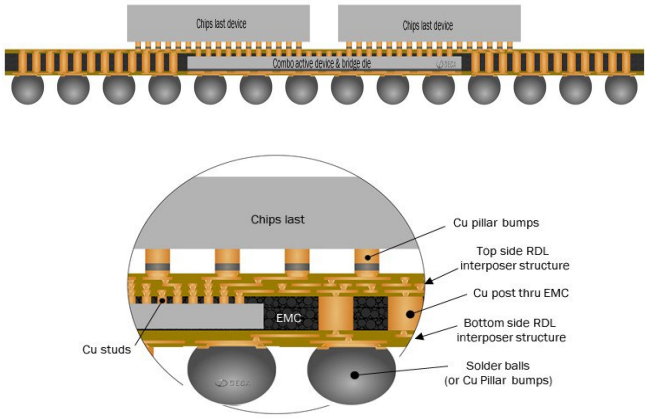

Figure 6. Active customer design using Deca's Fan-out WLP structure and Lithographic Patterning Technology with dry films for through mold Cu posts and liquid resist for RDL.

Another key LDI advantage is the ability to utilize a unique optimized design per wafer to precisely overcome embedded die shift related to natural variation due to die placement and compression molding. Adaptive Patterning electronic design automation (EDA) tools are utilized by package designers to establish deterministic rules for Adaptive Alignment, Adaptive Routing or Adaptive Metal Fill for each new product.

In the above design, Adaptive Alignment is used in an LDI environment to align the first via layer to the Cu studs to compensate for the movement of the die during die attach and mold. When more chips are added into the package (multi-die), Adaptive Routing is used to compensate for the inherent multi-distributed die shift. Adaptive Metal Fill is used to manage pattern densities across the package, eliminating large open areas leading to topography affects (important for > 2 RDL layers), see Figure 7.

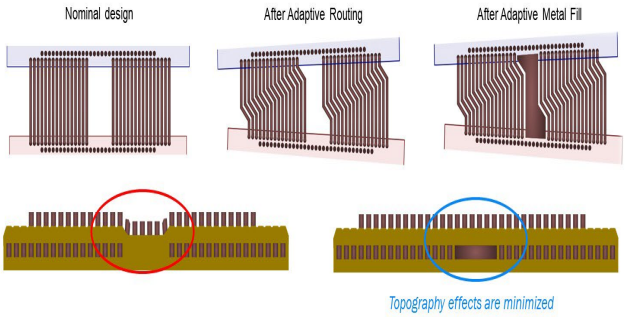

Figure 7. Adaptive metal fill is used in conjunction with Adaptive Routing and Adaptive Alignment to minimize the topography affects, critical for high-density multi-layer RDL applications.

In this design example, it is possible to use both LDI and steppers to complete this integration. The bottom side RDL's, Cu post, and Cu studs can all be created in a stepper or LDI environment leaving the topside Via and RDL layers exclusively for the LDI tool (due to uniquely optimized unit specific designs per wafer or panel).

The use of steppers along with LDI tooling allows fabs to re-use current capital with the stepper limitation listed above of reticle size requiring stitching for large package body sizes.

V. LDI and RDL Patterning

A new generation of LDI tools are coming to market with enhanced capability to achieve 2µm lines and spaces and below.

Next generation tool, DE-2, that supports Deca's Gen 2 process has demonstrated 2µm lines & spaces using liquid resist that was tailored for 405nm and supports both 300mm wafers and 600mm x 600mm large panels. Below, in Figure 8, is a test case of RDL at 2um lines and spaces done on a 300mm Cu seeded wafer at ADTEC.

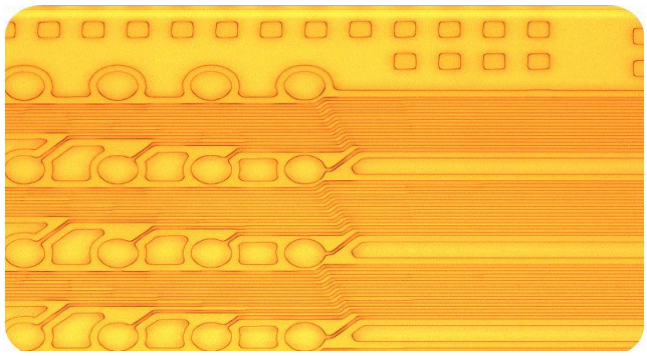

Figure 8. 2µm line & space on a 300mm Cu seeded wafer imaged at ADTEC. ADTEC tools are capable of formats from 200mm up to 600mm.

Additional LDI suppliers have entered the market and show promising capabilities for the future. Heidelberg Instruments is an example using mixed wavelengths including 375nm and 405nm. The shorter 375nm option opens the door for using more broadly available I-line sensitive materials.

VII. Conclusion

In this paper, LDI was presented as an option for photolithography in the advanced packaging discipline. Currently LDI is deployed for both 300 and 600mm formats at Deca's licensee partners in support of M-Series™ with Adaptive Patterning®. LDI has advantages of higher DOF, mask-less, large panel processing experience, large packages without reticle stitching, and real time design optimization. LDI processing classically uses dry films from the PCB industry supporting high aspect ratio imaging up to 4:1. Liquid resists have been developed in support of 2µm line & space using 405nm for advanced RDL features. These processes have been successfully deployed in support of heterogenous integration in multi-die products. The LDI tool enables full lithographic patterning technology capability to maximize yield, enhance design rules and improve performance.

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