Effect of QFN I/O Pad Solder Paste Overprint on Thermal Pad Void Reduction*

Norman J. Armendariz, PhD, Raytheon, Andover, MA

Abstract

QFN- Quad Flat No-lead SMT-surface mount technology components continue to be increasingly used and also becoming smaller for applications further requiring a high level of thermal performance and reliability. QFN device thermal pad regions have been observed w/ excessive void densities >30% in area, which limits the thermal conductivity or performance of the device and often requires subsequent costly rework. Voids also become more dominant for smaller devices as the surface area of the thermal pad regions decrease, but voids may not correspondingly reduce in size or density. Using various reflow profiles, solder paste volumes and over-print values showed a statistically significant reduction of large voids and void density using the solder paste over print method. In addition, void formation and escape paths were demonstrated using x-ray imaging technology equipment that can be programmed to simulate an actual SMT surface mount technology reflow profile on a thermal platform or hot plate and provide real-time X-ray imaging recording the materials physical and void behavior.

Introduction

Quad-flat no-leads (QFN) device thermal pads have been observed with excessive void densities (>30%) which pose a serious risk to the reliability and functionality of the solder joint., as the presence of voids within the solder reduces the interface contact area for metallurgical bonding and thermal conductivity, that may cause components to overheat during electrical use or detach. Moreover, costly rework and production delays are often required to reduce the void density to tolerable levels.

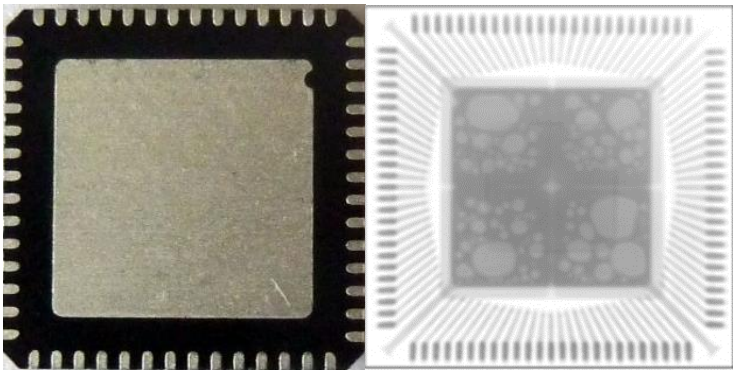


Figure 1. OM-optical microscopy view of QFN I/O and thermal pads (L) and X-ray image of QFN thermal pad exhibiting approximately 40% void area density in solder after SMT thermal reflow processing (R) [1].

Process Void Formation

During SMT-surface mount reflow assembly of QFNs to PCBs, voids originate from gaseous by-products caused by the solder paste flux reduction reactions with surface oxides on the PCB and solder spheres in the paste.

This reaction occurs at certain temperatures slightly before melting and for certain rates or times to enable metallurgical bonding in the formation of IMC-intermetallic compounds that create the solder bond with the QFN and PCB metallic interfaces.

These oxide reduction reaction by-products are mostly CO and CO2, but also other gaseous constituents evolve [2] where the presence of gaseous products indicates reactions are occurring, i.e., a lot of voids mean a lot of oxide reduction.

However, gaseous voids need to leave, but there is no easy path or insufficient time for the voids to escape the solder melt during reflow after being used, and remain entrapped within the solder or at the QFN / PCB interfaces after solidification.

Void Reduction Methods

1- SMT Reflow under Vacuum: Significant equipment investment and larger production floor foot-print, but did reduce QFN thermal pad voids ~60% (L). However, voids within BGAs tended to expand and could result in BGA bridging (R) [3]

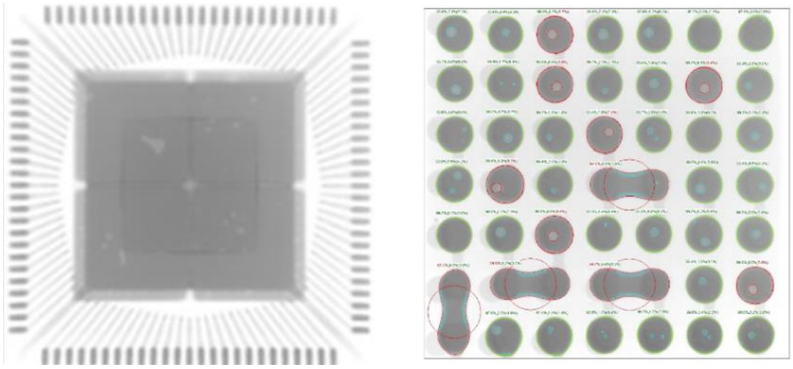


Figure 2. X-ray image of QFN MLF100 thermal pad region with little or no voids after vacuum processing (L) and a BGA device where voids expanded within some of the BGAs to connect to an adjacent BGA solder sphere (R).

2- SMT Reflow Profile / Flux Composition: Optimize the SMT RF profile and flux recipes for generating less volatile by-products / gases. However, would detail significant development and may impact other non-QFN components.

3- Void Reduction by Sweep Vibrational Stimulation: Reduces void formation by applying vibrational movements using a piezoelectric actuator applied to the PCB in the region where the QFN is reflowing. Risk that components could move during reflow. [4]

4- Overprint QFN I/O Pads: Low cost. Initial study showed a void density and largest single void reduction trend, with just a low-cost stencil modification, thus the focus of this investigation.

Thermal Pad Void Reduction Hypothesis:

AIM-Solder, T. O'Neil, 2017, published a method that showed overprinting solder paste onto the I/O pads of the QFN could reduce voids within the thermal pad. [5] Speculate that solder paste overprinted on the I/O pads melts before the thermal pad solder and lifts the QFN higher during reflow from the increased volume of solder paste on the I/O pads and creating a ceiling space for voids to egress. (C to D).

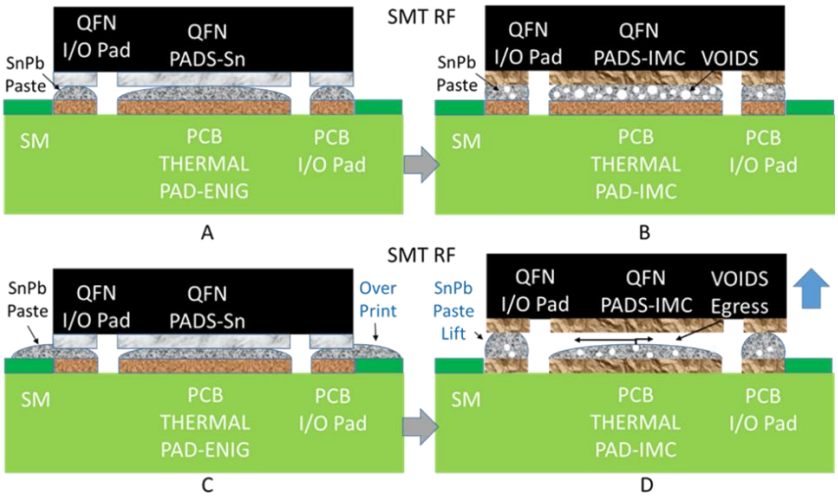


Figure 3. Current I/O pads not solder paste overprinted (A) with voids created during SMT reflow and eventually entrapped (B). I/O pads solder paste overprinted (C) lifting QFN, thus creating a ceiling during SMT reflow for voids to escape (D).

Test Vehicle PCB and QFNs

The test board was designed by the AREA Consortium specifically for void reduction studies and was recommended for next set of trials based on the smaller PCB size, with 2 different QFN sizes that are more centrally located within PCB area for real-time thermal imaging and are also daisy-chained for future electrical / reliability testing.

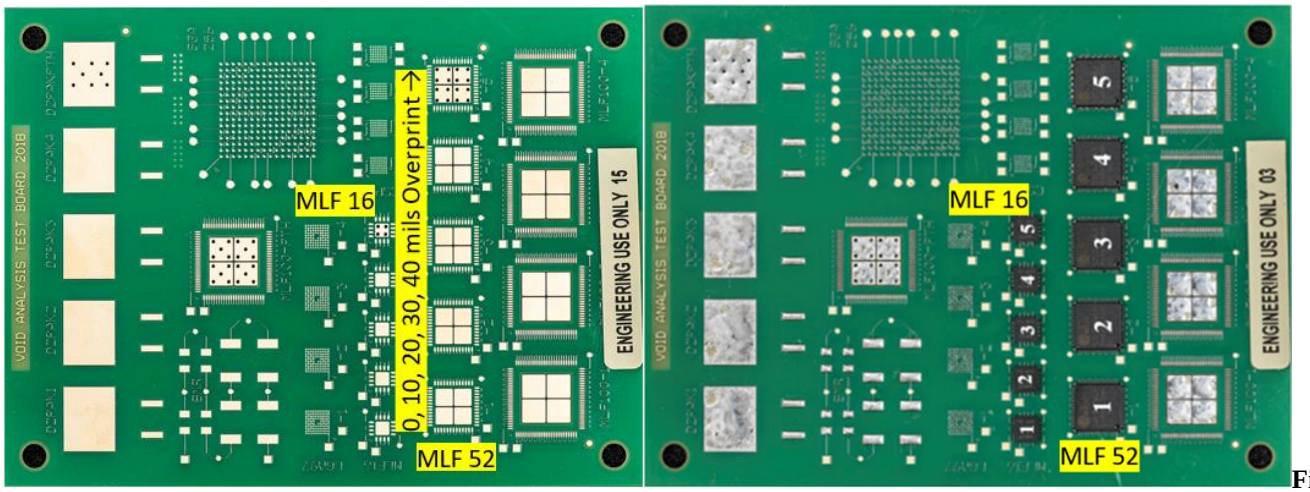
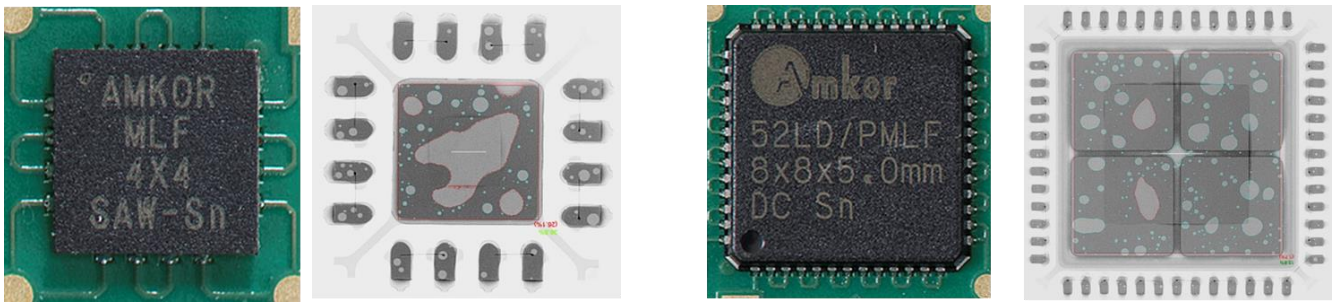


Figure 4. Test Vehicle 5x4" Bare ENIG-plated PCB to solder paste OP-overprint from 0, 10, 20, 30 and 40 mils on I/O pads (L) and QFNs MLF 16 and MLF 52 after SMT RF reflow (R).

QFN (Quad Flat No-leads) packages MLF 16 and 52 were SMT reflowed and evaluated to determine the effect of OP-over-printing solder paste on the QFN I/O pads for reducing the QFN thermal pad void densities and sizes measured by X-ray imaging methods.

Only three (3) stencil modifications were required to determine the effect of no print, over-print and accommodate THVs, and considered a flexible and low-cost method not requiring a process, solder / flux materials, or equipment change / upgrade.

In addition, real-time X-ray video imaging of void formation and behavior was performed using a hot plate to simulate a SnPb production SMT RF-reflow profile.



(L) **(R)**

Figure 5. QFN MLF 16, 4x4mm and X-ray Image (L). QFN MLF 52, 8x8mm and X-ray Image (R).

DOE Process and Analysis Flow

Evaluation followed a conventional SnPb SMT-surface mount technology assembly flow with samples taken off-line for certain measurements and analyzes. Test Vehicle PCB I/O pads were solder paste printed with different stencil configurations and I/O apertures sizes to OP-over-print along and beyond the length of the I/O pad, while maintaining the same width of the I/O pad.

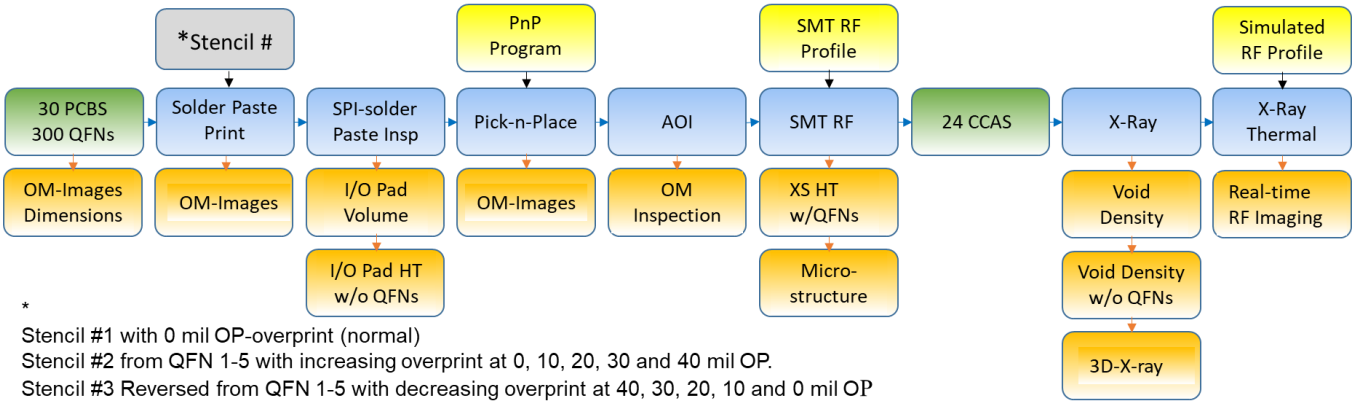


Figure 6. DOE Void Reduction Process and Analysis Flowchart**.**

Metrology & Analysis Methods

- SPI: Solder Paste Inspection: In-line measurement of solder paste volume after screen printing.
- OM: Optical Microscopy of test vehicles, bare PCB, QFN pads, before and after solder paste deposition and after SMT reflow.
- OM-XS: Cross-Section Analysis: QFN to PCB pad solder joint heights and microstructure after SMT reflow.
- OM-3D: QFN solder joint ht. after solder paste printing and after SMT reflow with and without QFNs placed.
- XRT-2D: QFN thermal pad void density and largest singular void measurements of QFNs with and out THVs.
- XRT-3D CT: Determine void interface locations in the QFN thermal pad solder-joint z-direction.
- XRT-Thermal Imaging: Real-time x-ray video imaging recording of QFNs under simulated SMT reflow profile thermal conditions to characterize void formation processes and void behavior.

QFN MLF Assembly Sequence:
Test Vehicle PCB I/O pads were solder paste printed with a stencil with increased I/O apertures sizes to over-print along the length of the I/O pad away from the QFN body and maintaining the same width of the I/O pad.
5 QFNs for each MLF 16 and MFL 52 on 10 PCBs had increasing overprints from 0, 10, 20, 30 and 40 mils. After solder paste printing, the QFNs were placed and then reflowed.
Then QFNs were 2D XRT x-ray transmittive measured for void density and largest void.
Separate samples were only solder paste printed (not SMT reflowed) and then taken directly to the X-ray machine for real-time thermal imaging video characterization under simulated SMT reflow conditions.
At certain points during the assembly process, samples were taken off-line as controls and / or practice samples or to have additional measurements performed, such as cross-sections for stand-off heights, microstructure characterization, as well as separate solder paste height measurements with and without QFN components after reflow.

QFN MLF 16

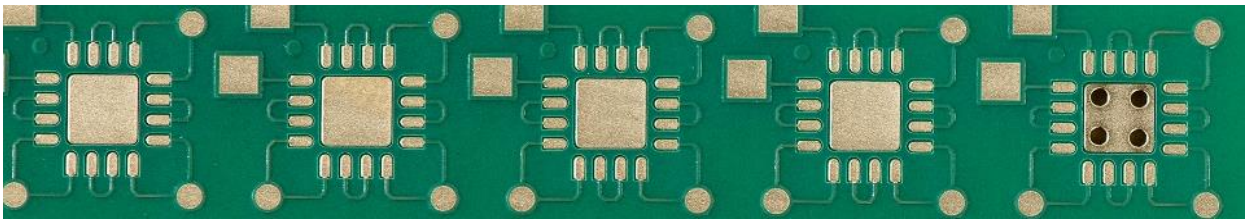


Figure 7. PCB: MLF 16-QFNs 1-5. All I/O PCB ENIG Pads same size.

Figure 8. STENCIL: I/O APERTUREs w/ increasing overprint sizes 0, 10, 20, 30, and 40mil (L to R).

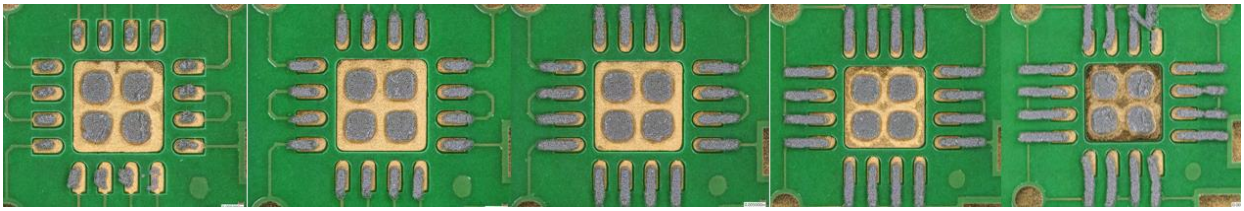


Figure 9. AFTER SOLDER PASTE DEPOSITION on PCB: w/ OP: 0, 10, 20, 30, and 40mil (L to R).

Figure 10. AFTER QFN 16 PLACEMENT AND SMT REFLOW: MLF 16-QFNs 1-5 SMT reflow attached to PCB.

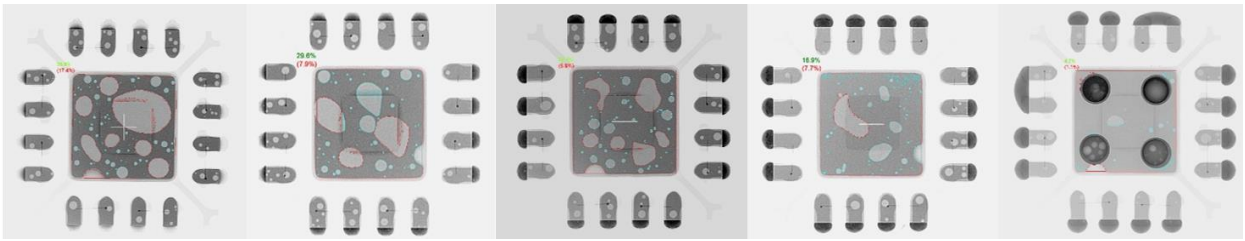


Figure 11. XRT IMAGE. Void Density and Largest Void Size decrease w/ increased over-printing (L to R).

QFN MLF 52

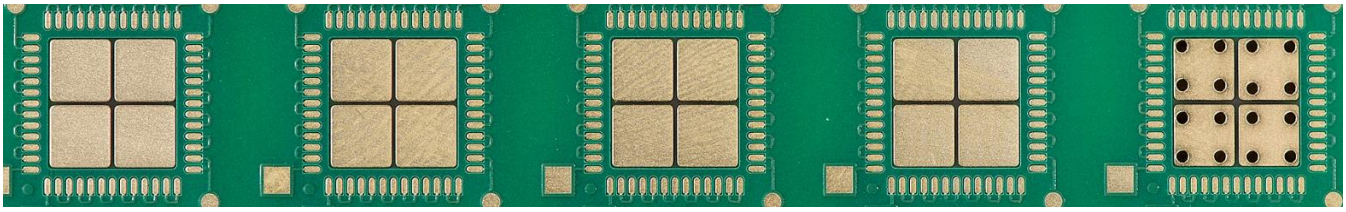


Figure 12. PCB: MLF 52-QFNs 1-5. All I/O ENIG Pads same size

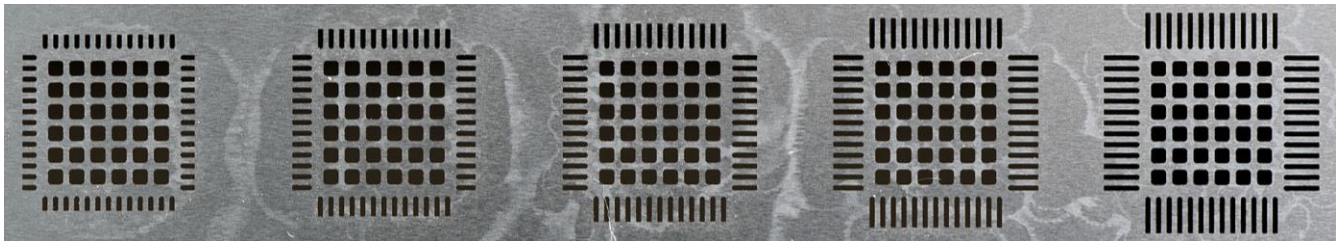


Figure 13. STENCIL: I/O APERTUREs w/ increasing overprint sizes 0, 10, 20, 30, and 40mil (L to R).

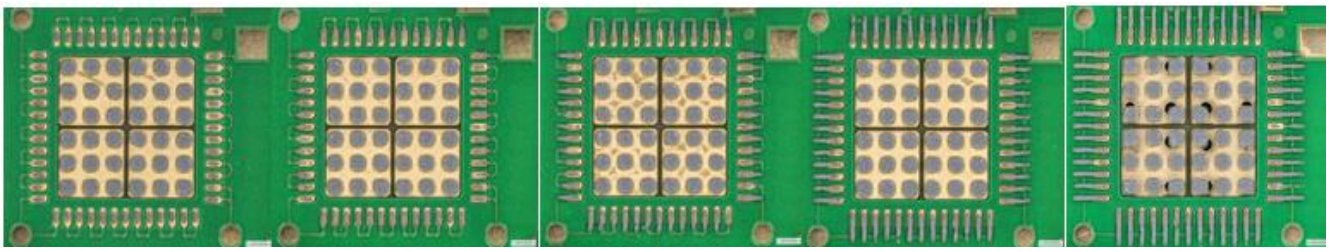


Figure 14. AFTER SOLDER PASTE DEPOSITION on PCB: w/ OP 0, 10, 20, 30, and 40mil (L to R).

Figure 15. AFTER QFN 52 PLACEMENT AND SMT REFLOW: MLF 52-QFNs 1-5 SMT reflow attach to PCB.

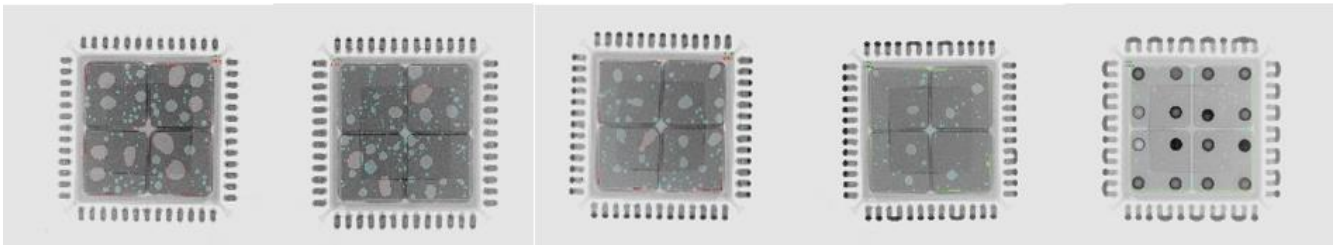


Figure 16. XRT IMAGES. Void Density and Largest Void Size decrease w/ increased over-printing (L to R).

Solder Joint Interface Characterization

Cross sections were performed to characterize the solder microstructure, interface and measure the stand-off heights with respect to overprinting amounts and correlate to final stand-off heights confirming degree of lift.

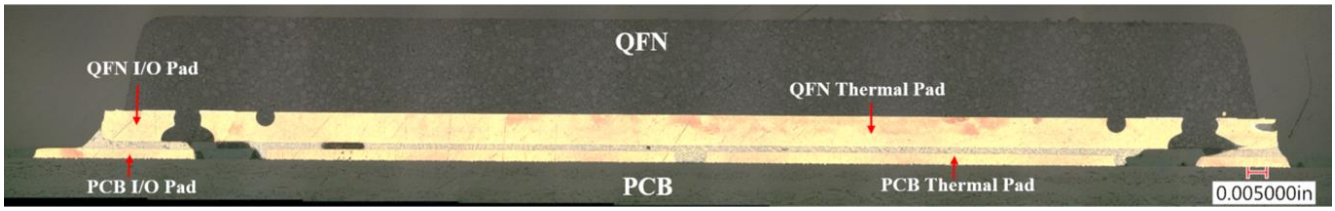


Figure 17. XS Cross Section of QFN MLF 52 (10 mil OP-overprinted) after SMT RF on PCB showing interface features.

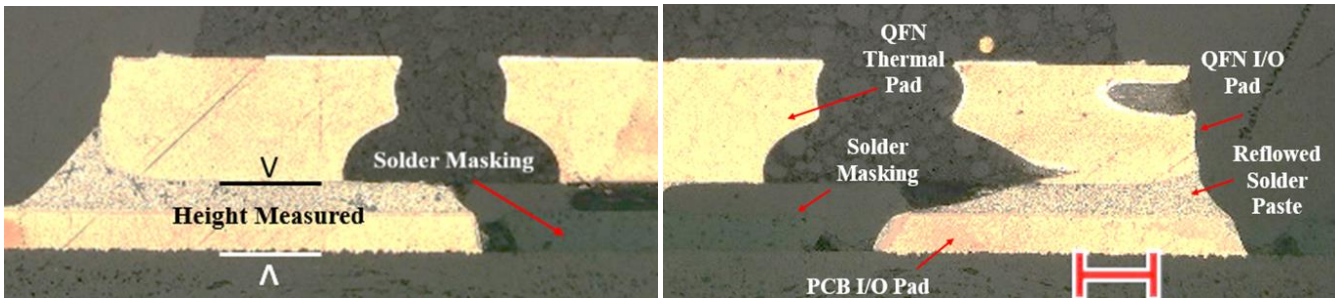


Figure 18. Height measured from the PCB surface to QFN bottom (L) Closer view of I/O pad regions (R).

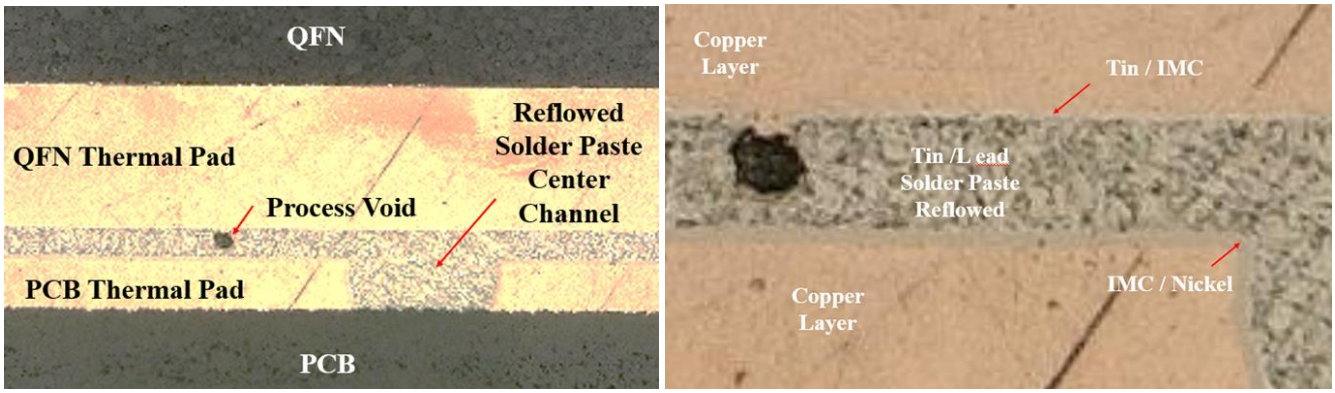


Figure 19. Closer views showing a process void (L) and the solder-joint microstructure well-formed at both the QFN and PCB thermal pad with IMCs- intermetallic compounds forming metallurgical bonds at their respective interfaces (R).

Solder Paste Height after Printing: OM-3D

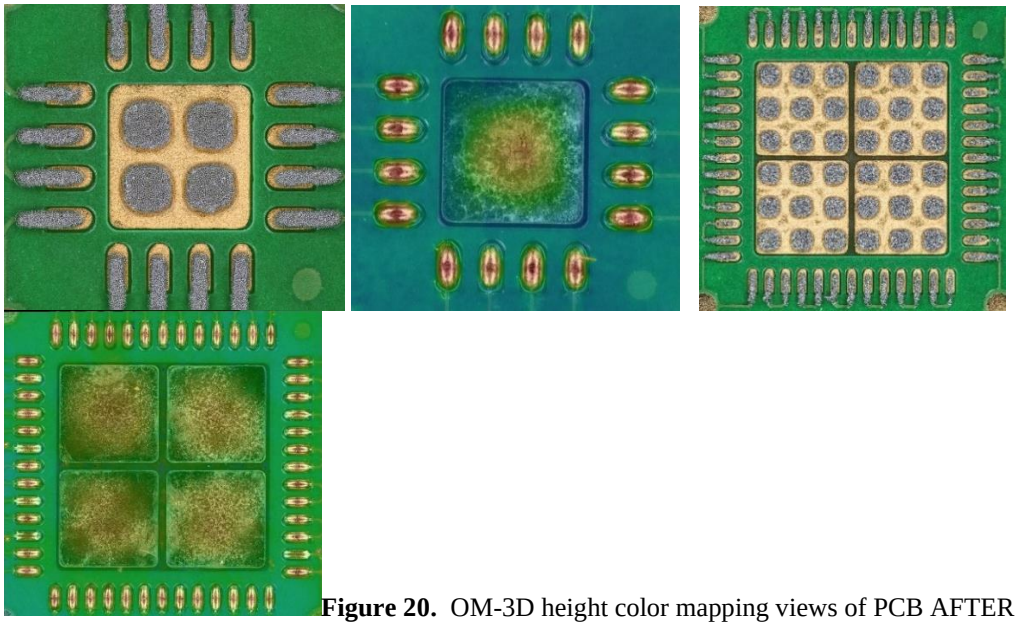


Figure 20. OM-3D height color mapping views of PCB AFTER SP-solder paste and AFTER RF-reflow w/o QFNs MLF 16 (L) and MLF 52 (R) placed. 20 mil overprint samples.

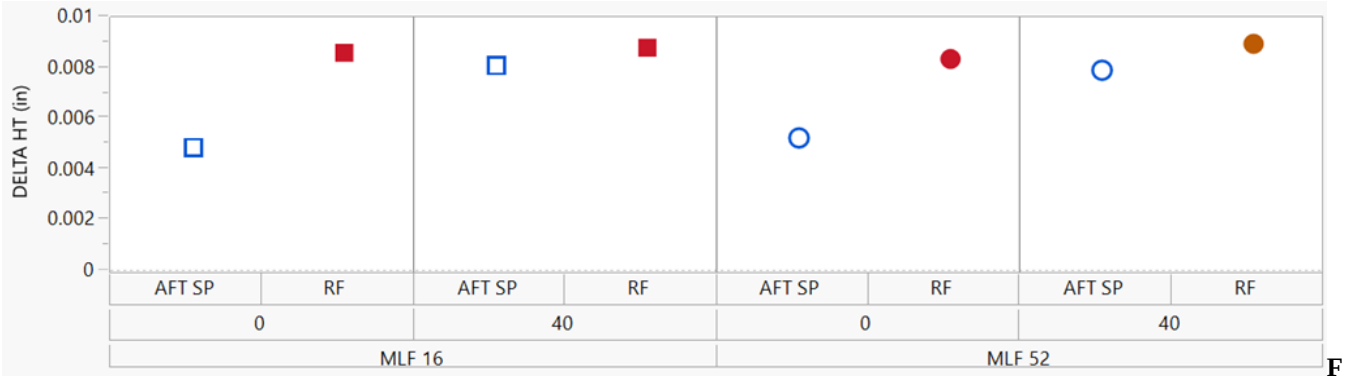


Figure 21. OM 3D Solder Paste Ht. AFTER printing and AFTER SMT Reflow without QFNs placed. 0, 40 mils OP. Both MLF 16 and MLF 52 solder paste heights increased after RF-reflow but increased more at 0 mil OP than at 40 mil.

Solder Paste Volume after Printing: SPI

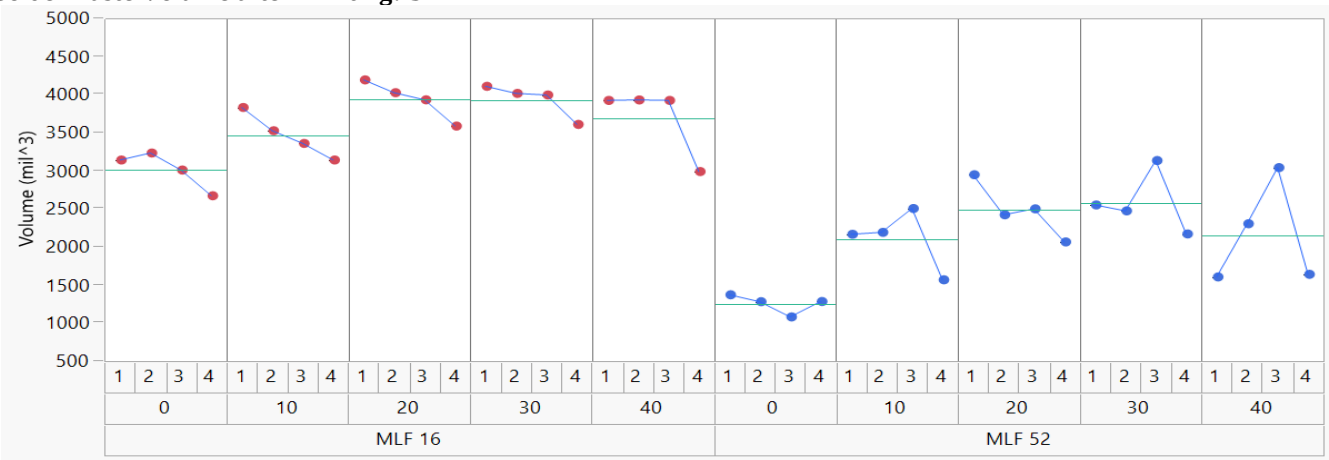


Figure 22. SPI- solder paste inspection tool measurer volume at four (4) I/O pad corners of each QFN MLF type with THV through-hole vias at 40 mil OP-overprint. Solder paste volume increased with increasing OP, with a QFN "tilt" observed from the solder paste volume differences at QFN corners.

Stand-off Heights of QFNs after SMT RF: XS

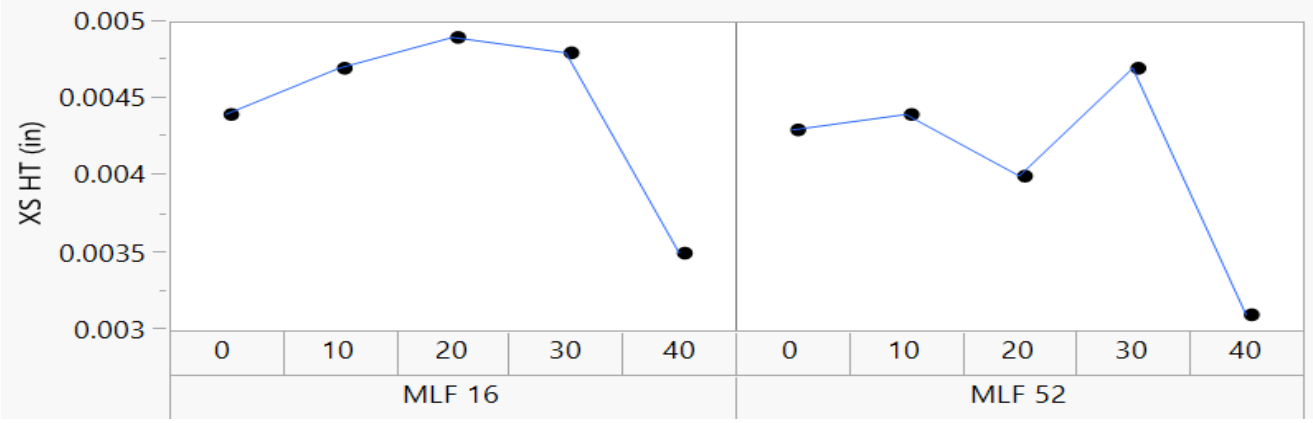


Figure 23. XS- cross-section QFN stand-off heights of both MLF 16 and 52 increased with increasing OP-Overprint. QFNs at 40 mil OP ht. decreased on THV-through-hole vias in thermal pad region.

Void Density with THV at 0 Overprint: Stencil 1

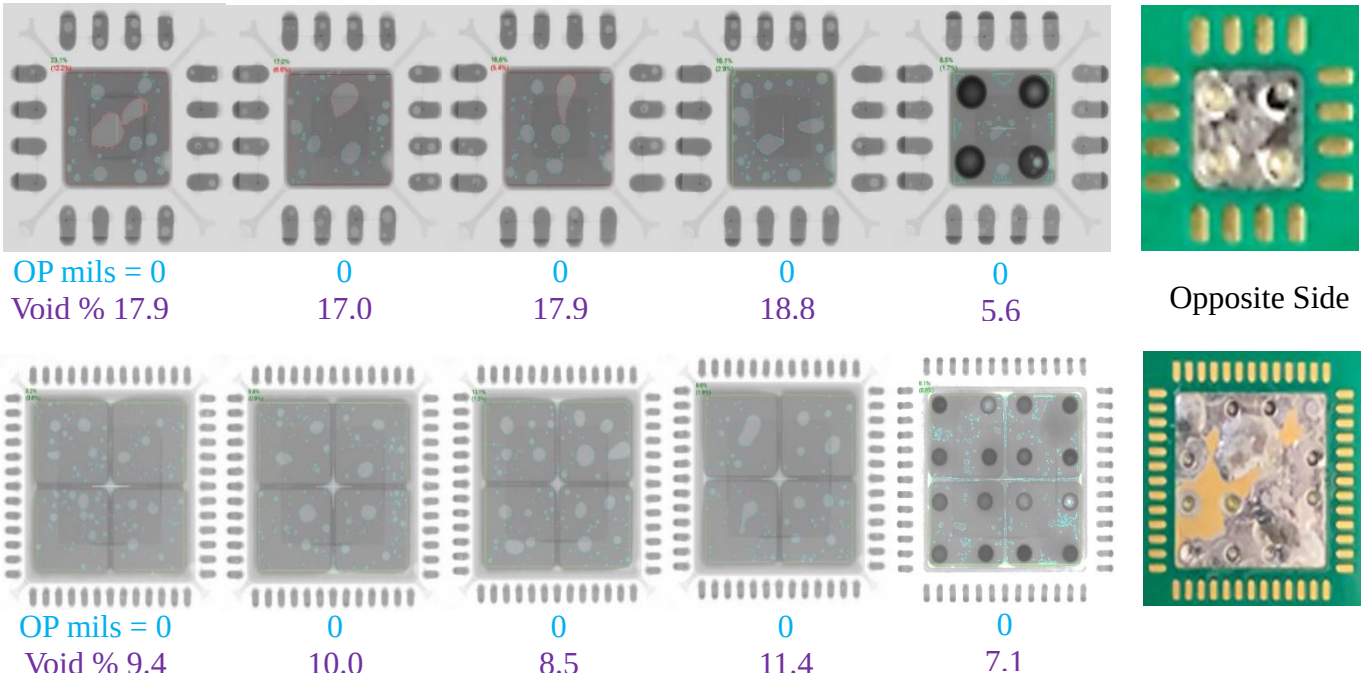


Figure 24. Control QFNs MLF 16 (top) and MLF 52 (bottom) 1-5 with Stencil #1 with 0 or zero OP-overprint and THV-through-hole vias (last QFN on right) where void density decreased, but solder wicked to the opposite side.

Void Density and Largest Single Void Analysis with THV at 40 mil Overprint: Stencil 2

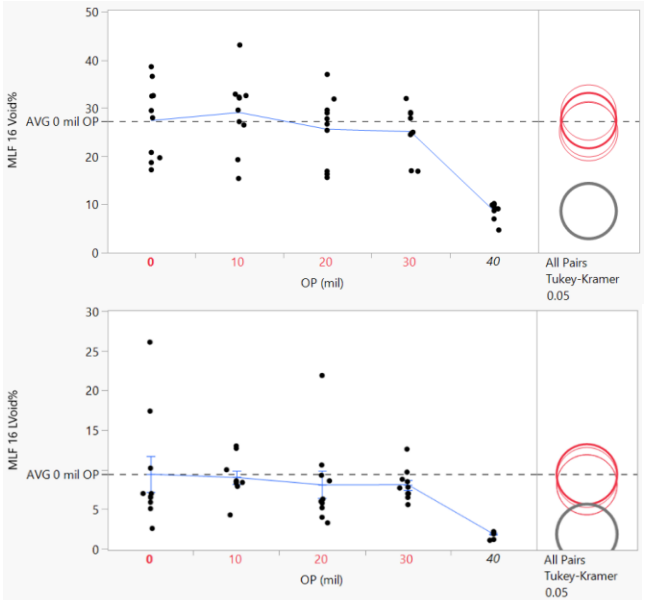


Figure 25. MFL 16 Void Density (L). MLF 16 Largest Void (R. THVs significantly reduced void density and largest void.

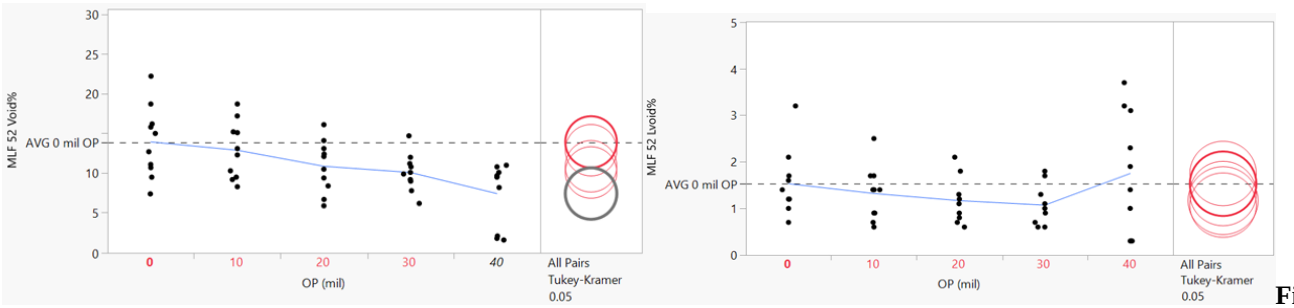
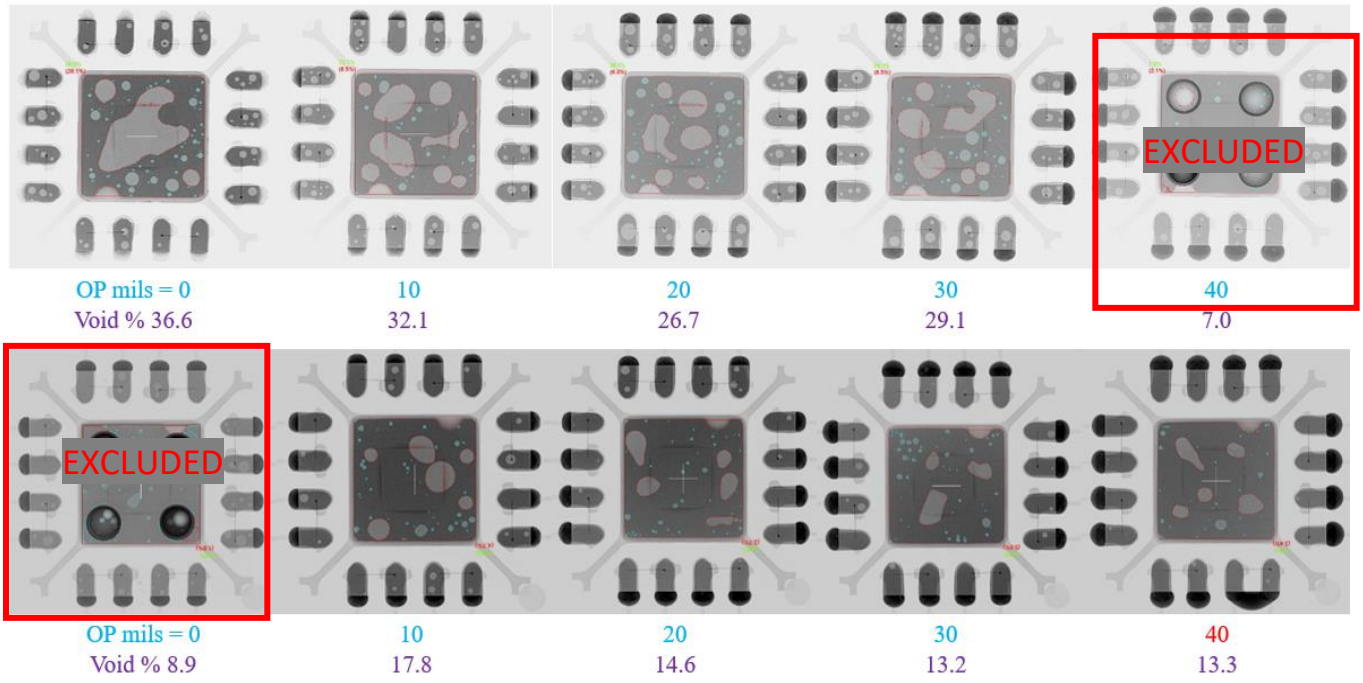


Figure 26. MFL 52 Void Density (L). MLF 52 Largest Void (R).

Void Density and Largest Single Void Analysis with Overprint: THVs Excluded: Stencil 3

MLF 16 (top panel)



MLF 52 (bottom panel)

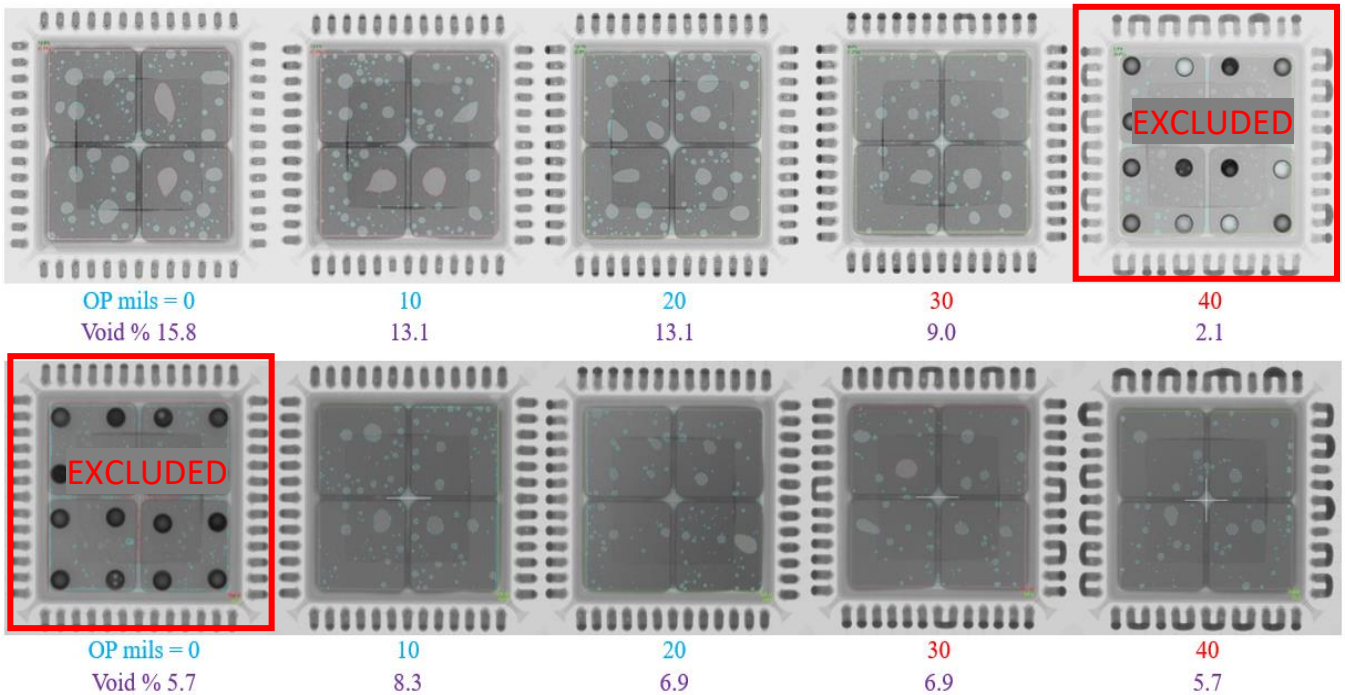


Figure 27. MLF 16 (top panel) and MLF 52 (bottom panel). QFN thermal pad void density and largest singular void on QFNs without THVs. This was accomplished using 2 stencils, stencil #2 with 0-40 mil overprints and stencil #3 with 40-0 mil overprints reversed. The data from QFNs with THVs were excluded and replaced with QFNs at same OP without THVs.

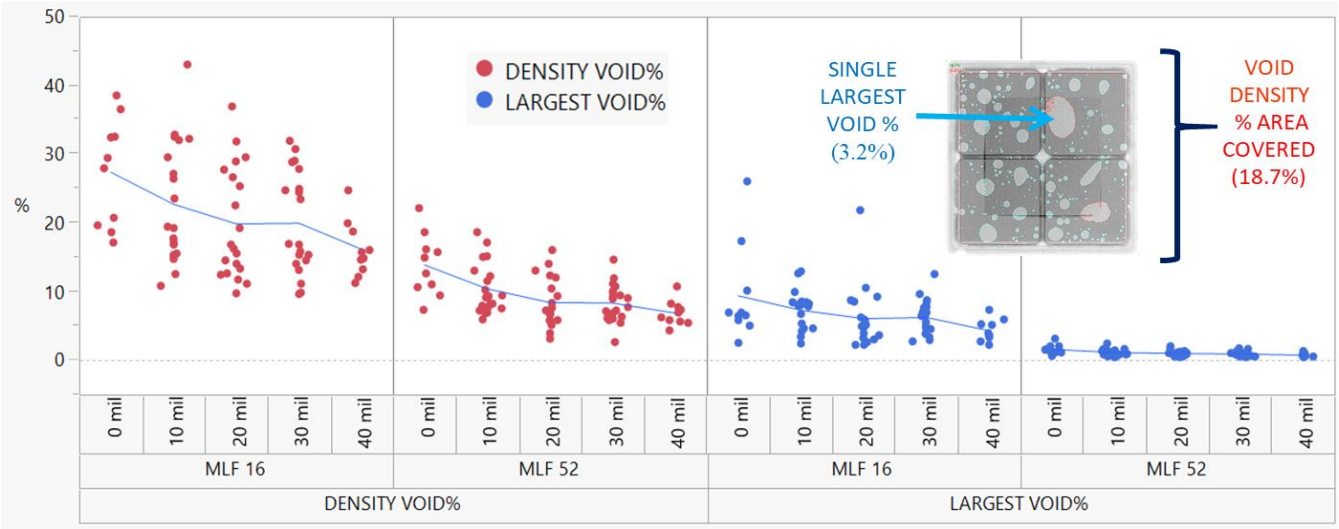


Figure 28. When excluding the THV-through hole vias, both QFN Types showed ~ 50% void density reduction (L) and ~ 50% reduction in the largest single void (R) in the thermal pad region when solder paste OP-overprinted to 40 mils.

Real-time X-ray Thermal Imaging

X-Ray imaging performed to observe and video record void formation and reduction processes of the QFN solder joint thermal pads using a hot plate programmed to simulate the SMT RF profile. Samples were solder paste printed, then taken directly to the x-ray machine for video recording void processes. Video recording showed the process voids formed just before the QFN I/O solder spheres melted, and which melted before the QFN thermal pad solder spheres. Process voids often combined and showed tear drop shapes that moved and escaped towards the thermal pad edges, but also disappeared in thermal pad centers indicating a "ceiling" path escape.

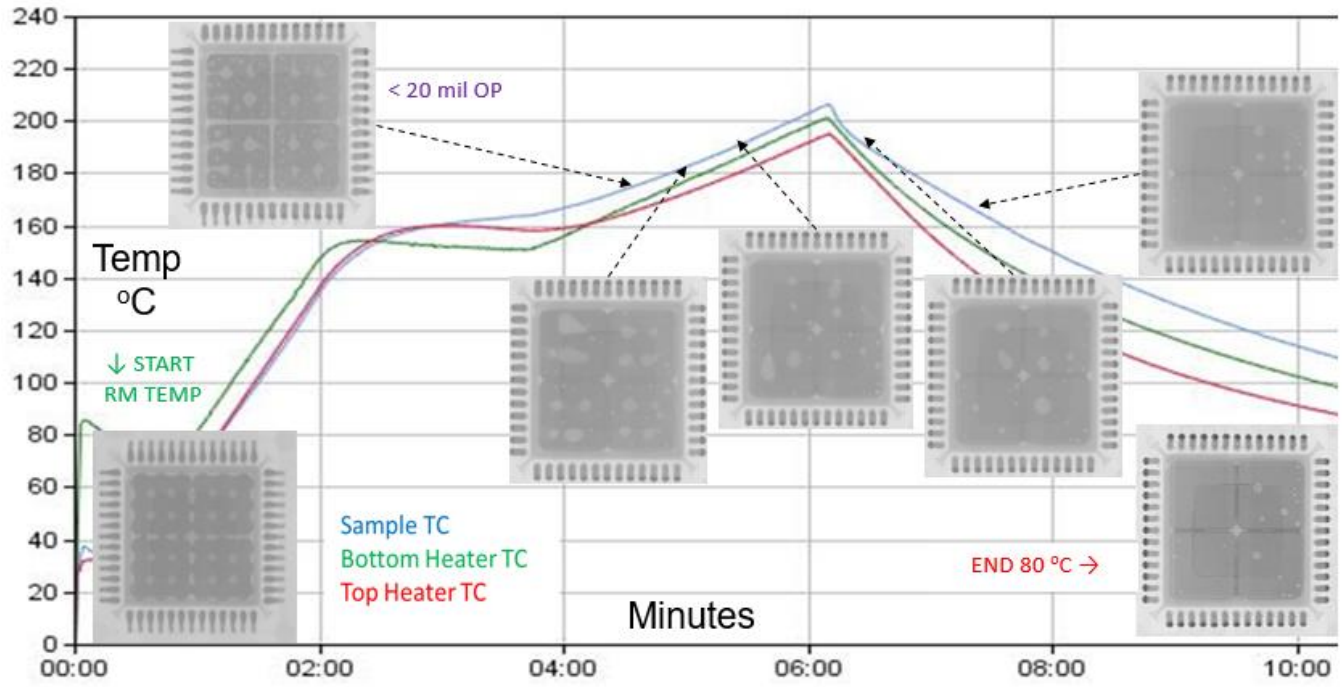


Figure 29. Simulated SMT reflow thermal profile showing hot plate and sample temperatures with X-ray snapshot images taken at specific intervals from X-ray real-time video of QFN MLF 52 at 20 mil OP- overprint showing when, where process voids form and, in what shape.

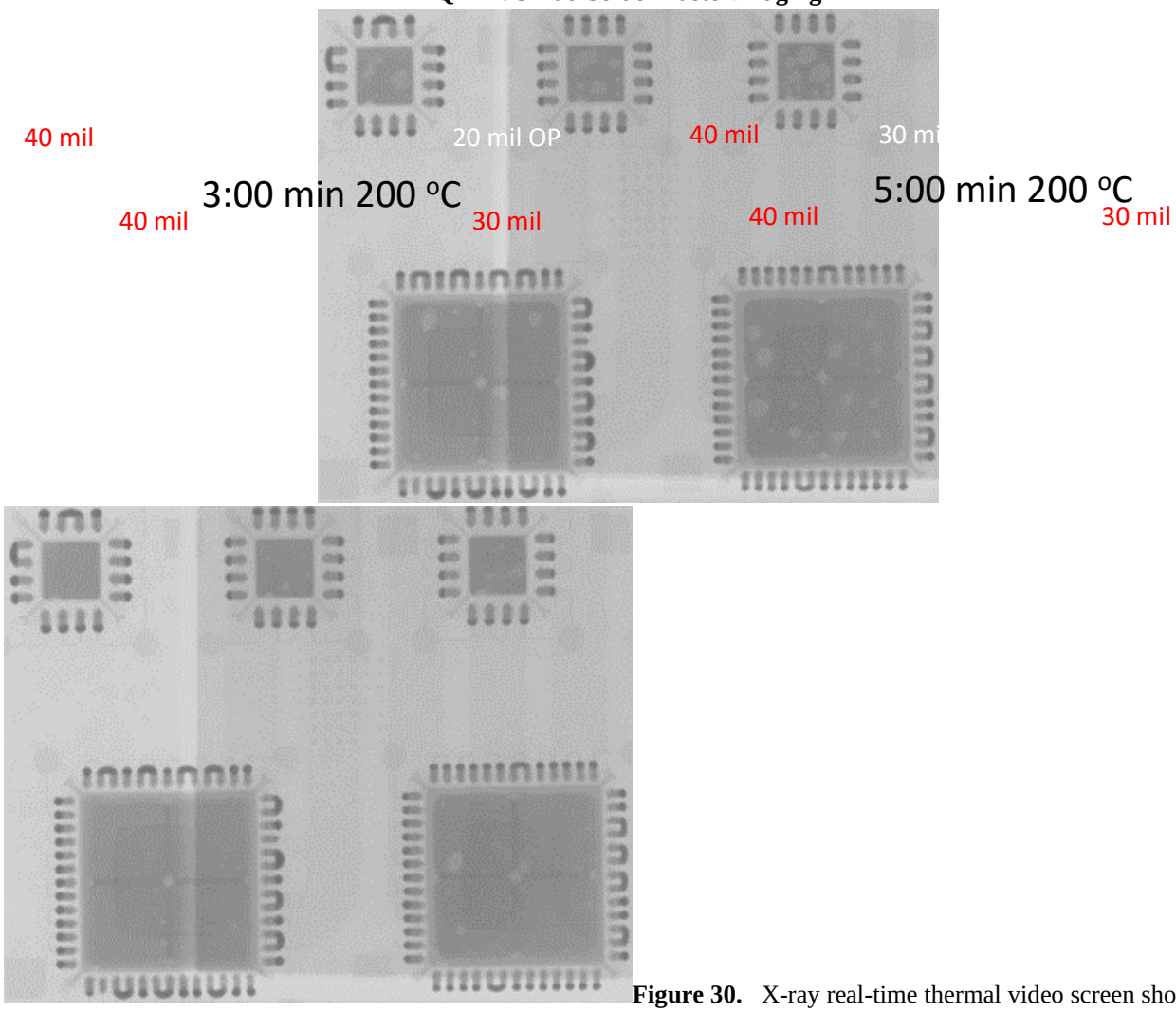
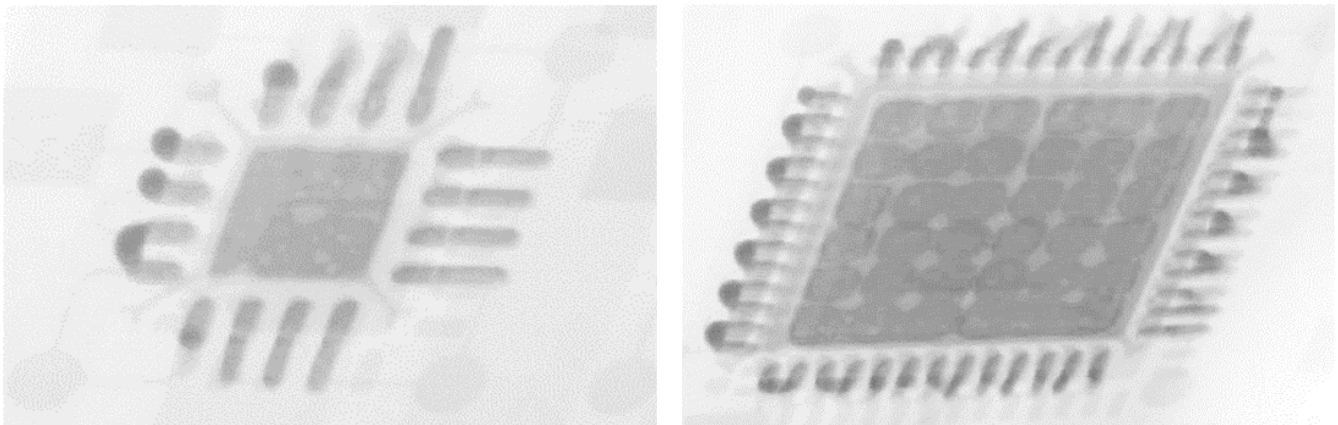


Figure 30. X-ray real-time thermal video screen shots show QFN MLF 16 (top) and QFN MLF 52 (bottom) process void density decreasing with increasing OP-over print from 20 to 40 mils before (L) and after reaching peak temperature (R). However I/O pad solder bridging (red) was observed with increasing OP as I/O pad solder spheres started to melt.



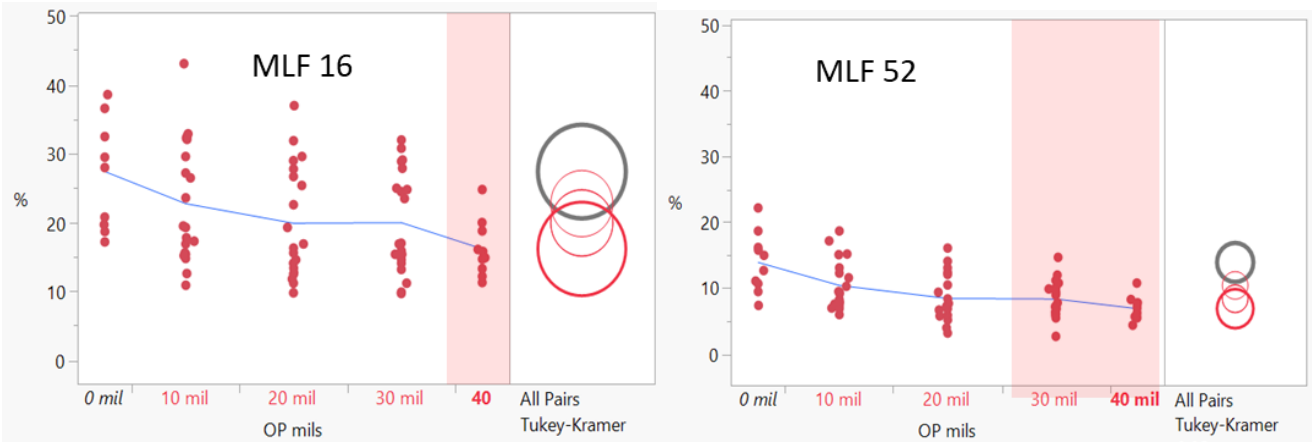


Figure 31. Real-time X-ray video snapshots show process voids already forming and at the moment I/O pads solder melts, the I/O pads solder melts and bridge before the solder melts on thermal pad on MLF 16 at 40, and MLF 52 at 30 & 40 mil OP.

3D X-ray CT Imaging

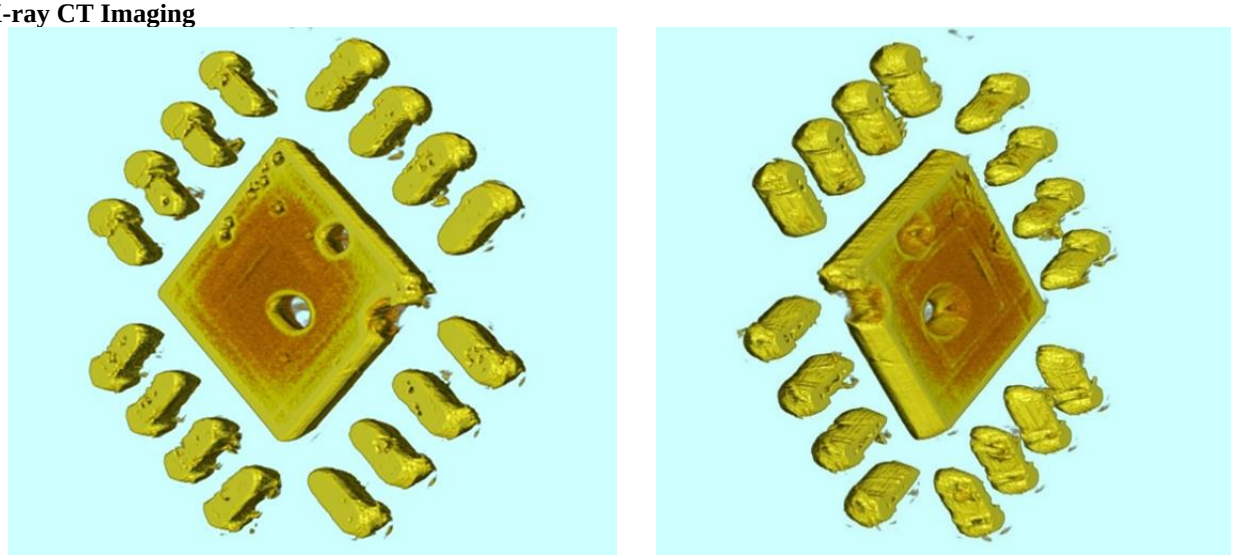


Figure 32. 3D CT-computed tomography image of a QFN pad interface to solder (L) and solder to PCB interface (R) which showed voids tended to locate near or closer to the QFN interface (L).

Summary and Conclusions

DIMENSIONS→ QFN TYPE ↓	Pitch (in)	I/O Pad X (in)	I/O Pad-Y (in)	I/O Edge SPACING (in)	I/O Pad Area (in2)	T-Pad X (in)	T-Pad-Y (in)	T-Pad Area (in2)
MLF 16	0.025	0.030	0.011	**0.012**	0.00034	0.087	0.087	0.0074
MLF 52	0.020	0.032	0.010	**0.010**	0.00030	0.23	0.23	0.053

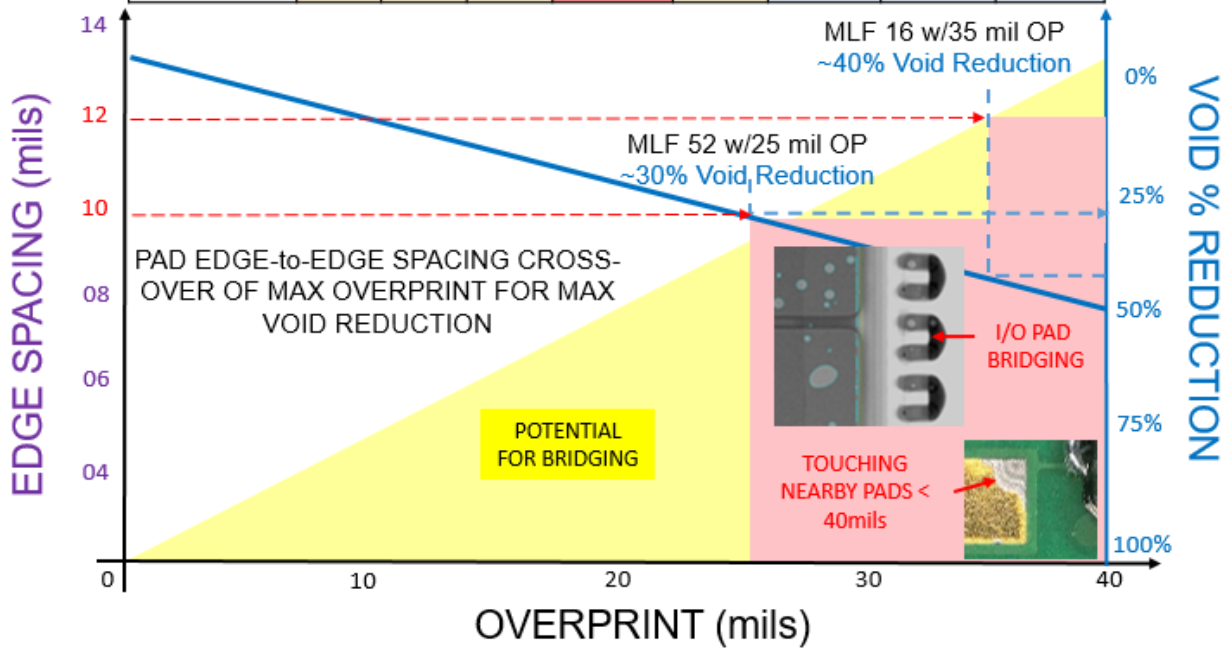


Figure 33. QFN I/O pad solder paste overprint limited by the pad edge-to-edge proximity. It is not clear if the daisy-chain "looped" Cu circuitry underneath soldermask may have contributed to I/O pad solder bridging.

- Solder paste over-printing on QFN I/O pads reduced the void density and largest voids ~ 50% on both QFN MLF 16 and 52 thermal pads at 40 mil OP.

- QFNs with THVs-through-hole vias showed significantly less voids, but solder paste "wicked" through to other side.

- Solder joint bridging was observed at 30, 40 mils for QFN 52 and QFN MLF 16 at 40 mils overprinting. Not clear if the daisy-chain "looped" Cu circuitry underneath soldermask may have contributed to I/O pad solder bridging by providing a thermal path for each I/O pad solder paste print to follow towards each other.

- Video images showed the process voids formed just before the I/O solder spheres melted, which melted before the thermal pad solder spheres.

- Process voids formed tear drop shapes that moved and escaped towards the edge and also disappeared in thermal pad centers indicating a ceiling path escape.

- Recommend solder paste over-printing for QFNs that require thermal pad void reduction, but taking into account the limitations of QFN I/O pad edge-to-edge spacing and distance from nearby pads or components.

***** This document does not contain technology or Technical Data controlled under either the U.S. International Traffic in Arms Regulations or the U.S. Export Administration Regulations

Acknowledgements
Mike Jansen, Nicolas Casilli (NEU), George Georgacopoulus, Nenad Opijac, Louis Chin, Callie Schadt, William Themelis, Joel Pollack, Jonathan Touchette, Colin Smith, Armagan Sezer, William Themelis, Joe Sarcione, Colin Smith, Chuck Smith III, Anthony Gironda (NEU), Tim O'Neill (Aim Solder), David Vicari (AREA)

References

[1] K. Sweatman, T. Nishimura, K. Sugimoto, and A. Kita, "Controlling Voiding Mechanisms in the Reflow Soldering Process," Nihon Superior Co., Osaka, Japan. Accessed on: June 12, 2018. [Online].
[2] Tolla, B. (2017). Impact of reflow and cleaning processes on the electrochemical activity of flux residues. SMTA-SMART Group Cleaning and Coating Conference. Amsterdam, Netherlands. SMTA, Minneapolis, MN.

[3] M. Meilunas, "Solder Joint Void Formation in LGA and QFN Assemblies," Universal Instruments, Conlkin, NY, 2017.

[4] V. Rawinski with the Kurtz Ersa Group "Void Reduction by Sweep Stimulation of PCB Substrate."

[5] T. O'Neill, "Aperture Design to Minimize QFN Voiding," AIM Solder, June 7, 2017.

Author's Biography

Norman Armendariz is an Engineering Fellow at Raytheon responsible for materials engineering design, materials analysis, process equipment development, production support and technology roadmaps associated with the manufacturing of CCA- circuit card assemblies used in missiles, smart munitions, ground based radars, and mobile sensors across multiple US and international sites. Norm has over 25 years of industrial experience, having worked for LTV, Lockheed/NASA, Motorola, Intel, Texas Instruments and American University. He holds an interdisciplinary PhD in Chemical Engineering from New Mexico State University, MS in Materials Science Engineering from the University of Illinois at Urbana-Champaign, and BS in Metallurgical Engineering from Colorado State University, with 9 US patents and 29 peer-reviewed publications.