The Effect of Board Design on the Drop Shock Performance of Lead-Free Solder Alloys

Saddam Daradkeh, Elizabeth Gainey, Mohamed El Amine Belhadi, Abdallah Alakayleh, Menghong Wang, John Evans, Sa'd Hamasha
Auburn University
AL, USA
smh0083@auburn.edu

Michael Osterman
University of Maryland

John Blendell
Purdue University

ABSTRACT
Tin-Silver-Copper (SAC) solders are widely recognized as superior alternatives to traditional tin-lead solders in microelectronics packaging due to their good mechanical properties. The frequent occurrence of drop events in portable electronic devices necessitates the assurance of board-level drop shock reliability to maintain optimal device performance and extend electronic device lifespan. This paper aimed to investigate the impacts of printed circuit board (PCB) design, including the PCB thickness and solder mask opening, on the fatigue performance of lead-free solders. Each test vehicle includes one of two component types: CABGA192 and MLF32, assembled using SnAgCu solder paste with an Organic Solderability Preservative (OSP) surface finish. Drop tests were performed at two acceleration levels—1500G and 3000G with a pulse width of 0.5 seconds. A predictive model for drop life was developed for each test condition across various energy levels. The results indicate that thicker PCBs typically demonstrate higher drop shock reliability due to their increased mechanical strength. Additionally, solder mask define opening (SMD) boards have shown much better reliability than Non-solder mask define (NSMD) boards, regardless of board thickness or component type. A detailed failure analysis was also conducted to identify the failure modes.

Key words: solder joint, drop shock, PCB design, CABGA, MLF, intermetallic compound, SAC305, aging.

INTRODUCTION
In recent years, there has been an increase in research on lead-free solders as an alternative to standard Sn-Pb due to concerns about the hazards that lead poses to the public. Research is being done to find a suitable replacement by understanding the mechanical properties of various solder alloys, with much work being done on tin-silver-copper (SAC) combinations. Extensive reviews of databases from the Surface Mount Technology Association (SMTA) and the Institute of Electrical and Electronics Engineers (IEEE) show a great deal of research has been conducted on solder materials such as Sn-Pb and SAC305, with additional studies on other SAC combinations such as Sn100C, SAC105, and SAC405 [1, 5]. Mechanical shock can occur from impact, such as a collision or drop, or from a higher energy event, such as a sonic boom. Shock events can be analyzed in both time and frequency domains, with the Shock Response Spectrum (SRS) serving as a valuable graphical tool in the frequency domain to represent system responses to shock inputs [1, 2]. Steinberg's comprehensive discussion on shock environments provides foundational insights into shock characterization and its effects on electronic systems. Analyzing the effects of mechanical shock is essential as these events often lead to material failures, including fractures in solder interconnections, printed circuit boards (PCBs), copper traces, and components [2].
Studying the various causes for failure mechanisms also provides insight into other component failures, such as those in the PCB, copper traces, and other parts of the board being put under various stressors. The failure mode is influenced by board design, material, and construction factors. The most common failure sites are at the solder-copper pad/trace interfaces and epoxy composites of the PCB. Cracking tends to initiate where shock-induced stress exceeds material strength, with crack propagation depending on the material's fracture toughness [5, 6]. For PCBs, flexing is a primary driver of mechanical shock-induced failures. The relative motion between the board and mounted components during flexing can lead to failures in components, interconnections, or the board itself. As described by Liu, Kuan-Ting et al. [7], when the thickness of the PCB is increased by adding more layers to the composite, the maximum von-mises stress on the PCB surface decreases. While it is known that flexing causes board failure, more research needs to be done on the effects of board thickness on failure modes in PCBs. Failures in a solder joint can occur in the copper trace, the intermetallic layer, or the bulk solder. In efforts to minimize the failures in the intermetallic regions, research is being done on the shape of the mask of the solder pad and the effects each has on the

failure modes – either solder mask defined (SMD) or non-solder mask defined (NSMD). However, it has been shown that SMD causes more degradation of the copper pad than NSMD [8]. Yoshida et al. [9] build on this idea and add that SMD pads cause the component to have a decreased fatigue life compared to NSMD pads. Ma and Lee [10] outline that NSMD can withstand thermal cycling better than SMD pads. It is also added that more testing needs to be done to compare failure mechanisms under mechanical stress cycling. The mechanical behavior of Sn alloys bonded to copper substrates is complex [11, 12, 13].

Moreover, at low strain rates, the material shows predominantly ductile deformation, whereas high strain rates lead to brittle fracture due to insufficient stress relaxation and the strength of the Intermetallic Compound (IMC) layer. The thickness of the IMC layer plays a significant role in the failure mode of the solder joint [14]. Failures can occur in the bulk solder or at the solder-copper pad interface, with differences observed between copper-tin and nickel-tin intermetallic. Pad cratering, a failure mode involving cracking or breaking beneath the copper pad, and copper trace failure due to mechanical cycling and stress concentration are also discussed. Notably, pad pullout and cratering may indicate issues with board laminate selection or formation processes, particularly when transitioning to Pb-free solders [15].

Another property affecting solder properties and mechanical shock performance is aging. Elevated temperature aging studies, such as those by Date et al. [16] and Ahat [17], reveal transitions in fracture modes from ductile to brittle with prolonged aging. Research by Mattila et al. [18] and Belhadi et al. [19] highlights variations in performance under mechanical shock and thermal cycling for different Sn-Ag-Cu solder compositions. There have been observations showing how aging also affects the intermetallic layer in the solder joint. Akkara et al. [20] discuss how specific compounds form in the intermetallic layer after SAC solder alloy reflow – Sn dendrites, Ag_3Sn, and Cu_6Sn_5. Lall and his team [21, 22, 23] have further demonstrated the dramatic effects of strain rate and aging on solder properties, highlighting the need for continued research in this area.

However, after surveying the available literature, there is a need for more research on the reliability of electronic packages using lead-free solders. Accordingly, the following sections seek to develop a better understanding and fill the gap by studying the effects of mechanical shock on electronic packages with SAC305 solder. Both CABGA and MLF package types are considered. The effect of board thickness, SMD versus NSMD on board/package life are explored for each package type.

EXPERIMENT SETUP, EQUIPMENT AND PROCEDURE

A. Test Vehicle and Test Matrix

This study references JEDEC standards (JESD22-B111A) and focuses on testing two types of components. The first component type tested is CABGA192 with a 0.8 mm pitch and a 14 mm body, while the second one is MLF32 with 0.65 mm pitch and 7 mm body. The test board is constructed from high-temperature FR4 glass epoxy laminate. FR4 is recognized for maintaining its mechanical and electrical insulation properties in dry and humid conditions, with a glass transition temperature of 170 °C. The board dimensions are either 76 mm x 76 mm x 1 mm or 76 mm x 76 mm x 2.3 mm. It consisted of six layers and was equipped with either solder mask-defined pads or non-solder mask define pads with OSP surface finish. The experiment utilized a daisy-chain configuration to interconnect the solder joints, and the test vehicle, as shown in Figure 1, was assembled with the component. The board design incorporated five monitoring pads to monitor five different daisy-chain circuits: four (C1, C2, C3, and C4) were designated to monitor the corner joints (two joints in each corner), which typically experience stress concentration during drop events. The fifth pad (S1) monitors the other remaining joints. The testing condition of CABGAs included a peak acceleration level of 1500 G and a pulse width of 0.5 ms, while they included a peak acceleration level of 3000 G with 0.5 ms pulse width MLFs. SAC305 alloy was used as a tested solder joints alloy containing 3% Ag and 0.5% Cu.

In this study, a total of 160 boards were subjected to a drop shock test. These 160 boards were divided into 80 CABGA192 components and 80 MLF32 components. One surface finish, 2 board thicknesses, and 2 mask defines states were used, as illustrated in Table 1.

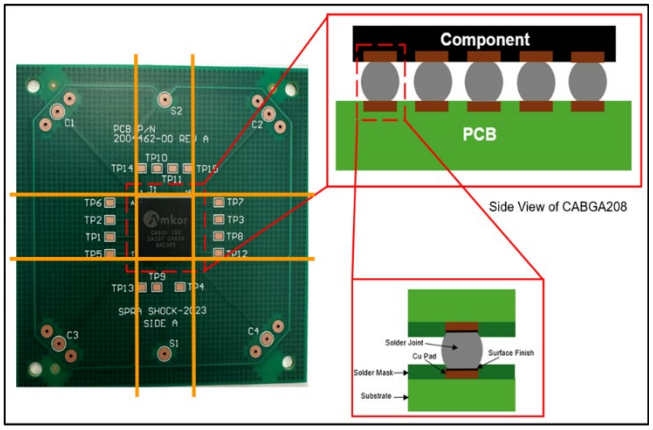


Figure 1: CABGA192 test vehicle, solder joints and the cutting path.

Table 1: Test Matrix

Board Design (Component)	G-Level	Board Thickness (mm)	Mask Define	Sample Size
CABGA192	1500	1	SMD	20
CABGA192	1500	1	NSMD	20
CABGA192	1500	2.3	SMD	20
CABGA192	1500	2.3	NSMD	20
MLF32	3000	1	SMD	20
MLF32	3000	1	NSMD	20
MLF32	3000	2.3	SMD	20
MLF32	3000	2.3	NSMD	20

B. Equipment

The Lansmont Model 23 drop shock test system was employed for the experiment, as illustrated in Figure 2. This system is designed to handle drops either automatically or manually via its release mechanism. The test boards undergo free-fall drops, allowing them to fall onto a rigid or semi-rigid surface. This dropping tower can generate accelerations of up to 5000 G and accommodate payloads weighing up to 80 lbs. It also supports pulse durations as short as 0.25 ms and can reach up to 32 feet per second velocities. The drop shock system is anchored by a seismic base constructed from cast iron and fitted with dampers to control vibrations. An aluminum horizontal fixture is secured to the shock table, where the test boards are placed on top of an aluminum drop plate. The shock table is elevated along guiding rods to a predetermined height during testing. Upon reaching this height, the shock table is released, causing it to fall and impact the base, which is covered with a felt cloth to generate the desired shock pulse.

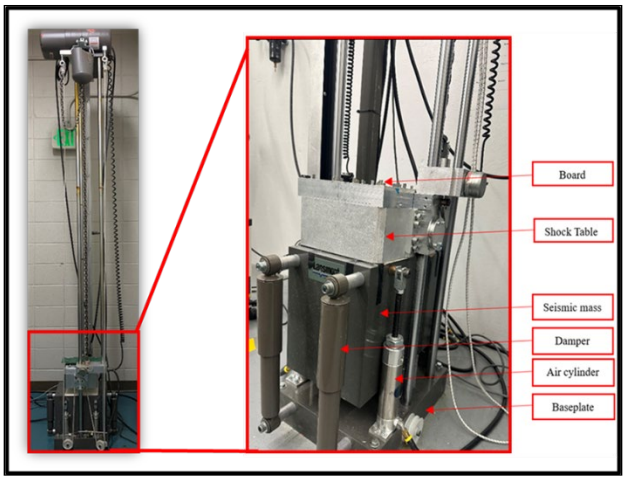


Figure 2: Model 23 Lansmont drop shock test

C. Boards' Assembly and Mounting

American Standard Circuits fabricated the printed boards. Plexus Corp. conducted the surface mount assembly. An organic solder preservative (OSP) finish was used. There are three main steps to assemble boards. The first one is printing the pads of PCB by solder paste onto the PCB using a solder printing machine. Then, a placement machine is used to align the components precisely on each board. Then, the board will be inserted into a nitrogen-controlled reflow oven to develop a reflow profile, as shown in Figure 3. Finally, the connections and resistances through the board will be verified among all completed boards, and x-ray images will be taken to ensure the solder joints are placed precisely on the copper pads, as shown in Figure 4.

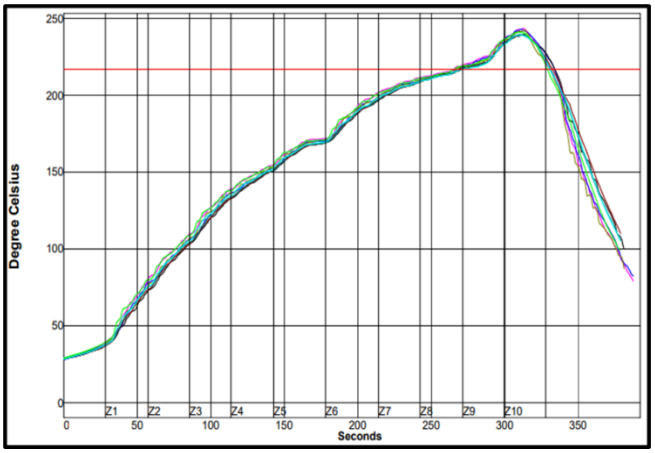


Figure 3: Thermal profile using multiple thermocouples
Source: Plexis corp.

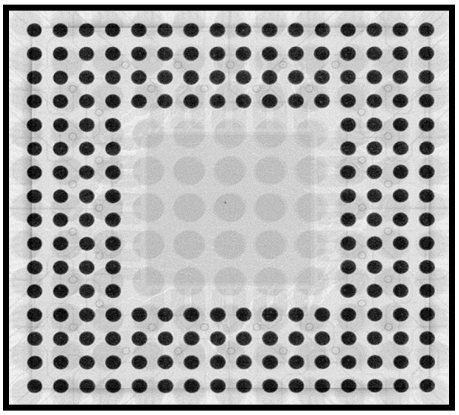


Figure 4: X-ray images of solder joints connection.
Source: Plexus corp.

Regarding the boards' mounting, the tested boards were mounted horizontally with the components facing downward. Four stainless steel screws were used to mount the board on the dropping plate, each tightened to 5 lb-in torque according to Joint Electron Device Engineering Council (JESD22-B111A) standards. Six boards were fixed on the drop tower plate and connected to a data acquisition system (DAQ970A). The DAQ970A is connected to BenchVue software to monitor and record the resistance of solder joints after each drop until the first failure is detected. Failure was defined as a point at which the resistance of the solder joint exceeded 100 ohms for three consecutive readings; the solder joint failed, and the whole component failed as well. However, the number of drops to failure of each board and the failed solder joint(s) are recorded for analysis, which will be discussed in the next section.

D. Microstructure Analysis Preparing

Microstructure analysis is performed on failed boards to confirm the failure mode and mechanism. Out of each board design group shown in Table 1, three boards were selected from each group: early failure, late failure, and failure near characteristic life. First, the samples will be separated from the board, as illustrated in Figure 1, through the orange lines. An Allied High-Tech precise saw with a diamond blade separates the component from the PCB. After that, the sample will be cleaned. Then, an epoxy solution is prepared by mixing hardener and resin with a ratio of 1:6. The samples will be placed in a mold for 24 hours. Finally, samples are removed from the mold for following grinding and polishing. The grinding process involved 6 sequence steps using 6 different grinding papers with grit sizes 120, 240, 400, 600, 800, and 1200. The polishing process will be the last step applied. The polishing process involves 3 sequential steps with 3 different silica particles: 3 µm, 1 µm, and 0.05 µm. Cross-sectional samples were analyzed using a Zeiss Axio Imager.M2M optical microscope, fitted with an Axiocam 503 color camera and operated through ZENCore software to capture images of the prepared samples. Captured images will be used to determine the failure mode and mechanism.

RESULTS AND DISCUSSION

The results of this study were collected and discussed in two main parts. The first part is the probability of failure analysis using Weibull analysis. The second one focused on microstructure analysis using cross-sectioning techniques.

A. Probability of Failure Analysis

In studying solder joint reliability, a two-parameter Weibull was employed to evaluate how the board thickness and solder mask define state and how they affect the board's shock reliability. Specifically, the parameter η denotes the characteristic life of the Weibull distribution, corresponding to the point at which 63.2% of the components are predicted to fail. On the other hand, β represents the slope of the Weibull plot when plotted in a log-log scale, providing insight into the distribution and tendency of the failure rates. Finally, to assess whether there was a statistically significant difference in the drop shock reliability among the thicknesses and the mask define state, an analysis of variance (ANOVA) was conducted. However, Figure 5 and Figure 6 represent the Weibull distributions corresponding to CABGAs and MLFs, respectively. Figure 7 and Figure 8 show the characteristic life corresponding to board thickness and mask define state, respectively.

Overall, the results indicate that SMD combinations exhibited better characteristic life more stable and predictable performance compared to NSMD, across all board thicknesses or components, as illustrated in Figures 5 and 6. The data has been summarized in Figures 7 and 8, respectively. In Figure 7, thicker boards demonstrated greater reliability than the thin ones across all board designs, regardless of the solder mask design, except for MLF32 with SMD. For that combination, the characteristic life of the thinner boards was slightly higher, though not statistically significant, as illustrated in Table 3. Figure 8 shows that solder mask define boards were more reliable than non-solder mask define boards across all designs, regardless of the board thickness, and this difference was statistically significant, as illustrated in Tables 2 and 3. However, thicker boards demonstrated better stability and predictability compared to thin boards, though the difference was not highly significant for specific board designs.

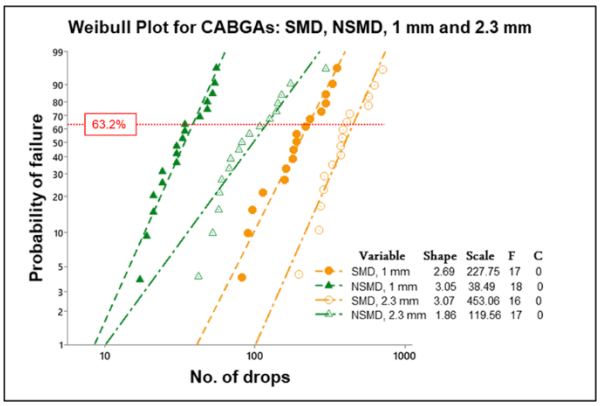


Figure 5: Weibull plot for CABGAs among all different board designs

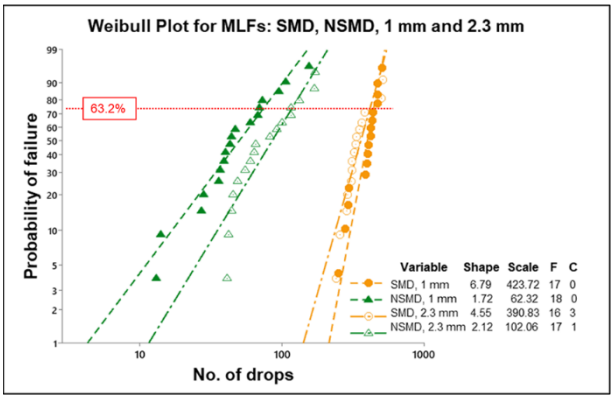


Figure 6: Weibull plot for MLFs among all different board designs

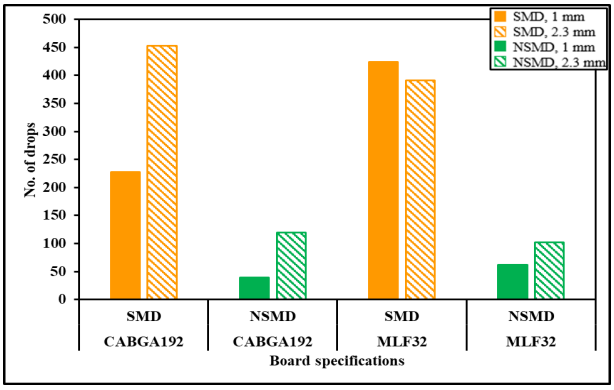


Figure 7: Characteristic life corresponding to board thickness

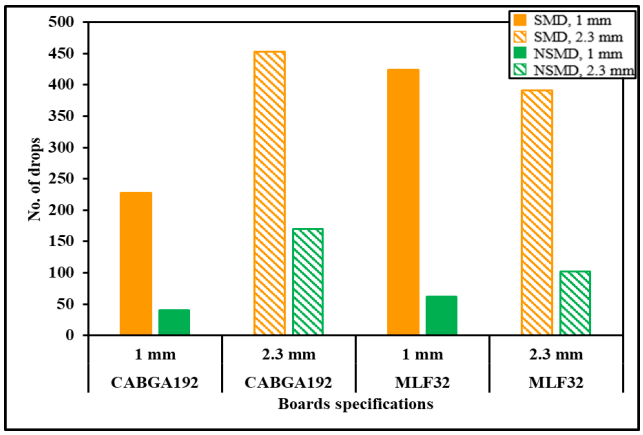


Figure 8: Characteristic life corresponding to mask define

Table 2: ANOVA Table for BGAs

Difference of Level	Difference of Means	T-Value	P-Value
NSMD, 1 mm VS. SMD, 1 mm	-167.5	-5.62	0.000
NSMD, 2.3 mm VS. SMD, 2.3 mm	-299.1	-9.75	0.000
SMD, 2.3 mm VS. SMD, 1 mm	202.6	6.60	0.000
NSMD, 2.3 mm VS. NSMD, 1 mm	71.1	2.39	0.09

Table 3: ANOVA Table for MLFs

Difference of Level	Difference of Means	T-Value	P-Value
NSMD, 1 mm VS. SMD, 1 mm	-338.9	-16.56	0.000
NSMD, 2.3 mm VS. SMD, 2.3 mm	-259.8	-13.08	0.000
SMD, 2.3 mm VS. SMD, 1 mm	-46.0	-2.25	0.121
NSMD, 2.3 mm VS. NSMD, 1 mm	33.1	1.67	0.349

B. Failure Microstructure Analysis

The failure analysis of the PCBs was conducted to identify the root causes of observed electrical failures. In this study, cross-sectional analysis was used to detect internal defects such as voids and cracks. Thus, the failure modes were determined for each board design by providing insight into how factors such as mask define, board thickness, and board components can affect the reliability of solder joints.

The failure occurred in the IMC for all CABGAs with SMD design, regardless of the board thicknesses, as shown in Figures 9 (a), (b), and (c). The crack initiated at the interface between the solder joint and the mask-define area then propagated through the IMC layer as long as there were no weaknesses in the solder joints. For CABGA boards with NSMD, the failure occurred at different locations, including bulk and IMC, as illustrated in Figures 9 (d) and (e). Moreover, for CABGA NSMD, a cross-section of many samples did not reveal any crack in the solder joint, while electrical failures were consistently observed. Thus, it is assumed that the failure occurred in the copper traces. However, the microstructural analysis indicates that thick boards experienced fewer trace failures compared to thin ones.

Regarding the MLFs SMD boards, the failure occurred either along the IMC layer or as a combination between IMC and bulk for both thicknesses, with no trace failures, as illustrated in Figure 10 (a), (b), and (c). On the other hand, the failure most likely occurred in the IMC layer among NSMD boards, regardless of the board thickness, as shown in Figures 10 (d), (e), and (f), with few samples showing failure through the traces. Figures 11 (a) and (b) show pad some pad cratering in CABGA192 with NSMD, while Figure 11 (c) shows pad cratering in MLF32 with NSMD.

CONCLUSION

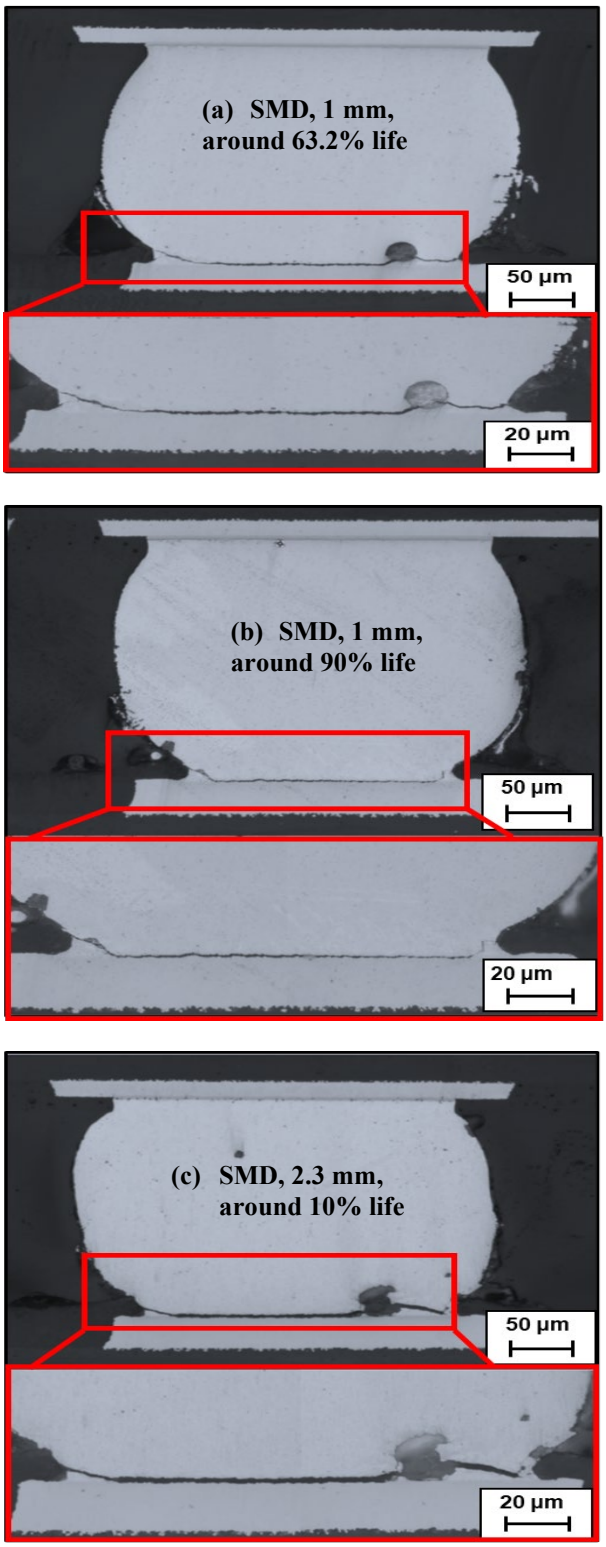
To sum up, SnAgCu305 alloy, applied with an OSP surface finish, was tested under two different board thicknesses (1 mm and 2.3 mm) and two mask define states (SMD and NSMD). The test was conducted in accordance with JEDEC standards (JESD22-B111A) to evaluate the effect of board design on the drop shock performance. The study focused on two key areas: drop shock reliability and failure analysis. In this study, Weibull analysis and microscopy images were used to assess the characteristic life and failure modes, respectively.

The outcomes of the Weibull analysis indicate that SMD boards are more reliable than NSMD across all board thicknesses and component designs. Notably, SMD boards show a more consistent failure mode for both CABGA and MLF components. Moreover, thick boards are more reliable than thin boards for both component types and solder mask designs, and they offer better resistance to failure under shock stresses.

One essential outcome was the more uniform crack propagation in SMD components compared to NSMD components, regardless of the board thickness. For instance, the cracks propagated along the IMC layer in BGA components with SMD design. In contrast, in NSMD boards, the failure occurred at different locations, including bulk solder, IMC, and even the traces. Trace cracking was particularly evident in NSMD boards, whereas SMD boards exhibited no trace-related failures.

The finding highlighted that the overall reliability of SMD boards was notably higher, as they showed more stable failure modes without trace issues, making them more suitable for applications requiring high durability and performance. These findings emphasize the importance of

board design, particularly the presence of solder masks, in enhancing the performance of solder joints under drop shock conditions.



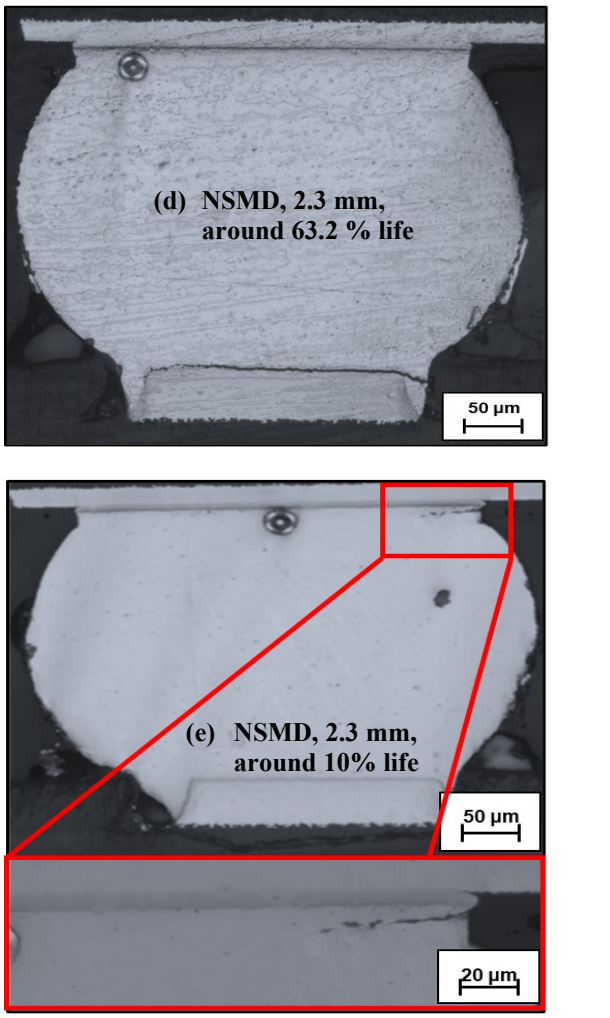


Figure 9: Microstructural changes in the IMC layer within solder joints. (a), (b) and (c) are BGAs with SMD, while (d) and (e) represent BGA192 with NSMD

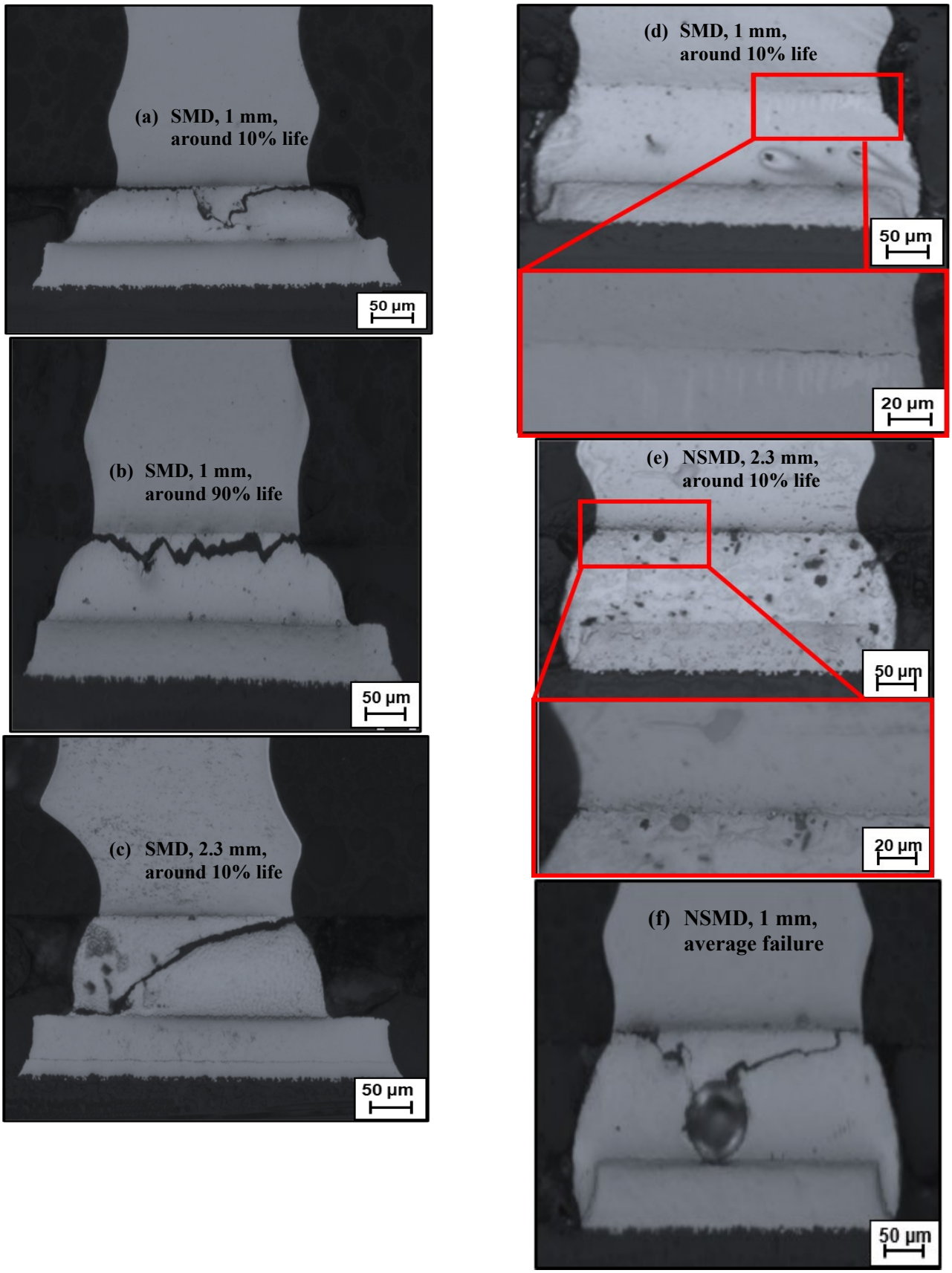
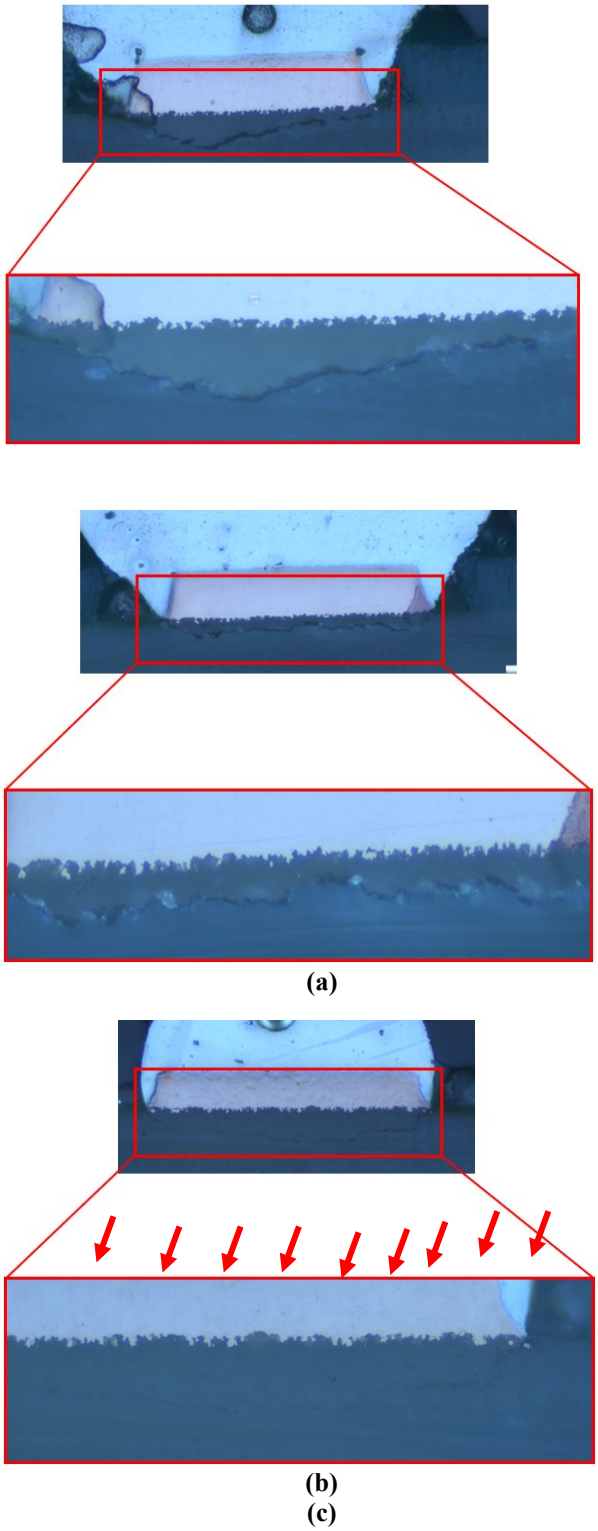


Figure 10: Microstructural changes in the IMC layer within solder joints. (a), (b) and (c) are MLFs with SMD, while (d), (e) and (f) are MLF32 with NSMD



(a)

(b)

(c)

Figure 11: Microstructure change of NSMD boards showing pad carting. (a) CABGA192, NSMD, 1 mm, (b) CABGA192, NSMD, 2.3 mm and (c) MLF32, NSMD, 1 mm

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