Development of a High-Density Adaptive Redistribution Technology for Embedded High I/O Components

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ABSTRACT
The industry's increasing demand for high-performance electronic devices with better functionality, lower power consumption and higher speed is driving innovation in advanced packaging technology. Improving the performance of semiconductor chips and advancing packaging features are critical.
One solution to producing high performance electrical systems to perform computationally intensive functions in volume constrained products is the use of miniaturized packages with advanced embedded components. In addition to requirements such as sufficient yield from the lithography process itself, to avoid losing high density and valuable components, an important issue in RDL formation is registering each layer of the production board to the corresponding component during lithography. One solution is to measure the deviation of the target from the actual position, then digitally calculate and re-route the connections in the RDL pattern, and finally process the adapted data into raster image data to perform a maskless direct imaging process. [1], [2].
This paper presents the development of the necessary technology blocks for high-density redistribution layers, required to realize such organic substrate-based packages.
The technology approach used is an advanced semi-additive processing (aSAP) at large panel level. This technology involves the use of dielectric layers, such as ABF or similar, PVD seeding and additive electrolytic copper deposition. It also describes the use of thin PVD seed layers below 100 nm, the incorporation of plasma processes to dry etch photoresists, to clean the surface and to etch back seed layers on 18”x24” / 610 mm x 457 mm panels.
Results from the EU-funded CHARM project are also described. Here, in close cooperation with AT&S, large dies of 26mm x 18mm were embedded using low CTE core material and dielectric thin film, Ajinomoto Build Up Film. During the embedding process performed by AT&S, ABF material was used to symmetrically embed temporary fixed components using a carrier. After exposing the copper pillars (30 µm diameter) through the BU film, PVD metal deposition was used to seed the surface with titanium and copper.
To connect the embedded components, IZM developed an adaptive patterning process consisting of an optical measurement routine and software to digitally correct the manufacturing data. The adapted data is fed into a maskless lithography tool so that each unique device on each unique panel is registered.
In addition, results are presented on how the Semi-Additive Process (SAP) itself can be advanced by using an improved direct imaging process on an embedded die to achieve a resolution of 5 µm L/S despite topography and roughness effects.

Key words: Embedding, Adaptive Imaging, Direct Imaging, RDL, IC substrate

INTRODUTION
To meet the demands of high-density organic substrates, which require a structure size of significantly less than 10µm lines and spaces and pitches of 50µm and below, new technological approaches need to be considered. Established substrate technologies such as mSAP (Modified Semi-Additive Processing) or SAP (Semi-Additive Processing), which rely on thin copper films and/or electroless copper deposition for seeding, cannot meet these requirements.

The technology approach used to address high-density organic substrates is based on Advanced Semi-Additive Processing (aSAP) at the large panel level. This technology involves the use of thin dielectric films, such as ABF or similar, PVD seeding and additive electrolytic copper deposition (Figure 1). Looking at this approach, it is clear that wafer backend technologies are merging with traditional PCB/substrate technologies.

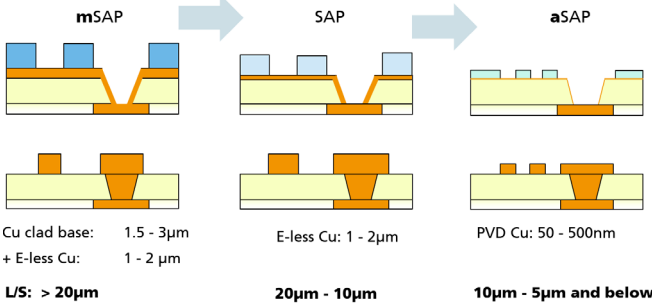


Figure 1: Overview of panel technologies towards smaller pitches

Vertical interconnects can be made by laser drilling, lithography if photoimageable dielectrics are used, or plasma with reactive ion etching (RIE). The process capabilities and limitations are discussed in detail.
Horizontal interconnects are fabricated by seeding, photo-imaging of plating masks and subsequent copper deposition, and resist and seed removal. Photo-imaging is an important step in this process.

The evolution towards line and space structures targeting 5µm and further down to 2µm on large panels up to 610x457mm² is described.
Finally, electrical test data and the resulting process yield for different structure sizes are essential to provide a reliable process technology.

ADVANCED SEMI ADDITIVE (ASAP) RDL PROCESS

Process description

The complete semi-additive process flow for RDL formation is shown in Figure 2.

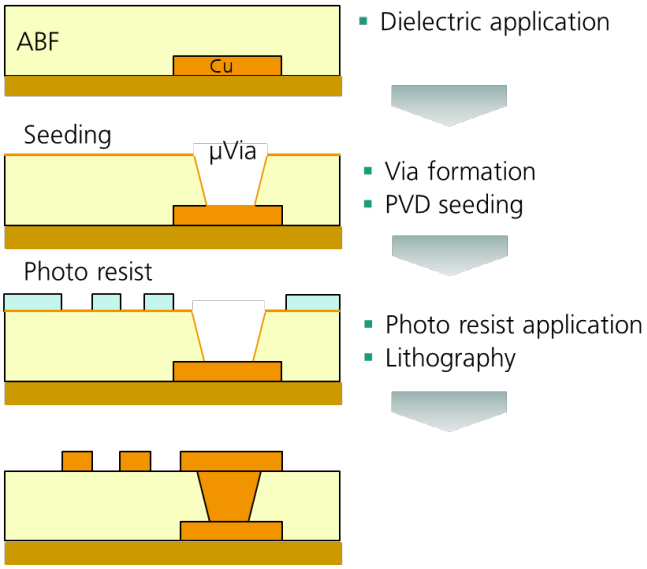


Figure 2: Schematic of semi additive processing.

After applying the thin dielectric material, the vertical interconnects, micro vias, are formed, which will be discussed in the next section. Next, a Ti/Cu layer is sputtered onto the front side of the substrate. Studies have been carried out to optimize the thickness of these two layers. On the one hand, they have to be thick enough to provide a sufficient electrically conductive layer for uniform copper plating and good adhesion to the dielectric. On the other hand, they should be as thin as possible to enable ultra-fine line capability, targeting 5µm and below structures. A combination of less than 100nm for Ti and Cu was found to be a reliable configuration. For a double-sided process, this is repeated on the backside as well. A thin dry film photoresist is then applied. Direct imaging is used for exposure. This step defines the RDL structure. This is followed by electrolytic copper plating to create the conductive lines. Finally, the photoresist material is stripped, followed by differential etching of the copper and titanium layers.

Vertical Interconnects

Laser via in non-photo dielectric

There are several ways to create vertical interconnects between layers. Depending on the type of dielectric used, the potential options are described below.
Although there has been tremendous progress in the development of thin film dielectric materials suitable for panel applications, non-photo-sensitive materials are still in the majority. One long-established candidate is the so-called ABF (Ajinomoto build-up film) dielectric. These films are made from various resin systems and are highly filled with particles down to less than 1µm in size to adjust the coefficient of thermal expansion (CTE). They are not glass reinforced like PCB material.
The typical method for making vias in this material is laser ablation using a laser drilling process essentially derived from HDI substrates.
Due to the nature of this laser drilling method, it has several limitations. The size of the holes drilled is primarily limited by the focal point of the laser beam. Modern laser systems can produce a focal spot as small as 10 µm in diameter, resulting in via diameters of this order. However, the process window and yield of such small laser vias still need to be studied in detail to learn more about the impact on overall yield. In addition, laser drilling is a sequential process, which means that the time required to process a complete substrate depends on the total number of vias to be drilled. If these are in the millions per panel, drilling times become long, throughput decreases and is not economically acceptable.

Photo imageable dielectrics

Recent material developments are moving in the direction of photoimageable dielectrics (PID). These offer several advantages. Using a lithographic imaging system, the resolution and thus the via diameter can be significantly reduced compared to laser vias. When using a high resolution imaging system, the via diameter is mainly limited by the resolution of the PID. In addition, photo imaging is a parallel process that creates all the vias on a board simultaneously. This has a significant impact on throughput.

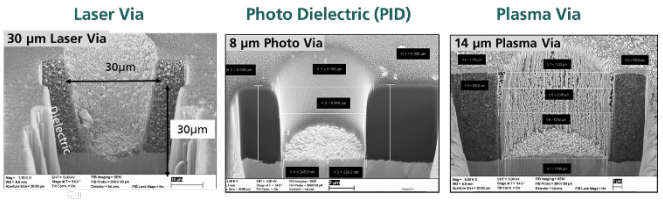


Figure 3: Overview of different via technology approaches

Plasma via in non-photo dielectric

Another method of creating a via in a non-photosensitive material is the reactive ion etching (RIE) plasma via [3],[4].
This is a dry, plasma-based process that allows all vias on a board to be created in parallel. To define the via size and position, an additional temporary mask must be applied to the dielectric. This can be a PVD deposited metal mask which is then patterned by lithography and etching.
The advantage of this approach is that it can target via dimensions similar to the photo via process, it's selectivity between polymer and copper, and the ability to use established CTE-adapted dielectrics such as ABF.
Challenges remain: the still relatively low etch rate, the effect of polymer redeposition and the need for fluorine gases for the process.
Figure 3 outlines all three via technologies.

RDL formation

The RDL is realized by an advanced semi additive processing. The sequence here is:

- PVD seeding of Ti and Cu
- Photo resist application and lithography
- Electrolytic Cu deposition
- Resist strip and seed etch
- In the following the process steps will be described more detailed.

The lithography step is very important to achieve the required high resolution lines and spaces. Therefore, the choice of photoresist is very important. Several systems have been studied. A dry film resist (DFR) is preferred because it can be easily applied to a rectangular substrate. On the other hand, DFR could be a limiting factor in achieving the resolution offered by the direct imaging system. That's why liquid photoresist and suitable application methods to the panel were also investigated.

Exposure of the photoresist is mask less using a direct imaging system. For high resolution exposure, a direct imaging system based on a digital micro mirror device (DMD) is used. It is equipped with photo heads each carrying a DMD with 2560 x 800 mirrors. The light from a 405nm photodiode is reflected by switchable mirrors and passed through an optical system to project an image onto the photoresist. The optical system with a sub-pixel size of 210nm is designed for a lateral resolution of structures down to 2µm. Due to the operating principle, the photo heads move in strips over substrates with a size of up to 620mm x 620mm.

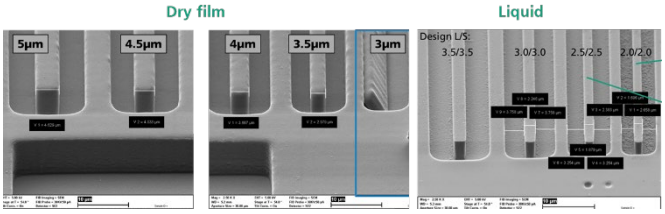


Figure 4: Direct imaging results for dry film and liquid photoresist

One DFR tested is a 7µm negative tone photoresist. This material has been shown to resolve feature sizes down to 3.5µm. Using a spray-coated liquid photoresist with a spray thickness of 3µm, feature sizes down to the resolution limits of the DI machine have been achieved.

Electrolytic copper plating is performed in dedicated panel plating equipment. It is important to achieve the highest possible uniformity, but also a reasonable deposition rate and reliable plating of lines and vias.

Removal of the photoresist material after plating is the next critical step. Specifically, wet chemical and plasma etching are considered.

Wet chemical removal is a commonly used technique, but at these feature sizes, some defects can occur in certain areas due to resist residues on the seed layer. Plasma treatment with O2 after wet stripping can completely remove the residues. Figure 5 shows an example of such a process.

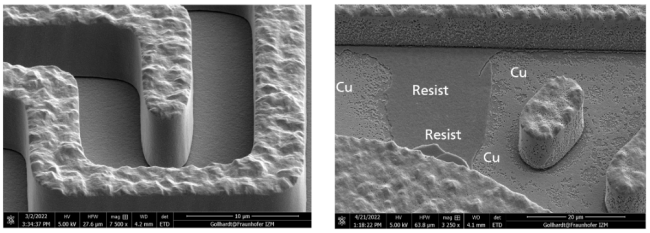


Figure 5: Cu structures after wet chemical resist strip

While wet stripping is a common industry process, IZM also evaluated options such as dry plasma etching of the resist to further reduce the size of the features (Figure 6).

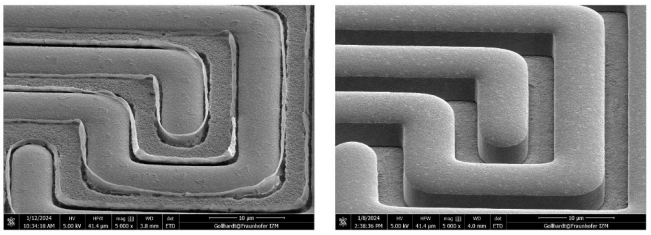


Figure 6: Resist plasma etching: at start (left), complete removal and wet cleaning (right)

The final step is to remove the Ti/Cu seed layer. Again, wet and dry etching methods are considered. Since wet etching is an isotropic process, there is a high risk of line width reduction and line adhesion during this process. The optimized Ti/Cu seed thickness used, provides a good starting point, but also has limitations for ultra-fine line structures when wet chemical methods are used. Figure 7 shows an example for 5µm L/S structures after dry etching of the seed layer. With this method, there is literally no under-etching of the line.

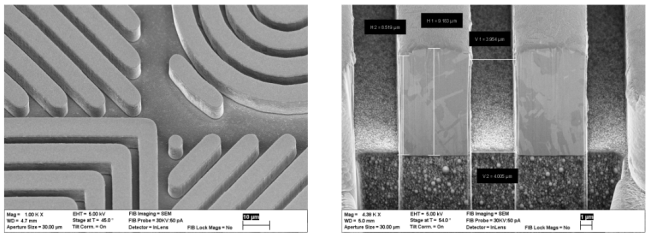


Figure 7: SEM overview of 5 µm L/S after dry etch of Cu and Ti

EU PROJECT "CHARM"

Introduction

As part of the CHARM project, IZM, in close cooperation with AT&S, was responsible for the development of a first-level interconnect technology that realizes a high-performance computing module for use as an ADAS system in autonomous mining vehicles.

These modules integrate power management, central processing units, memory and thermal management in a very small volume by combining advanced PCB technologies, high-density interconnects and component embedding. For the computing module within the ADAS system, AT&S embedded a large 26x18mm² die using core and ABF materials to form a 150µm thin panel. Vertical interconnects in this approach are formed by Cu pillars on the die, which penetrate through the ABF material and are then exposed in the surface. To provide the first level interconnect for this module, IZM's challenge was to develop a technology that could accommodate the high I/O count on the die and the given pitch in combination with the required routing density. For the complete ADAS PCB module, the computing module is stacked on a PCB along with the power supply and memory (Figure 8).

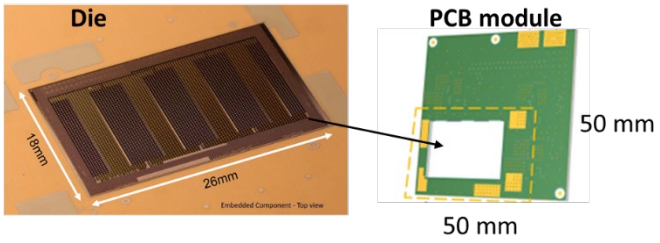


Figure 8: ADAS module concept

Adaptive Imaging

Method

To realize fan-out RDL of fine pitch embedded components, it is essential to use a method that compensates for possible component misalignment, which could be the result of component placement tolerances and displacement during the embedding process. Therefore, it is necessary to adapt the design data used to image the RDL structures. This method requires two main steps:

- Measurement of the given positions of the components on the panel after placement and embedding
- Adaption and recalculation of the design data
- Generation of raster imaging data (RIP)

Based on the above, direct imaging could be performed by digitally imaging the RDL structures using adapted designs.

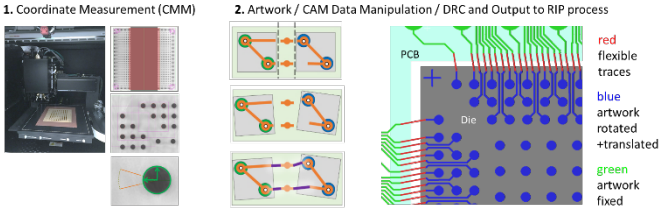
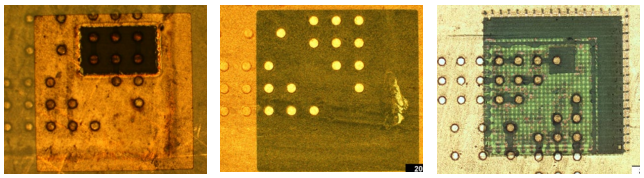


Figure 9: Adaptive processing sequence

Coordinate measurement and layout adaption

The goal of the coordinate measurement is to obtain reliable x/y/theta measurement data of the components after embedding to ensure accurate and precise results. The measurement is based on a high precision optical coordinate measuring machine (Rudolph/Onto Firefly 1200S). It is crucial to ensure that the substrates are properly illuminated and in optimal surface condition to guarantee the reliability and reproducibility of the measurements. Therefore, it is essential that the marks on the substrate and the components have ideal contrast, which is affected by the opening of these marks and the illumination.

To determine the optimal method for opening the marks, we investigated a number of techniques, including lithography, etching (both wet and dry), and laser ablation. Figure 10 illustrates the results.



a) b) c)

Figure 10: Opening of marks by a) litho & wet etch, b) litho & dry etch, c) laser

For optimal illumination, we recommend the use of fluorescent lighting. This will allow us to clearly visualize the contour of the metal die pad and registration marks with high contrast (white = organic/ABF/laminate, black = metal/Cu). Please refer to Figure 11.

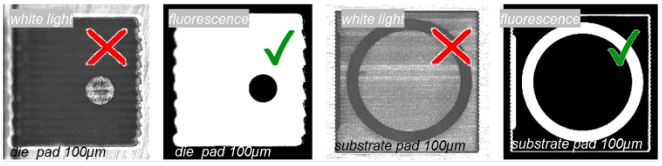


Figure 11: Component registration using white light (red cross) and fluorescens light (green mark)

The measurement data is fed into a CAM-connected script that recalculates the layout on a GBR or ODB basis for each die and all surrounding conductors, traces, and vias for each module. The data set is then imported into a CAM program and checked for design rule compliance (DRC) and error checking of the adaptation routine, Figure 12. Thousands of elements (connections, pads, vias) have to be processed during this step. By optimizing the algorithm, the time required for each module to be calculated has been reduced from several hours to minutes.

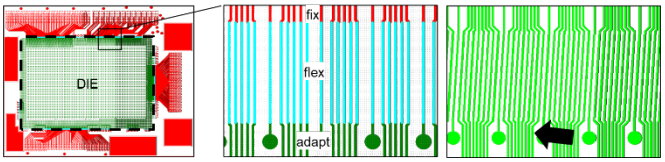


Figure 12: Artwork adaptation, schematic

Raster image processing (RIP) and lithography

In order to create the necessary exposure data for direct imaging, it is essential to convert the processed, adapted layout data into rasterized machine data. This process results in the creation of a unique RDL data set for each panel processed. The processing time is significantly affected by the resolution and number of elements, as well as the computing power of the RIP engine. The rasterization time for each row of four dies was 20 minutes, resulting in a total rasterization time of 80 minutes for a complete panel. Subsequently, direct imaging was conducted using the registration mark positions from the AOI. Finally, illumination of the panel, which took approximately 15 minutes for one panel, was completed.

Given the significant impact of the seed layer's roughness on the lithography tool, a series of experiments were conducted to optimize the digital compensation, fluence, and autofocus settings. This was done to achieve a compensated ideal line and space ratio on the modified surface. The optimization loops yielded the results depicted in Figure 13. Reduction values of up to 2.2 µm were employed in both the x and y directions. This outcome can be attributed to the disparate impact of the surface roughness of the copper on the optical system of the exposure unit in the x and y directions. Consequently, it is evident that a more substantial reduction of the structures is essential in the y direction due to this property.

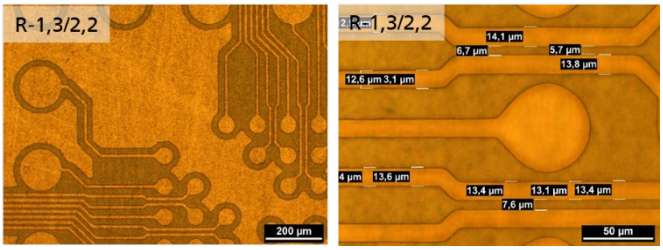


Figure 13: Digital imaging exposure optimization

The rasterization of the adapted data of each functional panel with embedded dies was performed in accordance with the specified settings. This resulted in a superior alignment accuracy of the RDL image to the embedded component, with a maximum deviation of 2–6 µm (Figure 14). The necessary 5 µm L/S resolution was achieved using a 7 µm thick dry film photo resist.

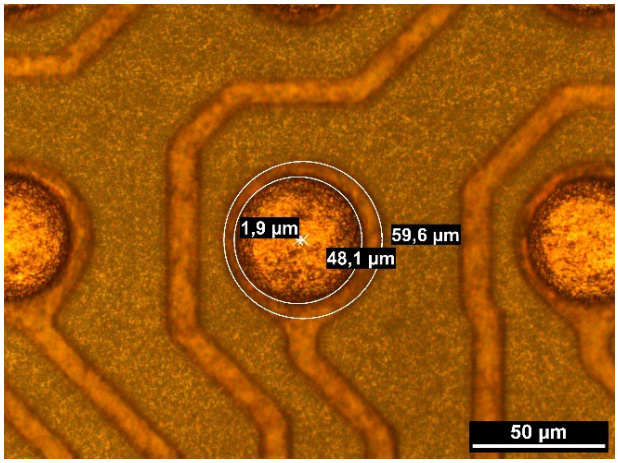


Figure 14: Alignment of RDL to embedded die pad

RDL formation

The RDL formation was then completed by Cu plating, resist removal and seed etching as described in the first part of this paper. For the project demonstrator, a double-sided SAP process was performed on 610x457mm² panels with 150µm thickness. In total, 9152 I/O pads of the 26x18mm² dies had to be connected to the fan-out RDL structure.

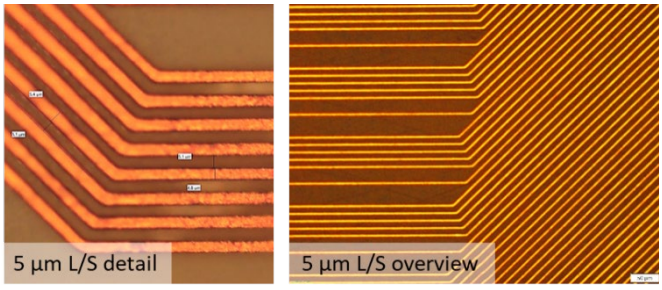


Figure 15: 5µm L/S RDL fan out CHARM demonstrator

Figure 15 shows a snapshot of the 5µm L/S fan-out RDL required for the CHARM demonstrator. In addition, Figure 16 shows the excellent alignment of the adapted RDL to the die pad and an example of the adapted RDL lines connecting the die pads to the fixed RDL areas.

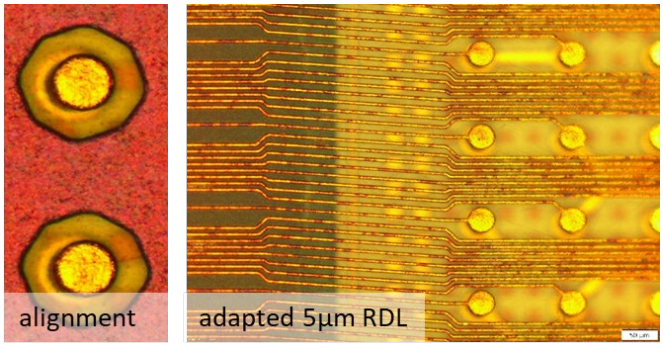


Figure 16: Pad alignment and adapted 5µm RDL

CHARM demonstrator conclusion

To complete the final demonstrator, an adaptive fan-out RDL process was successfully implemented.

To successfully fabricate the demonstrator, the development of the core steps for adaptive imaging: measurement of die shift and rotation, processing of adapted layout data, and rasterization of imaging data for exposure was essential.

To obtain the necessary data the die positions on each panel were measured after placement, embedding, pillar reveal, and sputtering. Adaptation of the design data stack resulted in the formation of unique packages and panels corresponding to the real situation of each individual panel.

Direct imaging was performed using the adapted true layout data, followed by completion of the fan-out RDL by ultra-fine line Cu plating, resist strip and seed etch. Final results are presented in Figure 17 and Figure 18.

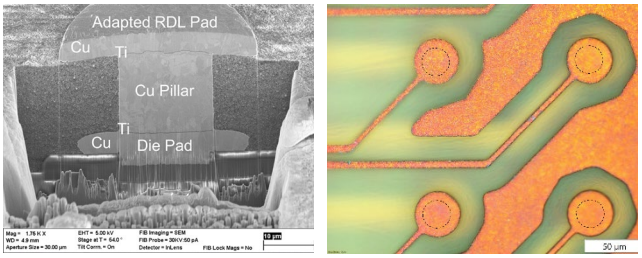


Figure 17: Example for connected Cu pillar to RDL

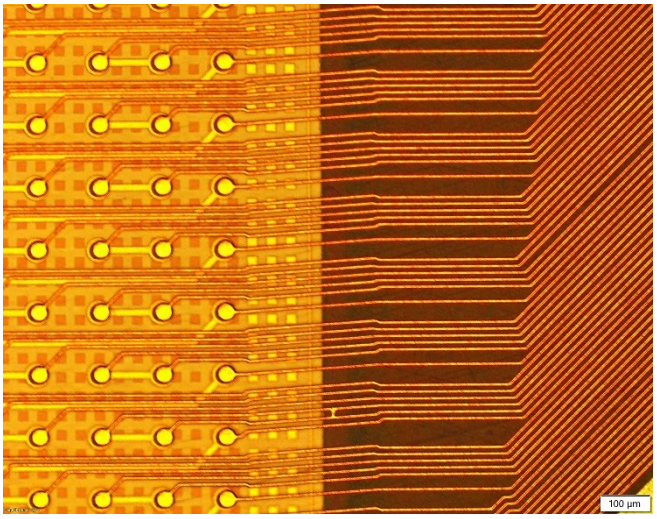


Figure 18: Overview of adapted 5 µm L/S RDL

SUMMARY

The development of a process technology for high density organic substrates, based on advanced semi additive processing was successfully demonstrated. Different technology blocks for vertical and horizontal interconnects were established, and the advantages and disadvantages of the different via technologies were determined as a result. In addition, the RDL processing was optimized and alternative process option implemented.

Within the EU project "CHARM", a successful development of RDL processing for fine L/S structures, which is of paramount importance for fan-out embedded modules with high I/O dies inside, as well in general for HDI substrate manufacturing was achieved. The work done has firstly developed all the core steps for RDL processing, namely the adaptive imaging taking into account the die shifts and twists, rasterization of the imaging data and the final implementation of direct imaging in combination with profound semi-additive processing, reaching even copper structures at 3.5µm L/S. In turn, the developed RDL processes were successfully demonstrated on the computing module manufactured by AT&S, where on one computing panel with four large dies, very fine copper structures at 5µm L/S were achieved as required in the compute module. The R&D work on RDL processing will further build on the CHARM latest results toward even finer L/S structures at high yield for large industrial format panels.

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