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Development of Si-Interposers for 3D Heterogeneous Integration

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ABSTRACT

SkyWater is working with our partner BRIDG (Bridging the Innovation Development Gap) to establish a domestic supply chain for Si-Interposers with and without through silicon vias (TSVs). BRIDG is leveraging a strategic advanced packaging partnership with imec by licensing and transferring the imec silicon interposer technology to the Center for NeoVation in NeoCity, Florida, making the State-of-the-Art technology available to the US Industrial Base for low volume production. Si-Interposers provide a platform to assemble multiple types of chips (chiplets) to achieve a very high-density multi-chip module. This is especially important when accommodating very fine pitched die (50um and less) that require a higher density circuity (1um lines/spaces L/S and less) offered by a semiconductor back end of line (BEOL) process. Current metallization processes used for organic substrates can only effectively go down to about 5um, which limit the die pitch to 150um or greater. Future chiplet designs are projected to scale below 20um pitch, and this is where Si-Interposers offer the advantage. Two silicon interposer electrical qualification vehicles will be discussed in this paper. The first one is a bridge interposer, having two metal Cu Damascene layers with 1um lines/space on a Si-substrate with a body size of 9mm x 13mm. The second electrical qualification vehicle has the same body structure along with through silicon vias (TSVs) having dimensions of 10um x 100um. For these two offerings, the basic process flows will be presented, along with supporting technical data. In addition, examples of applications for both offerings will be presented.

Keywords: Si-interposer, chiplets, multi-chip module, back end of line (BEOL), substrates and through silicon vias (TSVs).

INTRODUCTION

Silicon interposer technology has multiple advantages over conventional organic interposers. These include:

- The capability to produce very fine lines/spaces (L/S) of 1um and below using the Cu Damascene back-end process.
- Accommodate very small I/O pitches (10um and below).
- Extremely flat for good assembly yield.
- Matching CTE between Si devices and the interposer to achieve high reliability.

A typical application for a Si-interposer is shown in Figure 1, which is a Chip-on-Wafer-on-Substrate (CoWoS) Si-interposer with Through Silicon Vias (TSVs) multi-integration technology that is widely used in High Performance Computing (HPC) and Artificial Intelligence (AI) applications to attach multiple chips, developed by TSMC [1]. In this configuration, several highly dense I/O die can be successfully attached to the Si-interposer to achieve the appropriate 3D packaging solution.

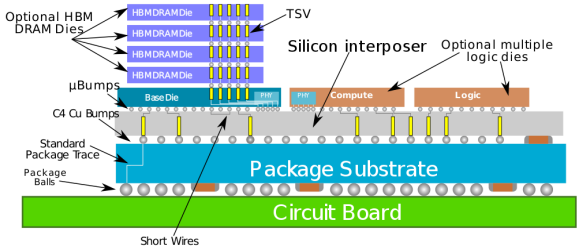

Figure 1: CoWoS is a 2.5D wafer-level multi-chip packaging technology that incorporates multiple dies side-by-side on a silicon interposer to achieve better interconnect density and performance

Another common application for a Si-interposer is what is referred to as a bridge interposer. This technology was developed by Intel and is referred to as Embedded Multi-die Interconnected Bridge (EMIB) [2], where a small silicon device with high density interconnect is embedded directly into the substrate and serves to connect two devices with high-speed communication channels. This technology offers higher wiring densities over conventional high density organic packages, as shown in Figure 2 [3]. The TSV based design has the highest wiring density.

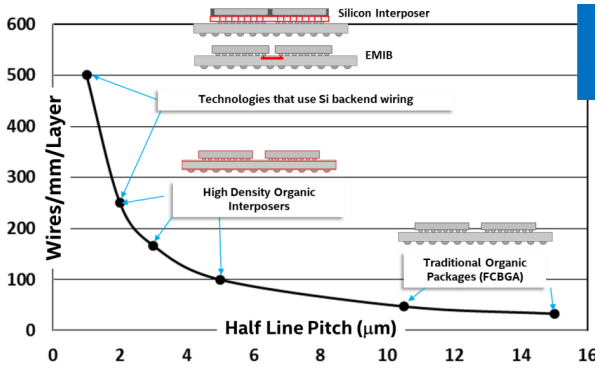

Figure 2: 2D Multi-Chip Packaging Landscape as presented by Intel [3]. This graph shows that the embedded bridge interposer (EMIB) and the TSV based Si-interposer designs offer the highest wiring densities when compared with advanced organic substrates.

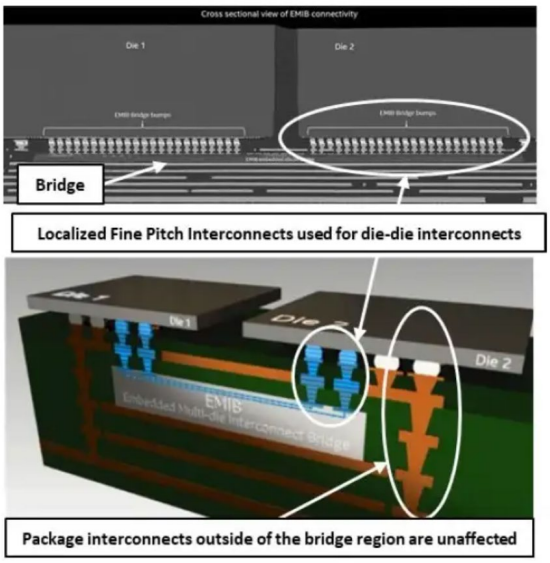

Figure 3: Bottom image, is a schematic of the embedded bridge Si-interposer in the organic substrate. Top image is cross-section of an actual bridge interposer connecting two adjacent chips.

Figure 3 shows a schematic of a bridge interposer embedded in a substrate along with a cross-section of a Si-bridge interposer embedded in the buildup structure of the organic substrate.

Another architecture for utilizing bridge interposers is in an advanced fanout embedded packaging technology. An example of this from Deca Technologies is shown in Figure 4 where the bridge interposer is embedded in a molded reconstituted wafer and used to interconnect devices mounted on the surface [4].

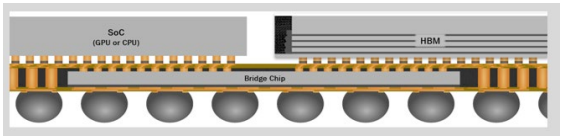

Figure 4: An embedded bridge interposer in a two die chips last FOWLP package design by Deca [4].

These examples show the two basic types of Si-interposer architectures that are common today:

1. A TSV interposer that can connect multiple fine pitch die on the topside and then be attached on the backside to a substrate.
2. A bridge interposer (non-TSV) embedded in an organic substrate that can interconnect two chips that are assembled on the surface of the organic substrate.

APPROACH

SkyWater and BRIDG are working together in a government-supported Industrial Base Analysis and Sustainment (IBAS) program to establish a silicon interposer fabrication and manufacturing capability in the U.S. A four-phase approach is being used to stand-up the Si Interposer technology, where each phase builds on the progress of the previous one to create more complex interposer structures. Figure 5 shows the phases and interposer structures for each phase of this activity. The interposer technology is based on a process flow developed by IMEC and utilizes Cu-filled through silicon vias (TSVs), Cu damascene processing for front side routing layers, and semi-additive Cu processing for back side routing layers. Phase I establishes the initial Cu damascene process capability and provides the basis for fabricating bridge interposers. Phase II incorporates the TSV structure with the Phase I Cu damascene process flow. Phase III extends the Phase II process with additional front and back side routing layers and incorporates integrated resistor and MIM capacitor structures in the flow. Phase IV modifies the Phase III process flow to incorporate a low dielectric organic passivation material (BCB) and R, C, and L integrated passive structures for an RF interposer platform. This paper will review the status of the ongoing interposer development program and provide details on the process capabilities that have been established and characterized to date.

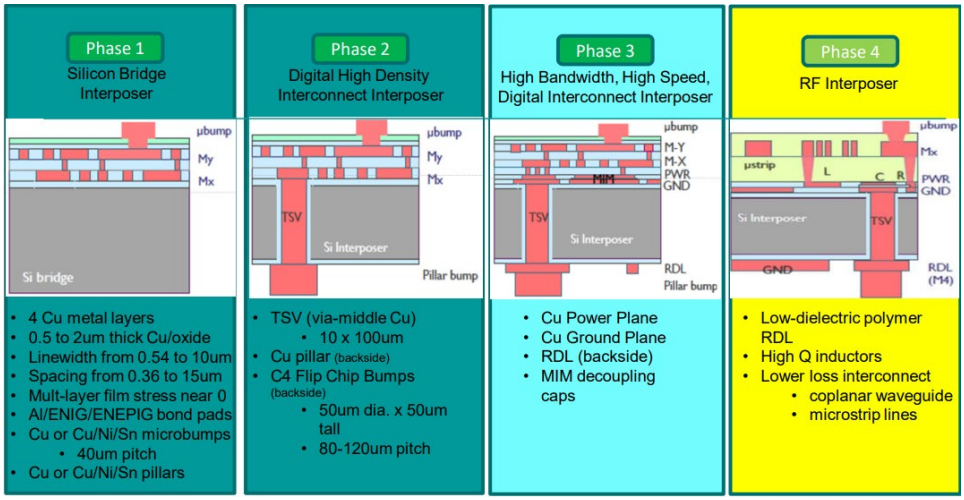

Figure 5: The four phases of Si-interposer product development.

PHASE I INTERPOSER DESIGN AND PROCESS DEVELOPMENT

A schematic drawing of the Phase I Cu damascene build-up structure is shown in Figure 6. In this design there are 2 copper routing layers, M1 and M2, and a via, V1, each with 1 micron thickness. The interposer is capped with an aluminum pad.

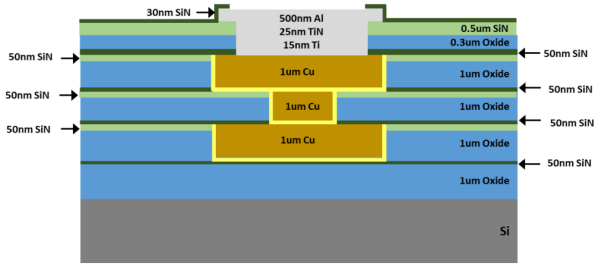

Figure 6: Schematic drawing of the buildup structure for Phase I interposer design.

In this process, SiN was used for the etch stop layer. Approximately a 1um thick dielectric layer was used for each Cu layer (M1, V1 and M2) and the final topside dielectric layer was 0.8 micron. The deposited

Al metal in the pad region was 0.540 micron consisting of a stack of Al-TiN and Ti, see Figure 6. A summary of the process learning is as follows:

- Metal etch was optimized
- CMP recipe was optimized with internally developed process parameters
- Cu anneal cycles were optimized to address Cu voiding and migration
- A lower temperature Al deposition process was developed to improve coverage
- Al etch validated and Al clean processes optimized

The via 1 (V1) anneal cycle of learning and M2 metal etch cycles of learning will be presented. In the first example, V1 to M1 cycle of learning, initially one can see in Figure 7-1, when both M1 and V1 were annealed, there was significant voiding in V1. In Figure 7-2, when only M1 annealed, no voids were shown, however, there were divots seen in the M1 from underplating. This process step required further plating thickness optimization. Finally, in Figure 7-3, the results of an optimized annealing profile and plating process are shown that exhibit no divots and V1 fully contacting M1.

The second process development example is the M2 metal etch. The initial recipe resulted in under-etching of the etch stop layers, in which the metal lines did not contact the vias, as shown in Figure 8-1.
In the case of Figure 8-2, there was 10% over etching, however, the M2 layer did not fully land on V1. After optimization of the etching, the M2 layer fully landed on the V1, as shown in Figure 8-3.

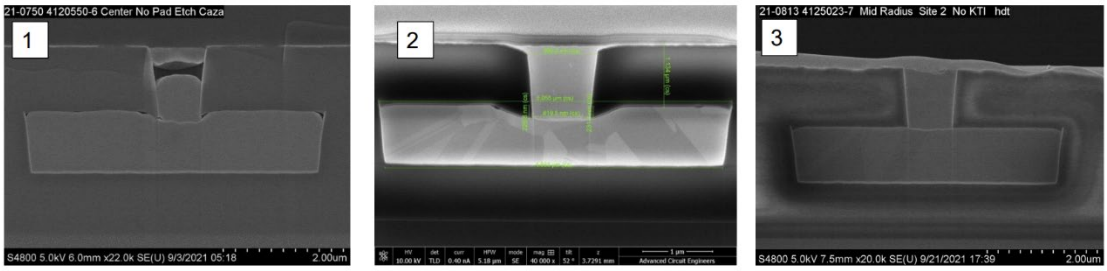

Figure 7: Sequence of learning involved to optimize V1 to M1 adhesion

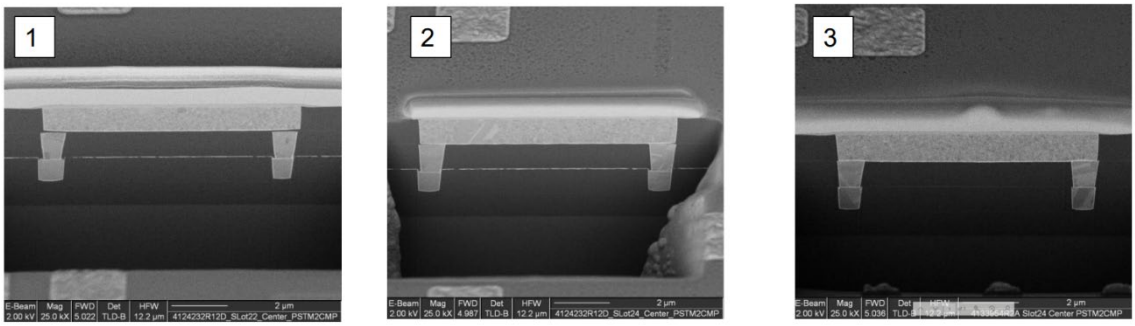

Figure 8: M2 metal etch cycles of learning

- 200mm semi-automated wafer prober
- FormFactor Summit 200
  - 200mm wafers to chip handling
  - DC, RF and Optical testing compatible
    - EMI Shielding >20db 0.5-20GHz
    - Light attenuation >120dB
    - Noise floor <-150dBVrms/rthHz
  - Temperature testing -60C to 300C
  - Auto-loader upgradable
  - Probe Card and Manual Probe Capable
- Electrical Test
  - National Instruments PXIe Chassis
  - Source Measure Unit 1uA-10A/600mV-60V
  - 512 Crosspoint (4x128 channels) Switch Matrix

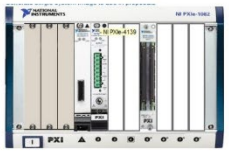

Figure 9: 200mm semi-automated wafer prober used for electrical testing.

PHASE I ELECTRICAL TESTING & CHARACTERIZATION

Five different electrical tests were performed to initially qualify this technology. A summary of the five test is as follows:

1. Metal comb capacitor for inter-level dielectric characterization
2. Metal-metal combs and meanders for intra-level dielectric characterization
3. Via Kelvin testers for contact resistance characterization
4. Via daisy chains for metal-to-metal continuity characterization
5. Van der Pauw sheet resistance and isolated/dense metal line configurations for electrical linewidth characterization

The electrical testing was done using a 200mm semi-automated wafer probe tester (Formfactor Summit 200), as shown in Figure 9.

The metal meander combs are used measure capacitance, leakage, and breakdown voltage. The metal meander comb parallel structures are process monitoring structures to characterize the yield and reliability of the metal patterning process. The capacitance between the combs and the meanders provides information about the dielectric properties of the intra-level-metal-dielectric structure. Figure 10 shows a schematic of the comb test structure designs.

The results of the metal meander comb capacitance testing are shown in Figure 11. As can be seen from this data, the capacitance values for M1, M2 and V1 are all higher than the minimum specification value of $1.8X10^{-12}F$. This data shows a 100% yield on the metal capacitance test.

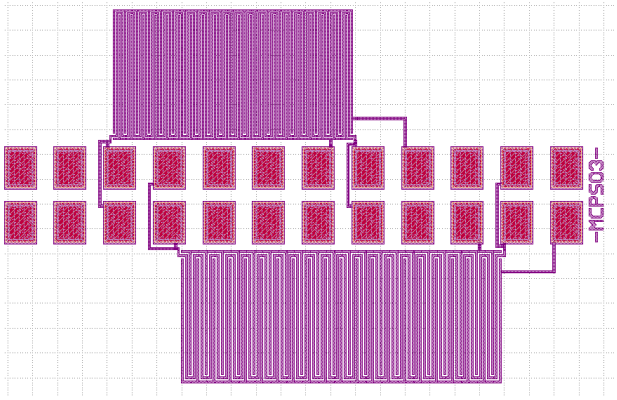

Figure 10: Metal meander comb test structure design.

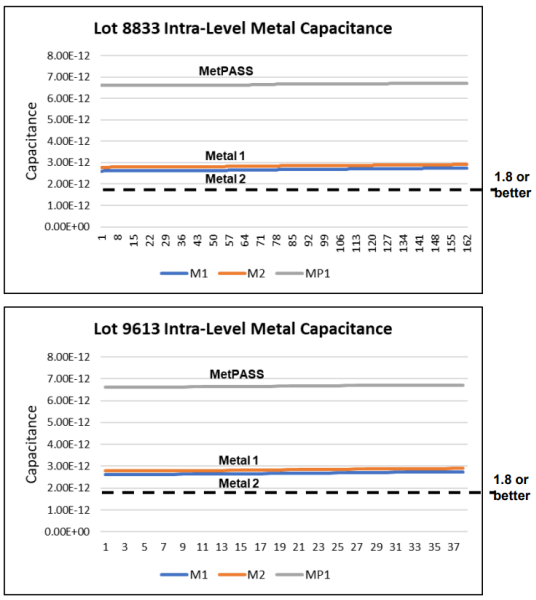

Figure 11: Intra-level metal capacitance test results for two lots.

The next test data is the metal meander comb leakage test results, which are shown in Figure 12. From this data there is 100% yield on M1, M2 and the MetPass (top Al pad) structures.

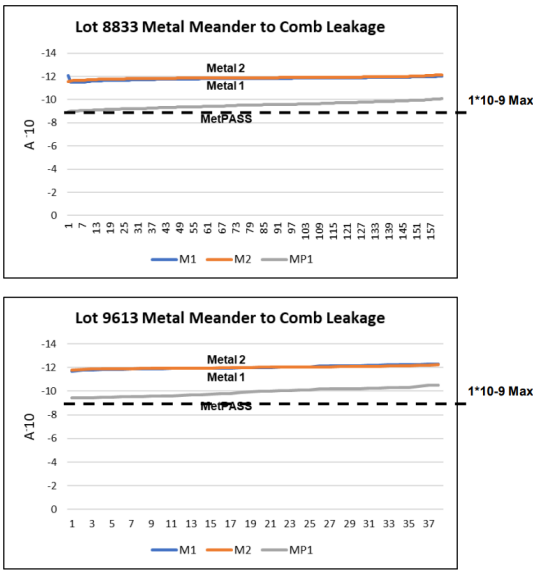

Figure 12: Phase I metal meander comb leakage test results for M1, M2 and MetPass (top Al pad) structures.

The next set of electrical data is the metal meander comb breakdown voltage test results, shown in Figure 13. In this testing 20V is the maximum value. From this data there is 100% yield on M1, M2 and the MetPass (top Al pad) structures. The specification for this design is 900V, which it should be able to survive, but the available test equipment was only able to go to 20V.

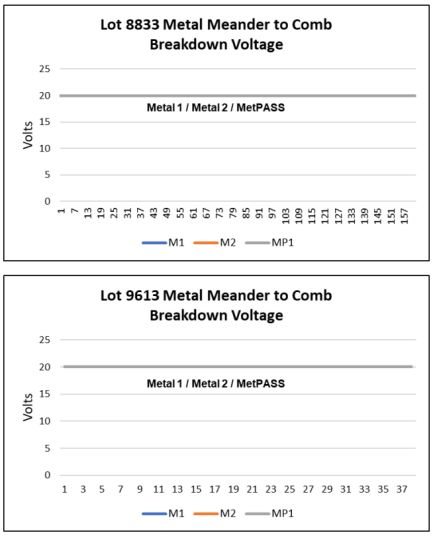

Figure 13: Metal meander comb breakdown voltage test results for M1, M2 and MetPass (top Al pad) structures.

The electrical testing results of the Phase I damascene process indicate a high yielding and robust process flow. The baseline design rules for this process can support line/space dimensions of 0.9 microns/0.9 microns for the Cu routing metal layers. In addition to being incorporated into Si interposers with TSVs, this process capability can also support the fabrication of bridge interposers that can be incorporated into a variety of substrate and fanout wafer level packaging architectures to enable high-speed chip-to-chip communication.

PHASE II TSV FILL LEARNING

In Phase II of the interposer development, a TSV is incorporated along with the Phase I topside Cu damascene routing layer buildup structure. In this process a blind via of dimension 10um diameter is etched into a full thickness 200mm-diameter Si-wafer with the Bosch DRIE process. Thin-film deposition processes are used to deposit passivation, diffusion

barrier, and electroplating seed metal layers into the via. These processes are developed to provide continuous films throughout the depth of the high-aspect ratio via, providing isolation of the Cu in the TSV from the Si substrate along with good adhesion. A bottom-up Cu electroplating process is used to fully fill the TSV. The Cu plating process is a critical portion of the overall flow, requiring a void-free fill through the entire depth of the via. The results after plating are shown in Figure 14 and higher magnification images of the top, middle, and bottom of the Cu-plated TSV are shown in Figure 15.

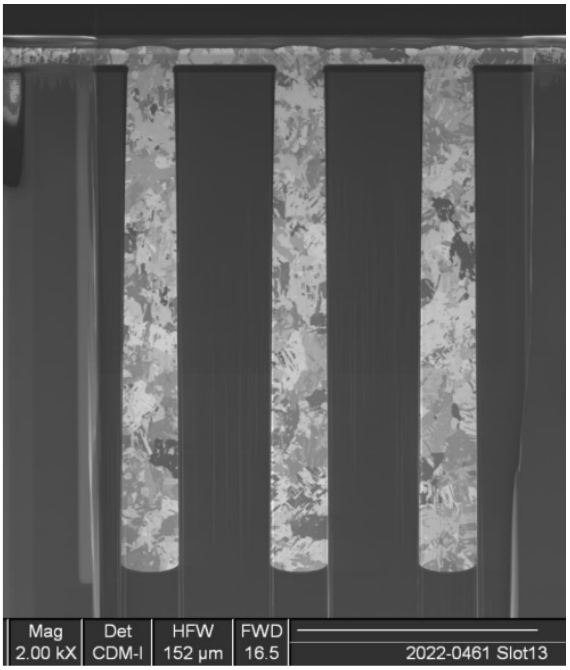

Figure 14: As-plated Cu TSV in a blind via.

These images illustrate fully filled TSVs with fine, equiaxed grains and no seams or voids, indicating a well-controlled bottom-up fill process.

SUMMARY

Through the IBAS program, we have successfully installed and performed initial electrical qualification for the Phase I Cu damascene process, which can be used to support bridge interposer applications. The program is currently in Phase II with the integration of the TSV and Cu damascene processes scheduled to be completed in late 2022.

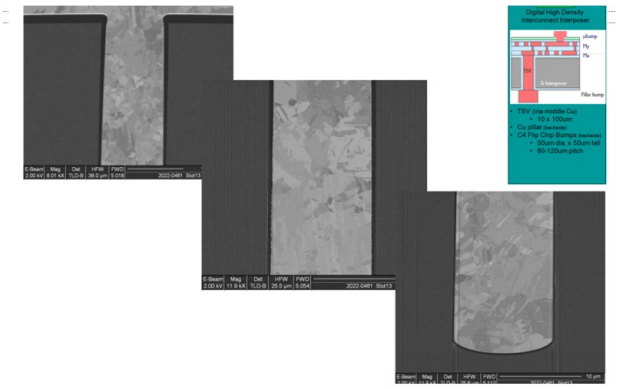

Figure 15: High magnification micrograph of the top, middle, and bottom sections of the as-plated Cu TSV.

The Phase II interposer offering will be a fully process design having TSVs that can be assembled to a standard organic substrate. Our partnership is currently designing a 30mm x 40mm Si interposer test vehicle demonstrator, that will incorporate multiple daisy chained die assembled to the topside using solder capped Cu-pillars and conventional C4 bumps on the bottom side to connect to a mating substrate, as shown in Figure 16. This test vehicle will provide the opportunity to characterize the reliability of a fully assembled exemplar system and serves as a "pipe cleaner" ahead of a functional system demonstrator.
The continuing development and advancement of this interposer technology in the IBAS program, the test vehicle program, as well as future programs, will establish SkyWater and BRIDG to provide an open access interposer capability for commercial and government customers.

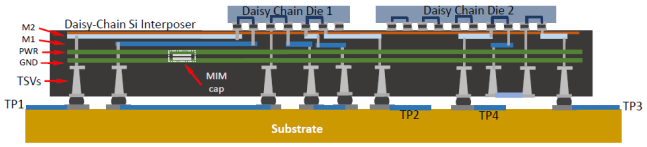

Figure 16: A schematic of the daisy chain test vehicle to generate yield and reliability data.

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