

Cu Conductive Paste as Via Filling Materials for Various Substrates

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ABSTRACT

In this study, we developed a Cu paste that can be used as a filling material for through silicon via (TSV), through glass via (TGV), and organic substrates. Non-through holes with diameters ranging between 20 and 100 μm and depths ranging between 70 and 100 μm (aspect ratios from 1 to 3.5) formed in a silicon surface layer were filled with Cu paste. TGV substrates with diameters ranging between 30 and 90 μm and thickness of 300 μm were filled with Cu paste without cracking. Multilayer substrates with the diameters of 180 and 260 μm and a thickness of 6.4 mm (aspect ratios: 25, 36) were filled with Cu paste without cracking. The 2.5D chip package was prepared using a TSV filled with Cu paste as a 2.5D interposer. The 2.5D chip package was verified through reliability test [thermal cycle test (TCT), high temperature storage test (HTST), un-bias high accelerated stress test (HAST) and pressure cooker test (PCT)]. After the reliability test, the conductive resistance of the package that adopted the Cu paste was found to be within 10% of the initial value. Moreover, we found that Cu paste can be applied to 2.5D interposer as filling material.

Key words: Low-temperature metallization, Cu paste, Via filling, TSV, TGV, Organic substrate

INTRODUCTION

Three-dimensional integrated circuits (3D ICs) and 2.5D ICs with silicon or glass interposers are considered to be promising candidates for overcoming the limitations of Moore's law owing to their advantages of low power consumption and high function density¹⁻²⁾. An interposer is a rigid insulator layer that serves as an interface between the high I/O of various logic and memory dies and lower-density substrate.

Through silicon vias (TSVs) and through glass vias (TGVs) are used in advanced 3D packaging solutions, such as the wafer-level packaging of microelectromechanical systems (Fig. 1 a), as well as silicon or glass interposers³⁻⁶⁾ (Fig. 1 b). Cu is preferred as the filling material in TSVs and TGVs owing to its superior capability of filling large structures and its excellent electrical conductivity. Cu filling by electroplating is one of the core and critical procedures in TSV and TGV fabrication. To reduce the number of voids in plated Cu, various studies have been conducted on plating conditions and additives⁷⁻⁹⁾. However, the plating of the

larger TSV and TGV structures often results in voids in the Cu filling, relatively thick outer surface layer plating, and low productivity.

Therefore, we investigated the filling of vias of TSVs and TGVs with high aspect ratios using Cu paste, which results in few voids suppressing thick outer surface layer plating and provides high productivity. Additionally, we examined the use of Cu for filling holes on organic substrates because this Cu paste can be sintered at lower 230 $^{\circ}\text{C}$. Assumed application items of the Cu paste are shown in Fig. 2. We are targeting TSVs and TGVs in Fig. 2(a), as well as hole filling and electrode formation in package substrates (Fig. 2b) and high multilayer organic substrates (Fig. 2c).

EXPERIMENTS

Process and Examination Items

Volume Resistivity Measurement

To investigate the effect of sintering conditions, Cu films with a thickness of 60 μm were prepared and the volume resistivity was measured. Cu film formation conditions are presented in Table 1.

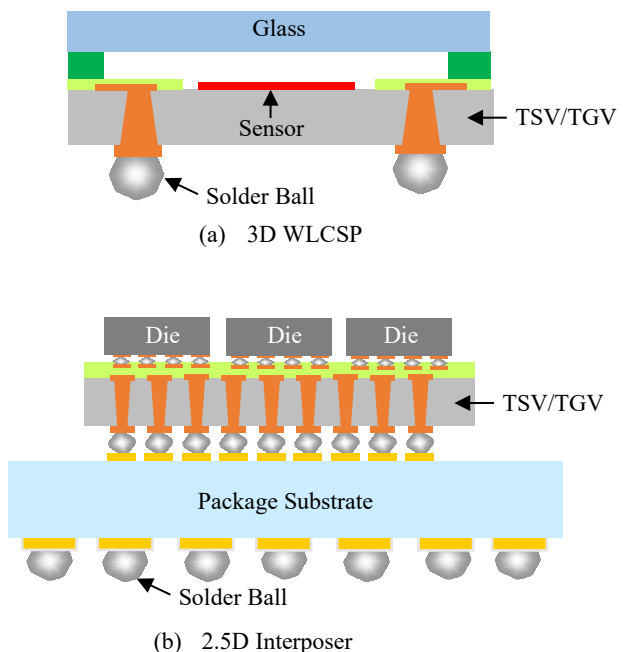


Figure 1. 3D Integration Technology.

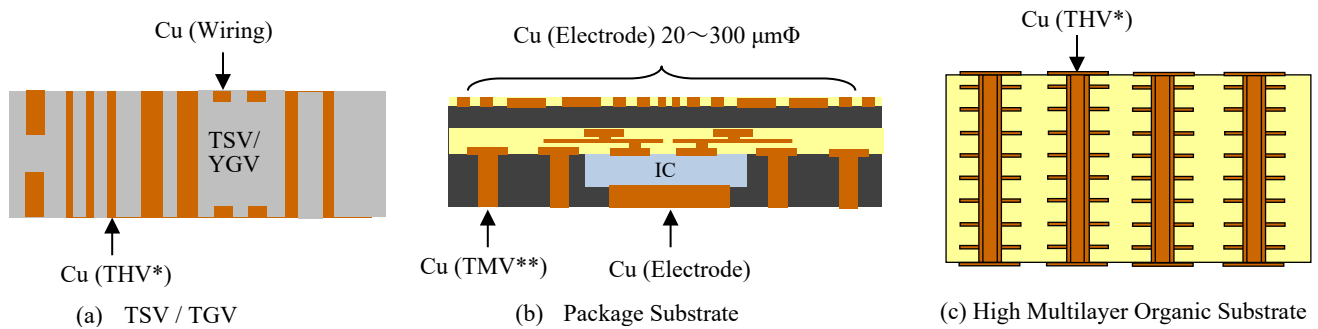


Figure 2. Assumed Application Items of Cu Past. THV: Through Hole Via, TMV: Through Mold Via

Table 1. Cu Film Formation Conditions.

Test Items	Details
Cu Paste	A, B
Sintering Temperature	150-400 °C
Sintering Conditions	Formic Acid, H ₂

Via Filling Evaluation on Various Substrates

The process and examination items are presented in Table 2. Three types of substrates were prepared by via filling.

Table 2. Process and Examination Items.

No.	Substrate	Kind of Via	Via Size (μmφ)	Via Depth (μm)	Aspect Ratio	Via Filling Method	Sintering Condition
1	Si	Non Through Hole	20-100	70-100	1-3.5	Printing	Formic Acid 220 °C (1 h)
2	Glass	Through Hole	30, 60, 90	300	3.3-10	Press	Formic Acid 220 °C (1 h)
3	Organic Substrate	Through Hole	180, 260	6400	25, 36	Press	H ₂ 220 °C (1 h)

(1) Si (TSV) – Non-through hole

Non-through holes with a diameters ranging between 20 and 100 μm and depths ranging between 70 and 100 μm (with aspect ratios from 1 to 3.5) formed in a silicon surface layer were filled with Cu paste. The overview of the Si wafer is shown in Fig. 3. A schematic of the vacuum printing method is shown in Fig. 4(a). The Cu paste was printed using a squeegee under vacuum and sintered at 220 °C for 1 h under a formic acid atmosphere.

(2) Glass (TGV) – Through hole

TGV substrates with a diameter of 30, 60, 90 μm and a thickness of 300 μm were filled with Cu paste. The overview of the glass wafer is shown in Fig. 5. A schematic of the press printing method is shown in Fig. 4(b). Cu paste was applied to a PET film and pressed at a pressure of 0.3 MPa. The TSV substrates were sintered at 220 °C for 1 h under a formic acid atmosphere.

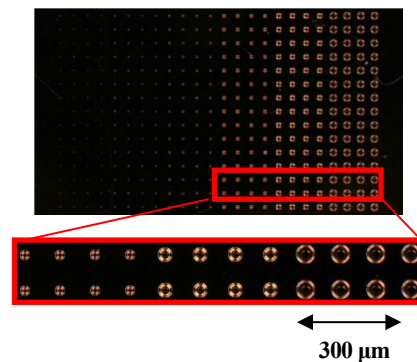


Figure 3. Over View of Si Wafer

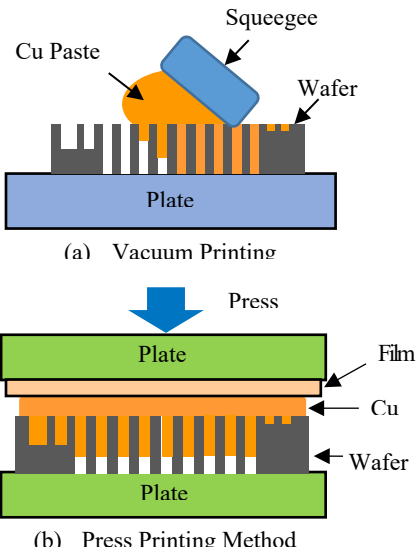


Figure 4. Process of Filling Holes by Cu Paste.

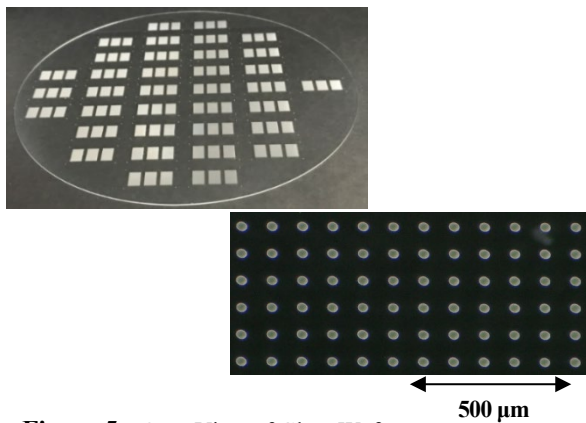


Figure 5. Over View of Glass Wafer.

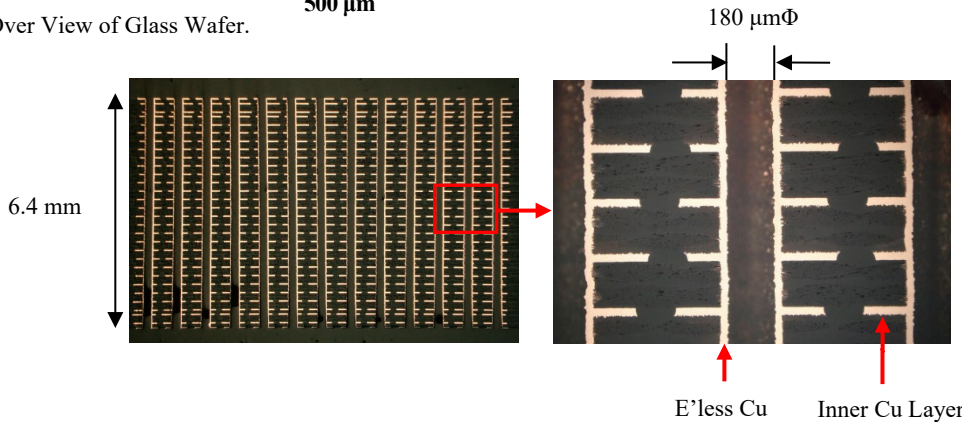


Figure 6. Cross Sectional Images of High Multilayer Organic Substrate. (Before Via Filling)

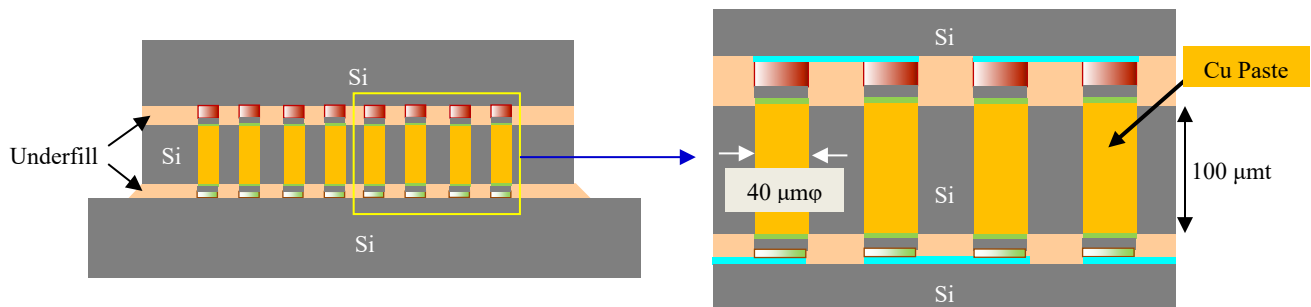


Figure 7. Cross sectional Image of 2.5D Integration with Through Si Interposer.

(3) Organic substrate – Through hole

Multilayer substrates with a diameters of 180, 260 µm and a thickness of 6.4 mm were filled with Cu paste. Multilayer substrates with side walls of vias shielded by an electroless Cu plating film were used. The cross sectional images of high multilayer organic substrate (before via filling) are shown in Fig. 6. Cu paste was applied to a PET film and pressed at a pressure of 0.3 MPa. Multilayer substrates were sintered at 220 °C for 1 h under a hydrogen atmosphere.

2.5D Integration with TSV Interposer

The cross sectional image of 2.5D integration with through Si interposer is shown in Fig. 7. TSV substrates with a diameter and thickness of 40 µm and 100 µm, respectively, were filled with Cu paste. The Cu paste was printed using a squeegee under vacuum and sintered at 220 °C for 1 h under a formic acid atmosphere. The Cu surface filled in the via of the TSV substrates was coated with electroless Ni (5 µm)/Au (0.05 µm) (ENIG: electroless Ni/immersion Au) plating. Si wafers with Cu pillars capped with Sn-3.5Ag and TSV substrates were connected by passing them through a nitrogen-reflow furnace. Subsequently, a Si wafer with electrodes formed with electroless ENIG plating and the TSV substrates were connected by a Sn-3.0Ag-0.5Cu (SAC305) solder paste passing through a nitrogen-reflow furnace. Finally, the underfill material was applied to both the sides of the TSV substrates. The 2.5D chip package was subjected to reliability test (TCT, HTST, HAST and PCT). The detailed test conditions are presented in Table 3.

Table 3. Reliability Test Conditions.

Test Items	Details
TCT	-55 °C, 125 °C / 1000 cycles
HTST	150 °C/1000 h
HAST	130 °C, 85%RH / 96 h
PCT	121 °C, 100%RH / 96 h

RESULTS AND DISCUSSION

Volume Resistivity of Cu Films

The volume resistivity of Cu films as a function of sintering temperature and atmosphere is shown in Fig. 8. The volume resistivity varies significantly depending on the types of Cu paste. Comparing the atmosphere of formic acid and hydrogen in paste A, hydrogen is effective in obtaining lower volume resistivity Cu film. In the case of paste B at 225 °C above, lower volume resistivity film was obtained in the hydrogen atmosphere compared to that in the formic acid atmosphere. It showed the film with the lowest volume resistivity of approximately 3.5 μΩ·cm was obtained at 350 °C or higher in hydrogen atmosphere. In the case of paste B at below 200°C, it was found that, compared to hydrogen atmosphere, formic acid atmosphere is effective in obtaining lower volume resistivity Cu film. The condition with the lowest volume resistivity at 150°C was at formic acid atmosphere and paste B.

Cu Filling State Based on Substrate Type

(1) Si (TSV) – Non-through hole

Cross-sectional images of the TSV filled with Cu paste are shown in Fig. 9. The enlarged view of each via in Fig. 9 is shown in Fig. 10. The holes can be filled with Cu paste regardless of via diameter and depth. In fact, the vias with a

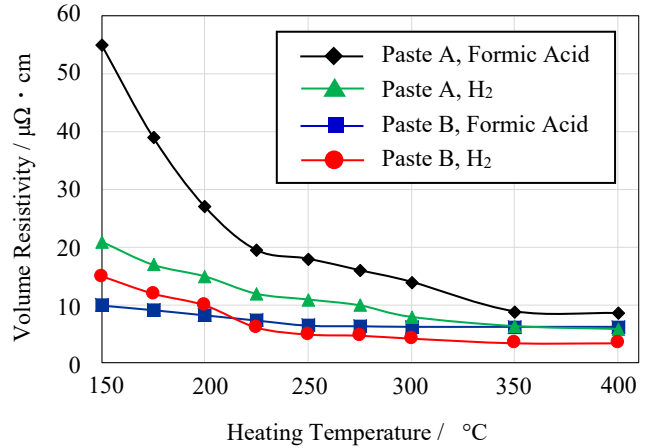


Figure 8. Volume Resistivity of Cu Films as a Function of Sintering Temperature and Atmosphere.
Cu Paste: A, B
Sintering Atmosphere: Formic Acid, H₂

small diameter and high aspect ratio (via diameter: 20 μm, aspect ratio: 3.5) can be filled with Cu paste without inducing cracks or voids. Via opening was flat regardless of the via volume ratio. We infer that the CMP process can be omitted using the Cu paste.

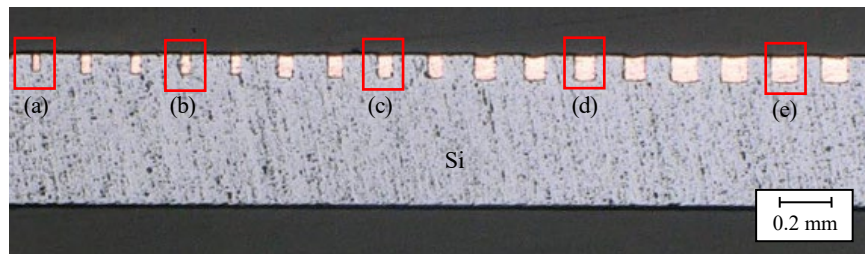


Figure 9. Cross-sectional Images of TSV Filled with Cu Paste.
Via Diameter: (a) 20 μm, (b) 30 μm, (c) 50 μm, (d) 70 μm, (e) 100 μm
Metallization Atmosphere: Formic Acid, Temp.: 220 °C, Heating Time: 1 h

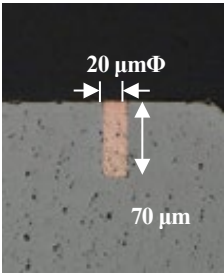
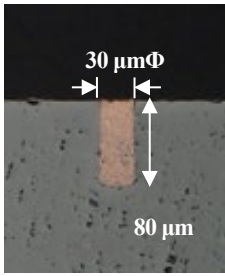
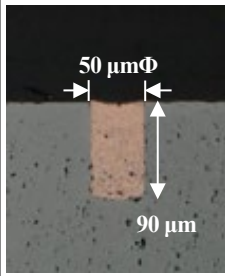
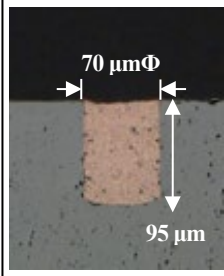
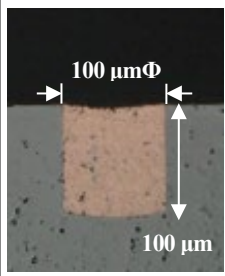
Item	Enlarged Point of Fig. 9				
	(a)	(b)	(c)	(d)	(e)
Via Diameter (μm)	20	30	50	70	100
Cross-sectional Images					
Volume Ratio	1	3	8	17	36

Figure 10. Cross-sectional Images of TSV Filled with Cu Paste.
Metallization Atmosphere: Formic Acid, Temp.: 220 °C, Heating Time: 1 h

(2) Glass (TGV) - Through hole

TGV substrates with a diameter of 30, 60, 90 μm and a thickness of 300 μm were filled with Cu paste. TSVs with a small diameter and high aspect ratio can be filled without inducing cracks, as shown in Fig. 11. In regard to the TGV (Fig. 11), the via diameter at the center of the substrate was narrower than the opening diameter, and the vias were filled with Cu paste without inducing cracks.

(3) Organic substrate - Through hole

Multilayer substrates with a diameter of 180, 260 μm and a thickness of 6.4 mm were filled with Cu paste (Fig. 12). Fig. 13 shows an enlarged view of the central part and opening of the cross section of multilayer substrates with a diameter of 260 μm . As shown in Fig. 13, Cu paste can be formed without cracking, even when using a thick and high-aspect ratio organic substrate. Therefore, we conclude that Cu paste can be applied to substrates that require a high current density and high heat dissipation.

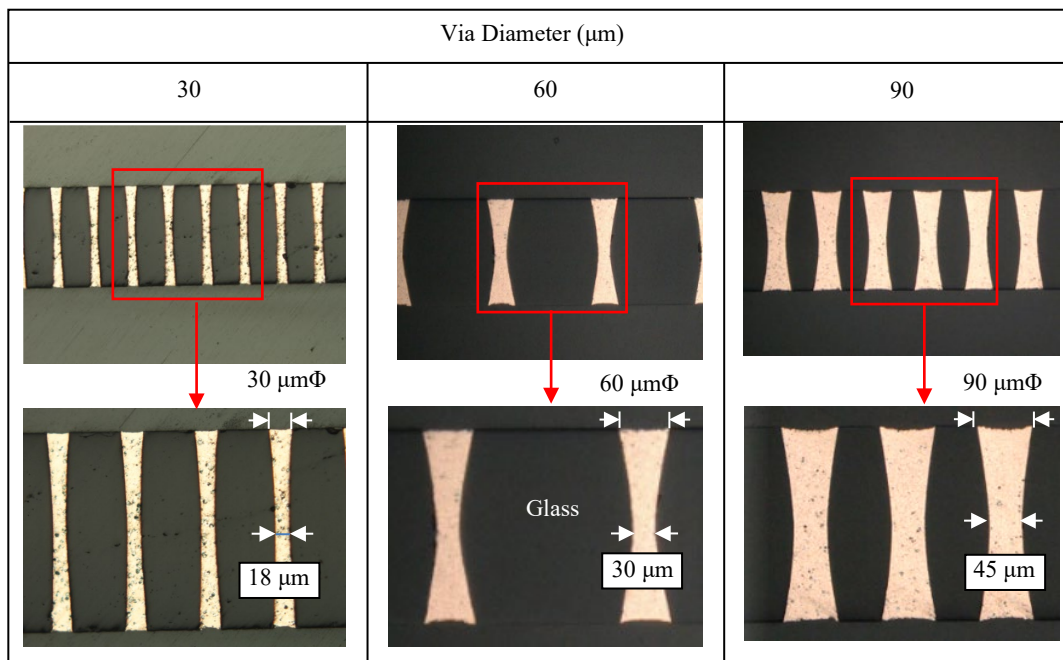


Figure 11. Cross-sectional Images of TGV Filled with Cu Paste.
Metallization Atmosphere: Formic Acid, Temp.: 220 °C, Heating Time: 1 h,
Thickness: 300 μm

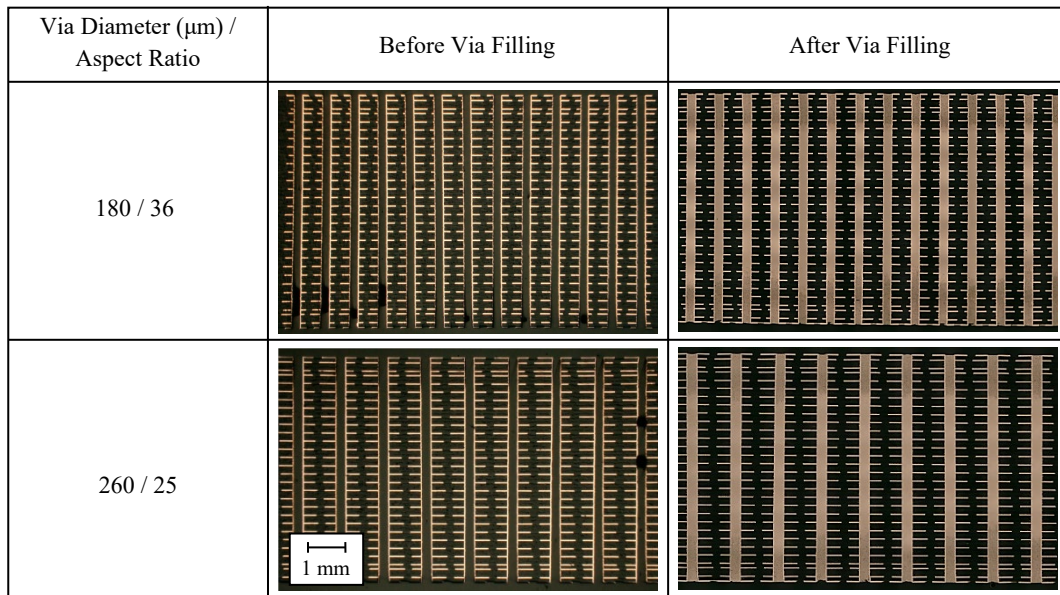


Figure 12. Cross-sectional Images of High Multilayer Organic Substrates Filled with Cu Paste. Metallization Atmosphere: H_2 , Temp.: $220\text{ }^\circ\text{C}$, Heating Time: 1 h Thickness: 6.4 mm

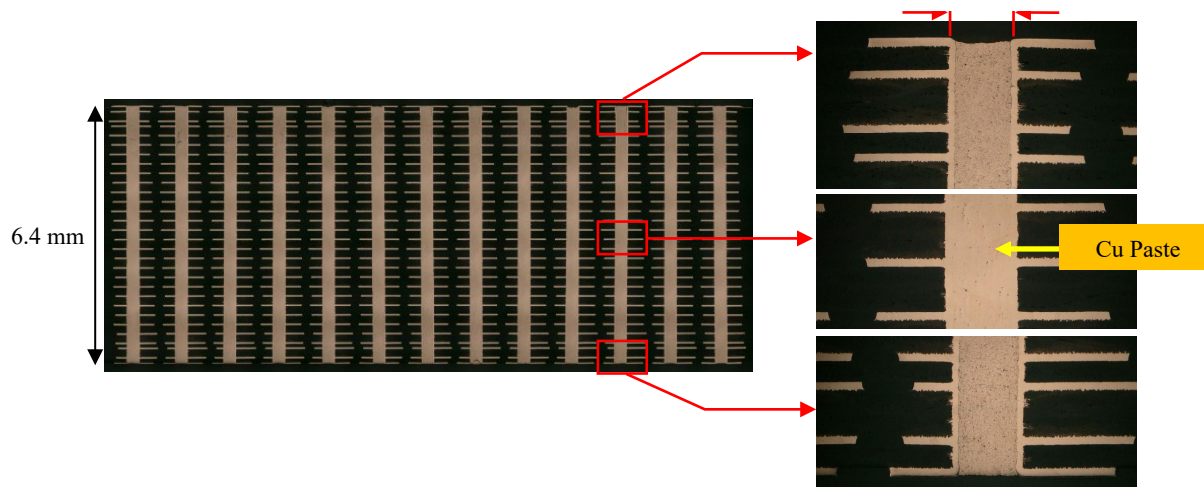


Figure 13. Cross-sectional Images of High Multilayer Organic Substrates Filled with Cu Paste. Metallization Atmosphere: H_2 , Temp.: $220\text{ }^\circ\text{C}$, Heating Time: 1 h Thickness: 6.4 mm, Via Diameter: $260\text{ }\mu\text{m}$

2.5D Integration with TSV Interposer

TSV substrates with a diameter and thickness of $40\text{ }\mu\text{m}$ and $100\text{ }\mu\text{m}$, respectively, were filled with Cu paste. The overview and cross-sectional images of the TSV substrate are shown in Fig. 14(a). The vias were filled with Cu paste, and no cracks were observed. The overview and cross-sectional images of the TSV substrate applied with ENIG on the Cu surface are shown in Fig. 14(b). The electroless Ni plating film was deposited directly on the Cu paste, and no extraneous deposition was performed on the Si wafer. The 2.5D chip package was prepared using a TSV-plated

substrate as a 2.5D interposer. The overview and cross-sectional images of the electrodes connected via soldering are shown in Fig. 14(c). It was found that, the Cu-filled vias plated with ENIG were joined by soldering, and no peeling occurred between the Cu paste and the electroless Ni plating film. The underfill material is applied to both the sides of the TSV substrates. The 2.5D chip package was subjected to reliability test and the conductive resistance changing rate was within 10% in all tests. The TCT results were specifically shown in Fig. 15. We found out that Cu paste can be applied to 2.5D interposer as filling material.

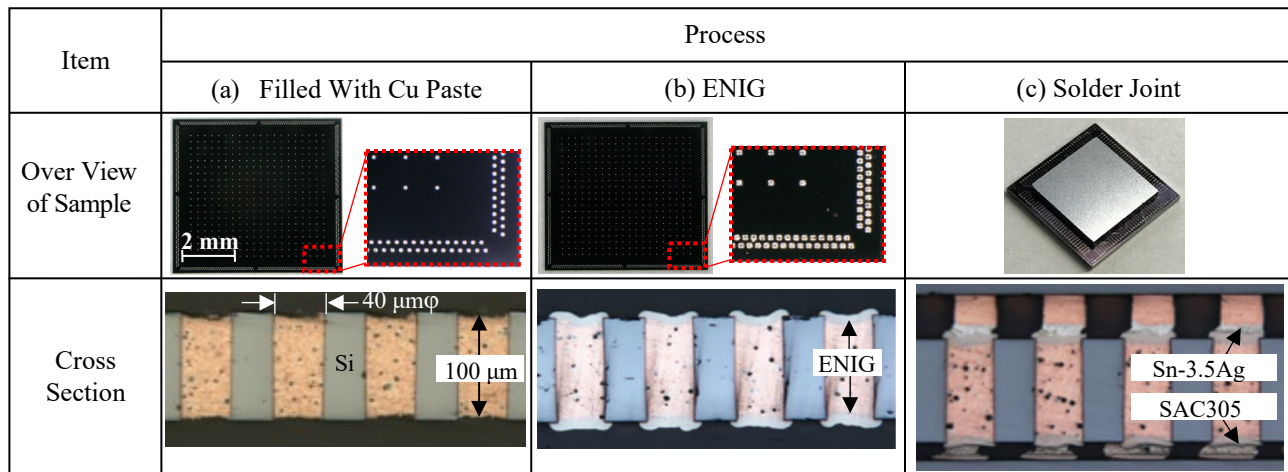


Figure 14. 2.5D Integration with Through Si Interposer.

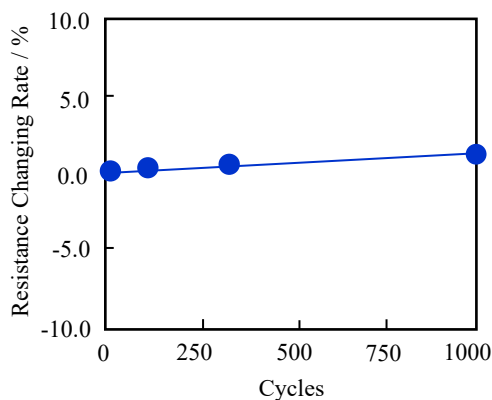


Figure 15. TCT Results of 2.5D Chip Package.

CONCLUSION

We developed a Cu paste that can be used as a filling material for TSVs, TGVs, and organic substrates. The following key conclusions are obtained:

- (1) The film with the lowest volume resistivity of approximately $3.5 \mu\Omega \cdot \text{cm}$ was obtained at 350°C or higher in hydrogen atmosphere.
- (2) Non-through holes with diameters of $20\text{--}100 \mu\text{m}$ and depths of $70\text{--}100 \mu\text{m}$ (aspect ratios from 1 to 3.5) formed in a silicon surface layer were filled with Cu paste.
- (3) TGV substrates with a diameter of $30, 60, 90 \mu\text{m}$ and a thickness of $300 \mu\text{m}$ were filled with Cu paste without inducing cracks.
- (4) It was found that Cu paste can be formed without inducing cracks even when using a thick and high-aspect-ratio organic substrate (thickness: 6.4 mm ; aspect ratio: 25, 36).
- (5) The 2.5D chip package was prepared using a TSV filled with Cu paste as a 2.5D interposer. After the reliability test, the conductive resistance of the package was found to be within 10% of the initial value. We found out that the Cu paste can be applied to 2.5D interposer as filling material.

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