Comparative Study for Solder Joint Performance Under Shock for ENIG and ENEPIG Surface Plated Tester PCBs

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ABSTRACT
Printed Circuit Boards (PCBs) - for Intel tester platforms such as HDBI (High Density Burn-In Tester); HDMT (High Density Modular Tester); XPV (Platform Validation Tester) uses Electroless Nickel and Immersion Gold (ENIG) as surface finish to prevent oxidation of copper pads and improve solderability. However, ENIG plated PCBs periodically exhibit two key failures during board assembly: Solder dewet or no wetting of the solder to the ENIG surface finish and Solder Joint Cracks (SJCs) or separation from the nickel layer surface causing an electrical open. The periodicity of assembled boards failures - with ENIG plated boards and its cost impact to Intel manufacturing - was the motivation to investigate an alternative PCB plating solution with a higher margin to failure under shock stress. This paper discusses the results of a comparative study for solder joint performance - under shock - for ENIG and ENEPIG surface plated tester PCBs.

Key words: PCB surface plating; Solder Joint failures; ENIG; ENEPIG; IMC; SMD; NSMD.

INTRODUCTION
Intel designs and manufactures its own testers, which are critical to meet Intel products outgoing quality and reliability targets. Intel testers need to survive continuous stress derived from High Volume Manufacturing (HVM). Testers have high expectations for stability and availability during HVM, which require testers with high quality and reliability. Intel testers are composed of three main hardware components: chassis, controller, and modules or instruments. Modules or Instruments are two Assembled Printed Circuit Boards (PCBA) integrated with a cold plate (a metal component that works as cooling solution). Printed Circuit Boards (PCBs) – for Intel tester platforms – use mainly Electroless Nickel Immersion Gold (ENIG) - as surface finish - due to its multiple advantages, for example support for fine-pitch BGA components for component placement and solderability due to pad coplanarity. However, ENIG plated PCBs periodically exhibit two key failures in tester manufacturing process: Solder dewet or lack of wetting of the solder to the ENIG surface finish and Solder Joint Cracks (SJCs) or separation from the nickel layer surface causing an electrical open. The SJCs failures are seen not only during shock and vibration reliability tests, which are intended to qualify tester boards for survival under shipment use conditions, but also during repair of production tester boards.

An example of a Solder Joint Crack Failure is shown in Figure 1, where a crack is observed between the Inter-Metallic Compound (IMC) and Nickel (Ni) interface. Figure 2 shows a typical joint microstructure. There are multiple interfaces in a solder joint microstructure. Each interface is denoted as T1, T2, T3, T4 to help identify the location of a crack interface within a solder joint microstructure. In addition, coloring is used to identify the Tx interface at which the crack occurred. For example, in Figure 2a, yellow colored board pads indicate that the solder joint cracks were observed at ball/pad interface, also called T3 interface. Similarly, the green-colored pads indicate that solder joint cracks were observed at pad/PCB interface or T4 interface, as shown in Figure 1b.

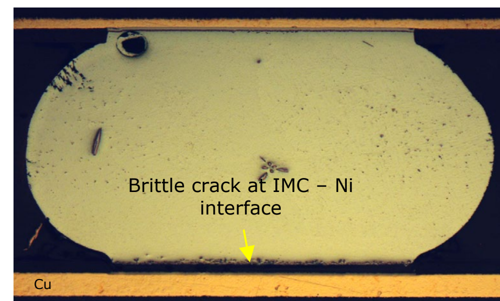


Figure 1. An example of a solder joint crack cross-section.

Tester boards use two types of solder land designs. They are Solder Mask Defined (SMD) and Non-Solder Mask Defined (NSMD) also called Metal Defined lands. There are differences in solder joint formation in SMD and NSMD lands [1], which may have an impact on solder joint performance under shock and vibration.

Solder Mask Defined (SMD) lands require larger diameter metal pads to achieve same diameter of solderable land as NSMD lands, because of the over-lapped solder mask. Since the molten solder cannot wet the solder mask surface, the geometry of the solder joint will be affected, with higher stress created at the point where the solder mask opening edge contacts the solder joint. This stress raising point may decrease the solder joint performance under shock when compared to NSMD lands.

NSMD lands requires a small diameter Cu land; the absence of solder mask around the solder land allows the solder to flow around the edges of the lands, into the `trench` created by the edges of the metal land and the solder mask, thereby eliminating any areas of stress concentration for the solder joint. NSMD lands make the solder joint wider giving a stronger response under shock and vibe [1]. Figure 3 describes NSMD and SMD Lands.

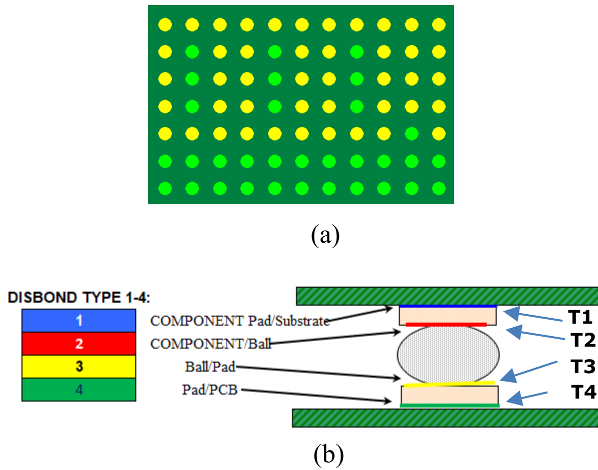


Figure 2. An example of a solder joint microstructure (a) The color of pads indicates the location of crack within the solder microstructure (b) Interfaces within a solder joint microstructure.

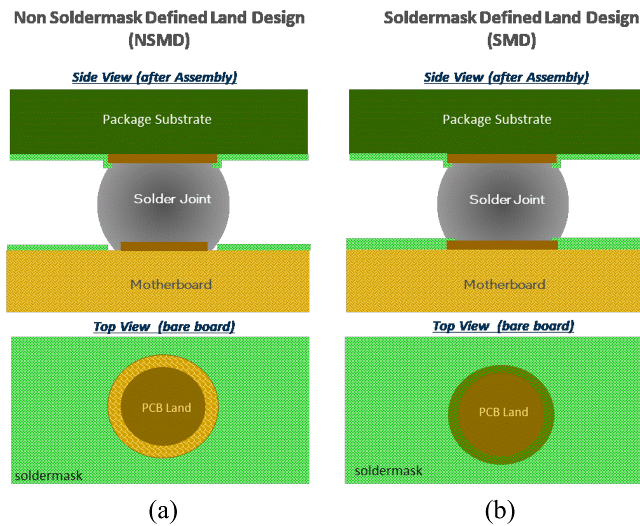


Figure 3. Two solder land designs are used in Intel tester boards. (a) NSMD Pads and (b) SMD Pads.

During development of HDBI testers, solder joint cracks were observed on HDBI MB tester boards post shipment and after shock and vibration experiments. The solder joint cracks' location had a dependency on solder land design (either SMD or NSMD), as shown in Figure 4. SMD pads exhibited brittle cracks at T3 interfaces (within the bulk solder joint), whereas NSMD pads exhibited cracking at T4 interfaces. This failure mode is characterized by cracking of the PCB laminate under the land and is termed `pad cratering`. Thus, the likely root causes of SJCs with brittle cracks (at T3) and pad cratering (at T4) were distinct.

Finding the root cause for these two different failing mechanisms required further data collection from HDBI boards that exhibited failures after shipment. – were directed to Failure Analysis (FA). Detailed Failure analysis of these boards discovered two critical findings:

1. The T3 crack surface presented a distinct dot-like signature.
2. The T3 interface showed signs of mud-cracks and black spots.

Let's analyze each finding individually. Further analysis revealed that the dot-like signature on solder joint cracked surface, at T3 interface shown in Figure 5b, was due to the Phosphorus (P) in the nickel layer. The dots found on crack surface were P-rich. But where does the P originate from? The electroless nickel-plating method does not deposit pure Ni, but a mixture of Nickel and Phosphorous (Ni-P). During the assembly process, when the solder joint forms, the Ni atoms diffuse into the Sn matrix and form a thin Inter-Metallic Compound (IMC) layer with the Sn atoms. Since the P atom does not participate in this reaction, the P element concentration the Ni layer just under the IMC would gradually increase. This specific structure, with high P element concentration, is called the P-rich layer [2]. Because of the weak bonding of this P-rich layer resulting from Ni depletion to the IMC layer, a low shear stress would be enough to crack the ENIG solder joint [3]. Additional studies indicate that the solder joint fractures at P-rich layer [4]. The brittle fracture at the interface results from the weak adhesion of P-rich layer and/or nanovoids formed in the Ni-Sn-P Layer [3-5]. Figure 5a represents the location of Ni-P enriched zone.

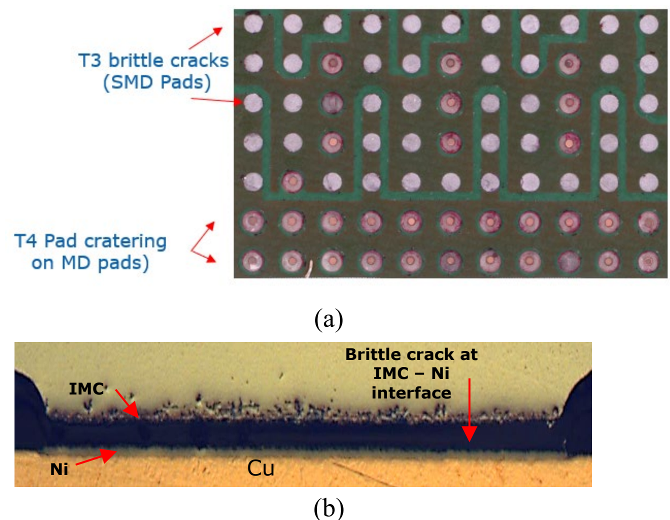
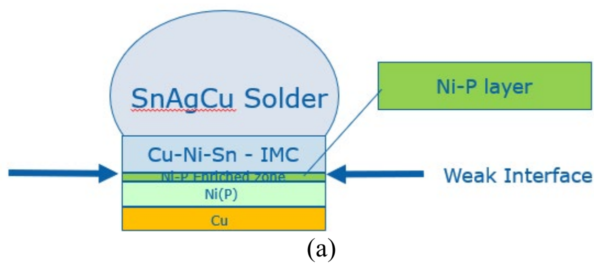


Figure 4. Solder joint cracks signature have a dependency on solder land design (a) SMD Pads presented T3 brittle cracks. NSMD Pads showed T4 pad cratering. (b) T3 brittle cracks seen at IMC – Ni (P) interface.



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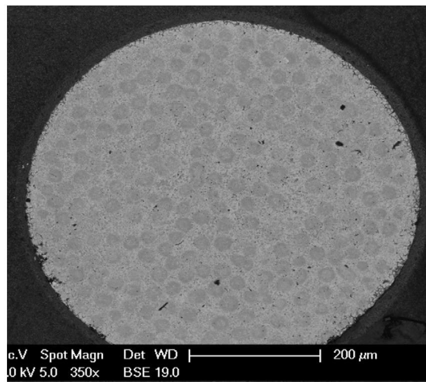
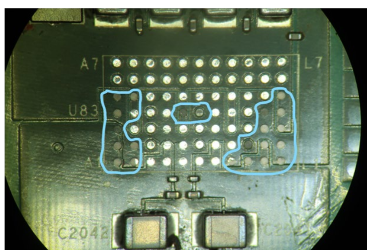


(b)

Figure 5. Post-reflow solder joint formation. (a) A Ni-P rich layer formation between SnAgCu Solder and IMC creates a weak interface leading to T3 brittle cracks. (b) A P-rich dot like signature observed on T3 brittle cracked surface.

When a tester board fails in production, the boards undergo repair at Intel Manufacturing Repair (IMR). IMR is an Intel Organization in charge of the repair of all hardware used at Intel Sort and Assembly Technology Manufacturing (ATM) Test Sites. IMR reported an increased number of HDBI MB boards failing due to opens in HDBI MB board components. Ball Grid Array (BGA), Low Temperature Module (LTM) components were seen failing more frequently. During repair of HDBI MB boards - for open failures - IMR observed black pads, as shown in Figure 6. A closer examination of the black pads found signs of mud-cracks and black spots, as seen in Figure 6c. The mud crack morphology and the presence of black spots degrades the solderability of the PCB pads, leading to a unacceptable wetting of the solder joints [6]. The two defects reveal a poor solder joint quality and this required further investigation.



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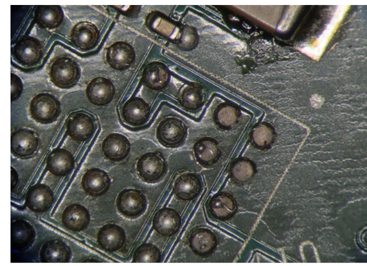

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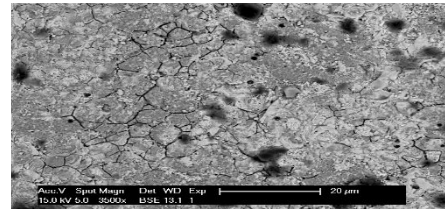


(c)

Figure 6. HDBI MB pads on repaired production boards (a) Black pads. (b). Black pads close-up. (c) Mud cracks and black spots seen on pads under higher magnification.

In summary, Solder Joint Crack (SJC) failures seen in HDBI MB assembled tester boards, post shipping and post vibration and shock tests, mainly on BGA LTM components, were due to multiple root causes. Finding a solution required creating multiple hypothesis to find answers for each separately.

1. Pad cratering solder joint failures at T4 interface, on NSMD pads, were likely due to mechanical overstress. The potential solution resides on a reduction of excessive stress by re-design of the shipping box. In addition, the thermal solution and handling of HDBI MB boards requires the attachment of mechanical hardware. This hardware increases the inertia of the HDBI MB by 2X leading to a higher energy applied to solder joints during Shock and Vibration (S&V) experiments. Furthermore, the added mechanical hardware creates areas with high stress concentration on HDBI MB surfaces where BGA LTM components are located. Taking these facts into consideration, the solution to pad cratering resides on re-designing the shipping box to protect the HBDI MB from induced stress during S&V experiments and shipment. A redesigned shipping box resulted in elimination of pad cratering failures.

2. Even with a redesigned box, which reduced stress induced to HDBI MB boards, solder joint cracks at T3 interface, on SMD Pads, continued to occur under S&V stress. The SJCs failures at T3 interface were likely due to poor mechanical strength between IMC and Ni-P solder joint microstructure. This hypothesis was supported by the following observations:

a. Presence of a P-rich spot like signature on solder joint cracked surface, which indicated the presence of a P-rich layer with a tendency to break due to the brittle property of this layer [7].
b. Presence of black spots and mud cracks on solder joint cracked surface indicates poor PCB ENIG plating quality, which leads to weak solder joints that breaks under shock stress [6].

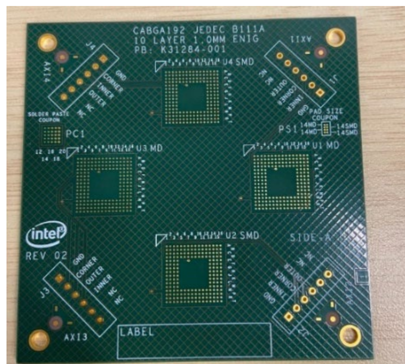
A solution with higher margin for solder joint cracks was desired for tester boards. Solder joints with ENIG plating provides a solution with minimal margin for solder joint crack failures. Intel Q&R looks for solutions with margin to survive stress from long term service (~ 8 years). Therefore, a study for solder joint performance for an alternative board plating solution was required. This paper discusses the results of a comparative study for solder joint performance, under shock stress, for ENIG and ENEPIG surface finish plated pads for Intel tester boards.

MATERIALS AND METHODS

In this paper, solder joint performance – under mechanical shock – was investigated for tester boards with two different surface finish on their pads - (Ni-P/Au) Electroless Nickel Immersion Gold (ENIG) and (Ni-P/Pd/Au) Electroless Nickel Palladium Immersion Gold (ENEPIG). Solder joint performance for these two surface finish plating technologies, will be compared by interface morphology, physical properties, and signal integrity differences.

Materials

The Board Test Vehicle (TV) was designed according to the JESD22-B111A standard [10] to evaluate solder joint performance under mechanical shock for ENIG and ENEPIG plated pads. Figure 7 shows pictures of the JEDEC TVs. Each TV board has four set of pads, as shown in Figure 7a. Two set of pads were SMD and the other two were NSMD pads. The solder joint was of SAC305 composition. The BGA lands on the TVs were plated with ENIG and ENEPIG surface finish. Both sets of TVs were manufactured at the same PCB supplier used to manufacture production HDBI MB boards. In addition, a set of HDBI MB boards were manufactured with ENIG and ENEPIG surface finish.



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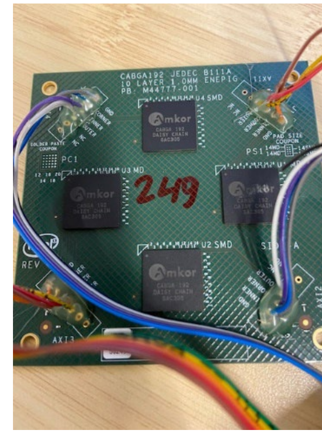

(b)

Figure 7. JESD22-B11A TV (a) 4 set of Pads are in each TV (b) Dummy components are assembled on each set of pads. Cables connect to an external data acquisition system.

Methods

The JEDEC Test Vehicles (TVs) were tested with a stress profile documented in JESD22-B11A [10]. The stress profile includes impact acceleration of 1500 Gs and a duration of 0.5 msecs. The experimental shock machine was calibrated to ensure the spec stress profile follows the spec requirements. The shock experiments were conducted by specialized Engineers at Intel Stress Labs located at Hawthorn Farms Campus in Hillsboro, OR. Figure 8 includes the lab setup for the Mechanical Shock Test. Resistance measurements were taken after each drop by a data acquisition system. The resistance threshold for failure was 1000 Ohms, as required by JESD22-B111A.

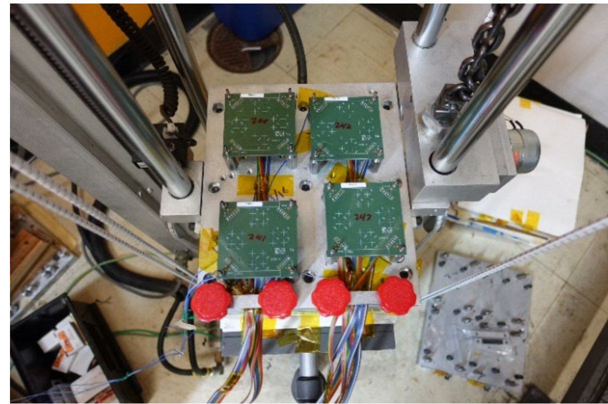

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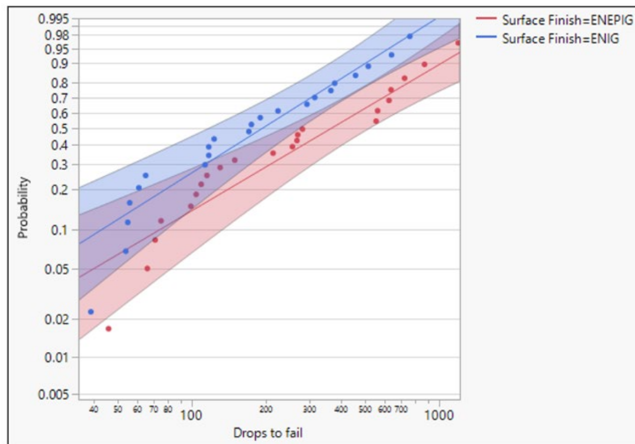
Figure 8. Shock stress for JEDEC TVs (a) Board TVs are mounted on a shock stress machine. (b) A calibrated shock stress machine is used to test TVs boards.

In addition to shock tests with JEDEC TVs, a set of production HDBI MBs boards, plated with ENIG and ENEPIG, were subjected to two sets of tests: 1. Packaged S&V DOEs; 2. Signal Integrity Analysis.

RESULTS AND DISCUSSION

The impact of PCB surface finish – ENIG and ENEPIG – on solder joint performance under mechanical shock, is shown in Figure 9, as Weibull Plots for component locations with NSMD land designs (Figure 9a) and SMD lands (Figure 9b). Table 1 summarizes the solder joint characteristic life (63% reliability values) for ENIG and ENEPIG by land design.



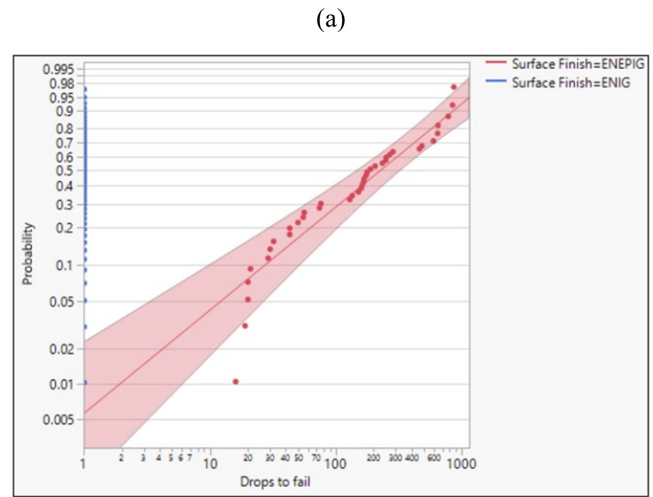
Statistics

Summary

Group	Number failed	Left Censor	Interval Censored Failure	Right Censored	Mean		Std Error
Surface Finish=ENEPIG	39	0	0	9	324.2604		44.53724
Surface Finish=ENIG	48	0	0	1	1	Biased	0
Combined	87	0	0	10	171.4242		28.59948

(a)

(a)



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(b)

Figure 9. Solder Joint life distribution for ENIG and ENEPIG solder joints by land design. (a) NSMD land designs. (b) SMD land design.

The solder joint life distribution or NSMD pads is shown in Figure 9a. The red line represents life distribution for ENEPIG plating. The blue line represents ENIG solder joint life distribution for ENIG plating. It requires ~ 40 drops to observe the first solder joint failure with ENIG and ENEPIG. The solder joint performance is summarized in Table 1. There is significant difference in the characteristic life of solder joints with ENIG and ENEPIG for NSMD lands. Data is clear that ENEPIG solder joint outperforms ENIG solder joints performance under mechanical shock stress for NSMD lands.

Table 1. Characteristic life (63% reliability values) for ENIG and ENEPIG solder joints by land design (NSMD & SMD).

Surface Finish (SF)	Land Design (LD)	
	NSMD	SMD
ENIG	**258**	**1**
ENEPIG	**500**	**337**

The solder joint life distribution for SMD pads is shown in Figure 9b. The red line represents solder joint life distribution for ENEPIG plated solder joints. The blue line represents solder joint life distribution for ENIG plated solder joints. All ENIG solder joints fail during the first drop cycle. This is the reason all the ENIG drop-to-fail values are in a vertical line at 1 value on the x axis. In contrast, the first solder joint failure for ENEPIG solder joints on SMD pads is observed at 20 drops. There is a significant difference in the characteristic

life of solder joints with ENIG and ENEPIG for SMD lands as shown in Table 1. All solder joints failed at 1 drop for ENIG on SMD lands. 63% of all solder joints failed at 337 drops for ENEPIG for SMD lands. This data clearly shows that ENEPIG solder joints outperform ENIG solder joints under mechanical shock stress for SMD lands.

Furthermore, the daisy chained CABGA192 components soldered on SMD lands with ENIG surface finish were completely de-attached from the board after the first drop cycle. These detached components are shown in Figure 10. This signifies that all 192 solder joints of the component were full cracked after the first drop cycle. On the other hand, 63% of all the ENIG plated solder joints – on NSMD lands – failed after 258 drops. The conclusion was that solder joints on ENIG MD lands outperforms solder joints on ENIG SMD lands under shock. ENEPIG solder joints outperform ENIG solder joints for both lands' designs (NSMD and SMD) under shock. The differences on solder joint performance for NSMD and SMD are due to solder joint formation for both land designs as explained earlier on this paper and as concluded in [1].

Figure 10. ENIG BGA dummy components were de-attached from board at first drop (for SMD pads). This is a catastrophic solder joint failure.

Intel tester boards use both land designs (SMD and NSMD). Therefore, for Intel use conditions, solder joints need to perform reliably on both land designs (SMD and NSMD). Solder joints on NSMD lands designs for ENIG and ENEPIG plating has margin to failure under shock. In contrast, solder joints on SMD lands for ENIG plating has no margin to failure under shock. Considering that tester boards' life in production should have a life of 7-10 years, during which the tester boards will be shipped from Intel manufacturing sites to Intel repair centers, it requires a solder joint solution with higher possible margin to failure to survive stress during shipment. Data reported in this paper, clearly shows that solder joints with ENIG, on SMD lands, is not a candidate for Intel manufacturing.

A closer examination of T3 solder joint crack surfaces – for SMD pads for the JEDEC TVs under shock – was conducted to understand root causes for the differences in solder joint performance between ENIG and ENEPIG plated solder joints. Figure 11a shows the crack surface of solder joint at T3 interface with ENEPIG plating. The surface does not show abnormalities. The surface is covered by solder material, which is the signature expected for a robust solder joint. In contrast, Figure 11b shows the cracked surface of the solder joint at T3 interface with ENIG plating. The crack is seen at T3 Ni-IMC interface. The cracked surface shows a dot like signature, with P-rich dots deposited on the Ni(P) surface. The observed dot-like signature, on the TV solder joint cracked surface, is like that observed on T3 cracked surface for solder joints on SMD Pads with ENIG for production ENIG HDBI MB boards.

(a)

(b)

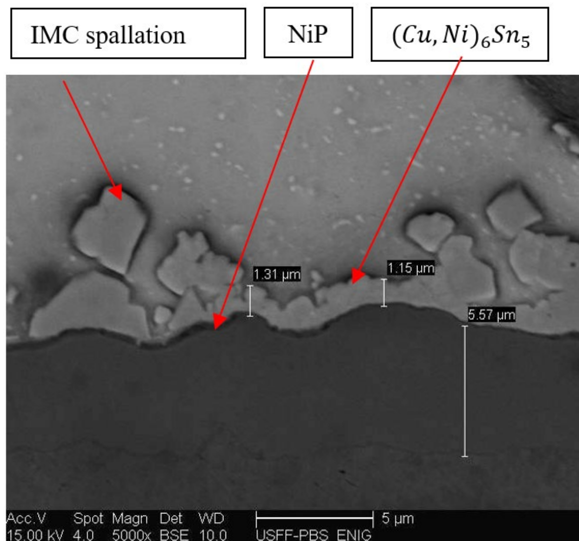
Figure 11. Solder Joint crack surface analysis at T3 interface for SMD Pads Pad surface analysis for ENEPIG and ENIG pads. (a) ENEPIG plated solder joint without P-rich spots. No P-rich spots on ENEPIG T3 interface. (b) ENIG plated solder joint shows P-rich spots.

The presence of a P-rich layer creates weak bonding. A low shear stress is required to crack the ENIG solder joint [2]. The brittle fracture at the interface results from the weak adhesion of P-rich layer and/or nanovoids formed in the Ni-Sn-P Layer [3-5].

The formation of a continuous and thin IMC layer, without spallation, is required to create robust solder joints. Figure 12 shows IMC layer formation – post board reflow – for ENIG and ENEPIG plated solder joints. Figure 12a shows the IMC layer for an ENIG Plated solder joint. Figure 12b shows IMC

layer for an ENEPIG solder joint. Key observations from these two figures include:

1. A thicker NiP layer is seen for ENIG IMC. A thinner NiP layer was seen with ENEPIG.
2. A thicker $(Cu, Ni)_6Sn_5$ layer for ENIG IMC was measured compared to ENEPIG.
3. ENIG IMC layer shows discontinuity. ENEPIG IMC shows continuity.
4. There are signs of spallation in ENIG IMC. ENEPIG IMC is clean of spallation.



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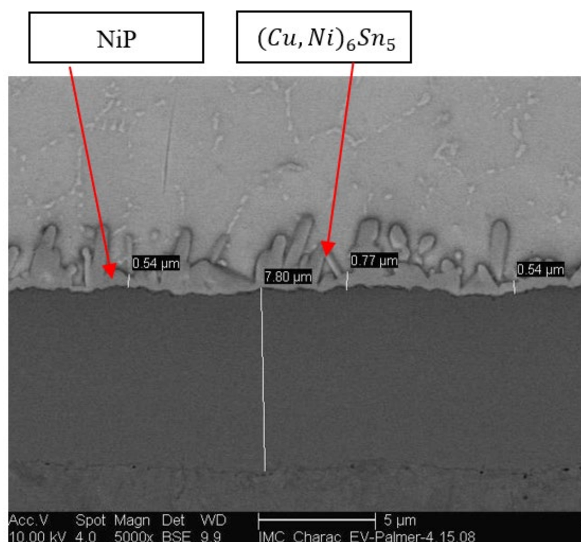

(b)

Figure 12. IMC comparison post reflow. (a) IMC with ENIG. (b) IMC with ENEPIG.

Solder Joint Reliability has dependency on IMC formation: A thinner IMC – with ENEPIG – with no spallation, continuous and with a thinner NiP result in a superior solder joint performance. Similar results were found after IMC characteristic analysis on HDBI MB production boards with ENIG and ENEPIG solder joints. Hence, it can be concluded that with ENEPIG, the addition of Pd suppresses interfacial IMC growth kinetics, causing thinner NiP layer, reducing overall IMC spallation, and producing thinner and continuous IMC layer, which results in improved solder joint performance.

Signal integrity on tester boards is a relevant property. The purpose of signal integrity analysis is to ensure that a signal is not degraded as it transfers from a driver component to a receiver. In this study, two ENEPIG HDBI MB boards were analyzed - for signal integrity - and compared with two ENIG HDBI MB boards. The analysis consisted of the following tests: 1. Double Data Rate (DDR) read/write margin; 2. High speed transceiver; 3. F-value regression; 4. Time Domain Reflectometry (TDR) impedance.

A summary of the signal integrity experiments include:

a) Read/Write margin data showed similar behavior between ENEPIG and ENIG boards with ENEPIG showing a better margin on almost all interfaces.
b) High speed transceiver revealed normal behavior based on eye diagrams captured on all lanes with the ENEPIG board. This applies to all lanes except two lanes which showed a narrowed eye.
c) To further evaluate the performance of the two lanes, a TDR analysis was completed for the two lanes. The TDR plots do not display major concerns. Figure 13 depicts these TDR plots. The different colored plots are impedances from the various data lanes.

From these data, it was concluded that although some differences were seen, the signal integrity test experts concluded that these differences can be remediated by reworking a trace path in ENEPIG board. Their conclusion was to switch to ENEPIG and remediate the signal integrity sighting by reworking a marginal trace path on the ENEPIG Board.

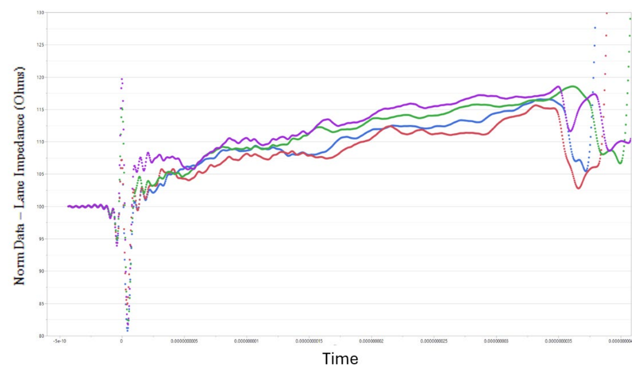

Figure 13. TDR plots for two lanes. There are no major differences in TDR plots for ENEPIG and ENIG boards on two suspected lanes – with differences in eyes diagrams.

Last, the cost adder to overall HDBI tester cost by converting all HDBI tester boards to ENEPIG surface finish was estimated as less than 1%. This total tester cost adder was considered negligible.

CONCLUSIONS

The best cost-reduction practice for Intel manufacturing is to deliver testers with high quality and reliability. Solutions with higher margins to failure will support this goal. In the case of solder joints in tester boards, it was demonstrated that ENEPIG delivers solder joints with significant higher margin to failure compared with ENIG POR plating solution under mechanical shock. Therefore, the team strongly recommends converting all tester boards to ENEPIG surface finish based on the results of this 1.5 years long study. The main learnings of this study include:

1. Solder joints formed with ENEPIG surface finish outperformed solder joints with ENIG surface finish under shock stress. Data indicates that ENIG solder joints are marginal. Therefore, ENIG solder joints should not be used on tester boards integrated to cold plates.
2. The investigation assessed the performance of solder joints with SMD and NSMD lands. Both land designs are used in tester boards designs. The solder joints on SMD lands with ENIG surface finish did not survive even one drop cycle during the mechanical shock test. In contrast, joints on lands with ENEPIG surface finish showed a superior performance under shock testing for both SMD and NSMD Lands. Therefore, for tester boards integrated to cold plates, boards with ENEPIG surface finish provide a solution with a large margin for failure.
3. The IMC layer on ENIG solder joints was formed badly which resulted in the insufficient mechanical strength of solder joints and caused crack or catastrophic solder joint failures at first drop. In contrast, IMC layer on ENEPIG solder joints was formed correctly which resulted on stronger mechanical strength of solder joints, outperforming ENIG solder joints.
4. The use of test vehicles to assess solder joint performance is a low cost and data rich approach to assess PCB pad plating quality delivered by PCB suppliers. The use of this approach should be encouraged as part of a PCB supplier qualification as well as enabling periodic monitors to assess PCB incoming quality.
5. Signal integrity analysis conducted on ENEPIG and ENIG HDBI MB production boards resulted in some differences. However, these gaps can be addressed by reworking trace paths. It is recommended that signal analysis is conducted for tester boards early on in development, when boards are being converted to ENEPIG. In this way, discovery of potential marginalities on circuit designs can be addressed earlier at a lower cost.
6. The cost adder for converting all HDBI tester boards from ENIG to ENEPIG surface finish is negligible.
7. This paper did not address the other key failure with ENIG surface finish: poor wetting (non-wetting or de-wetting) of the solder to the ENIG surface finish on PCB lands during soldering processes. This is a recurrent problem in tester manufacturing, impacting production cost. Hence, this is an important and relevant avenue for future work.
8. Published evidence in the literature [9-13], confirms the findings of this study that ENIG surface finish may cause catastrophic, brittle, interfacial solder joints.

ACKNOWLEDGEMENTS

The authors Acknowledge the support from CPTD management during this 1.5 yearlong study. Steve Folsom and Doin Davenport facilitated access to budget and assembly process. Authors also acknowledge the support of Intel stress labs. Parviz, Moradi - Ali - spent many hours running shock stress for TVs and HBDI MB boards. Larry Smith designed the boxes used to ship HDBI MB production boards. The reduction of induced stress to the boards required multiple iterations of box designs. Shelby Rollins; Jorge Fernandez; Preethi, Srinivas; Shilpa Srinivasan; Prithvee Sundararajan; Gabriel Melendez; and Naveen Kolavanahalli - designed, executed, and draw conclusions for the signal integrity experiments with HDBI MB production boards (ENEPIG and ENIG).

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