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Board Level Reliability of Large Body Size WlCSP for Automotive Radar Applications

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ABSTRACT

Wafer-level CSP (WLCSP), which is commonly defined as a package that is completely fabricated over the IC layers at the wafer-level, has been around since the mid-1990's [1]. WLCSP is commonly referred to as "fan-in" since all the package redistribution layers and BGAs are contained within the outline of the IC. Initial applications were mainly flash and DRAM devices with relatively low I/O density. The obvious advantage of WLCSPs is the decrease in form factor and weight versus more conventionally packaged parts. However, another advantage of WLCSP is better electrical performance due to shorter interconnects that also provide lower package, or in this case redistribution layer (RDL), parasitics and may therefore enable higher system speeds and frequencies [2]. For this reason, as well as packaging and test costs that can be lower than some other packaging technology alternatives, WLCSP was chosen for a next generation automotive mmWave transceiver radar application operating at 76-81 GHz [3]. Automotive radar transceivers, which integrate transmit and receive functions on the same silicon, are the primary sensor for automotive driver assistance systems (ADAS). These monolithic microwave integrated circuits (MMICs) are utilized in automotive applications for sensing and identifying the environment and objects around the vehicle. Data on these objects, whether in motion or stationary, such as distance and speed are collected for use in a variety of responses including collision avoidance in these increasingly intelligent vehicles.

Choosing a WLCSP for this demanding automotive application with stringent qualification requirements and a relatively large die presented its challenges [4]. Chief among these challenges is attaining the required reliability at the board-level. WLCSP typically has relatively thin passivation and redistribution layers over the silicon IC which may only minimally mitigate the CTE mismatch between silicon (CTE 2.6 ppm/°C) and the PCB (17 ppm/ºC depending on laminate materials). This paper will outline the board-level assembly development and reliability that was undertaken to demonstrate this WLCSP could meet the demands of automotive. With such a large die size, which is believed to be one of the largest WLCSPs ever qualified for automotive, underfill and edge bond were evaluated to enhance the reliability at the board level.

Key words: WLCSP, wafer-level chip scale package, mmWave, millimeterWave, automotive radar, advanced driver assistance systems, ADAS, Monolithic microwave integrated circuits, MMICs, transceiver

INTRODUCTION

Product Package Design

The radar transceiver was designed into a 0.3 mm thick, 7.9 × 9.3 mm, 214 I/O WLCSP with 0.5 mm BGA ball pitch. SAC405 spheres were used that had a diameter after attaching to the WLCSP of 0.31 mm. Many of the spheres were dedicated to power and ground and since the overall I/O density was low, the WLCSP was designed in only one metal RDL layer (See Figure 1). The WLCSP package bottomside view and a topside view is shown in Figures 2 and 3. As is evident from the bottom views of the device, the metal density was approximately 75%.

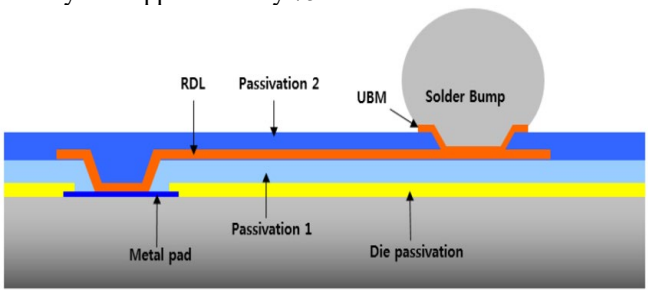

Figure 1. Cross-sectional view showing the one metal layer RDL and the two organic dielectric WLCSP passivation layers. Image is not to scale.

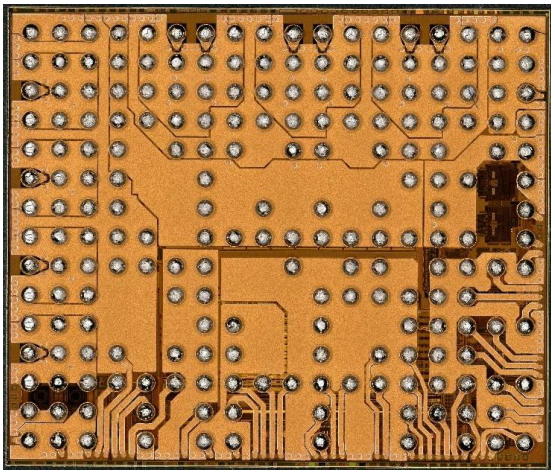

Figure 2. Bottomside of the 7.9 × 9.3 mm, 214 I/O WLCSP.

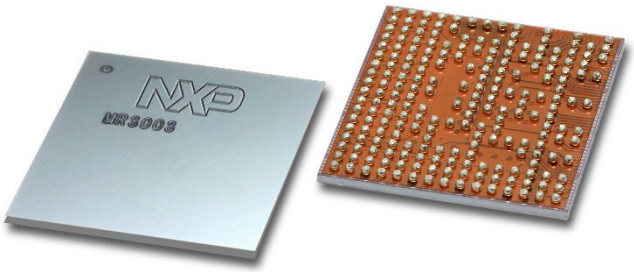

Figure 3. Backside and bottomside of the 7.9 × 9.3 mm, 214 I/O, 0.5 mm pitch automotive qualified single chip 76–81 GHz transceiver for ADAS radar applications.

RELIABILITY TESTING

Test Vehicle Design

A daisy-chain test vehicle version of the product was designed for SMT assembly and to facilitate board-level reliability testing. The goal was to replicate the WLCSP attributes, including metal density, layer thicknesses, etc. of the product as closely as possible. The design of the RDL layer of the actual product was used as a starting point and it was modified to result in connected pairs of BGA locations. Similarly, the die was modified such that the last metal was incorporated into daisy-chain. Both the WLCSP RDL and die last metal daisy-chain routing are shown in Figure 4. The product RDL routing in Figure 2 can be compared to the daisy-chain RDL routing in Figure 4. Some of the extensive power and ground planes were partitioned to allow those bumps to also be included in the daisy-chain. A representation of the resulting daisy-chain path while mounted to the PCB is shown in Figure 5.

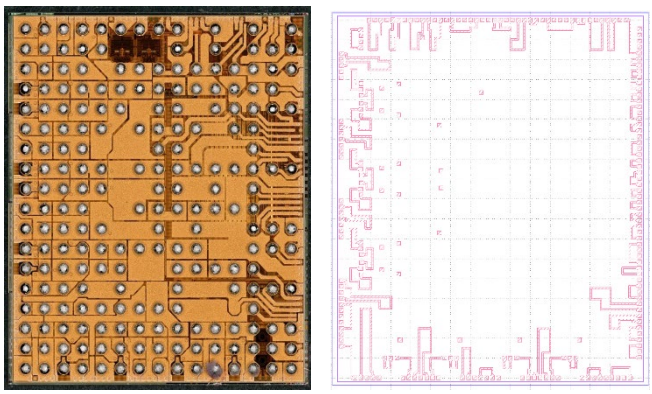

Figure 4. WLCSP RDL (left) and die last metal (right) designs used to form a daisy-chain test vehicle.

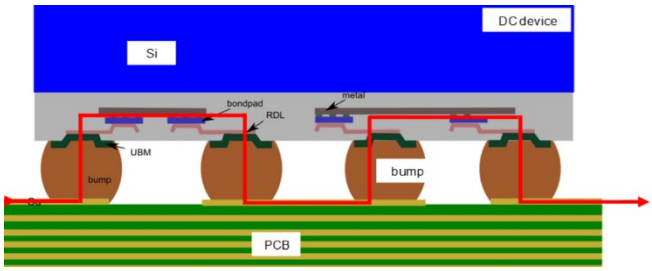

Figure 5. Representation of the daisy-chain routing used for reliability testing of this WLCSP. PCB layers shown do not represent actual.

Test PCB Design

A 1.3 mm thick thermal cycling test board was designed to represent a typical customer ADAS application. It is shown in Figure 6 below. The PCB had a total of five metal layers. The core and adjacent dielectric layers were typical high Tg FR-4 epoxy glass laminate material. The top layer dielectric where the WLCSPs were mounted was a low loss PTFE based material that was 0.130 mm thick. See actual cross-section of the PCB in Figure 7. Due to this asymmetry, components were only mounted to the top side of the PCB.

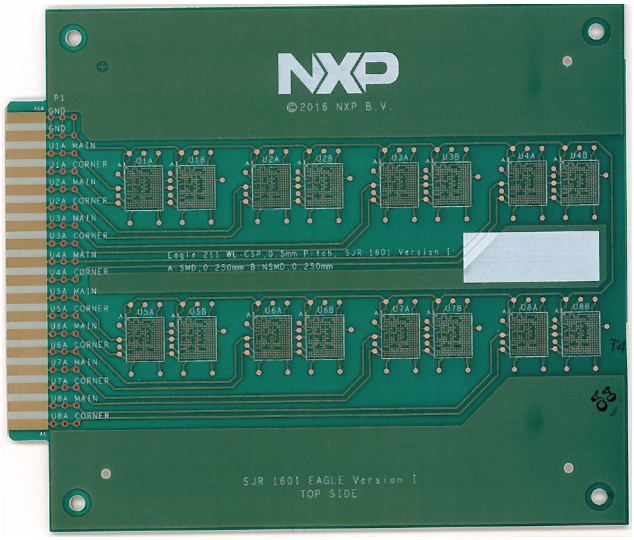

Figure 6. Board-level thermal cycling PCB containing 16 topside WLCSP footprints eight of which were NSMD and eight SMD.

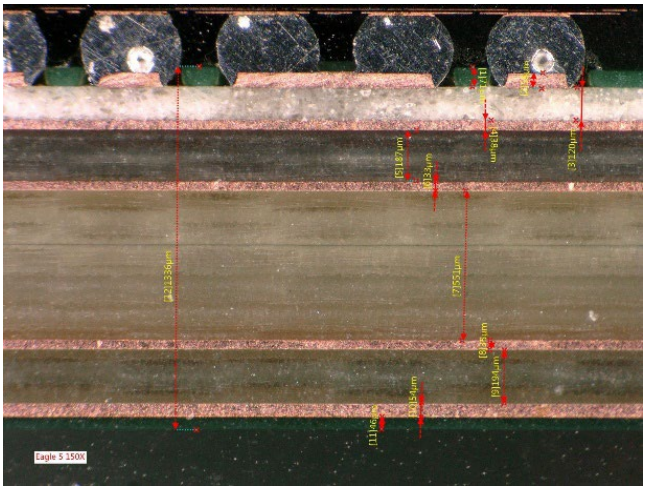

Figure 7. Cross-section of the thermal cycling board-level reliability PCB showing three layers of conventional dielectric with a low loss PTFE-based top layer.

The PCB topside contained a total of 16 footprints, eight SMD with a 0.25 mm soldermask opening and eight NSMD with a 0.25 mm copper diameter. The NSMD pads had a 0.10 mm soldermask clearance around the copper pad. These two footprints are shown in Figure 8. There has been much industry discussion over the years about the trade-offs between SMD and NSMD pads with the overwhelming

majority of users preferring and adopting NSMD. SMD was included since some customers may prefer it for electrical performance reasons in terms of being able to have almost continuous PCB top layer planes in critical regions under the device to optimize mmWave performance. OSP finish was used as the solderable surface. Hard NiAu electroplating was used on edge fingers that were used to provide a means of continuously contacting through a connector in the thermal cycling chamber so that in-situ resistance monitoring could be carried out.

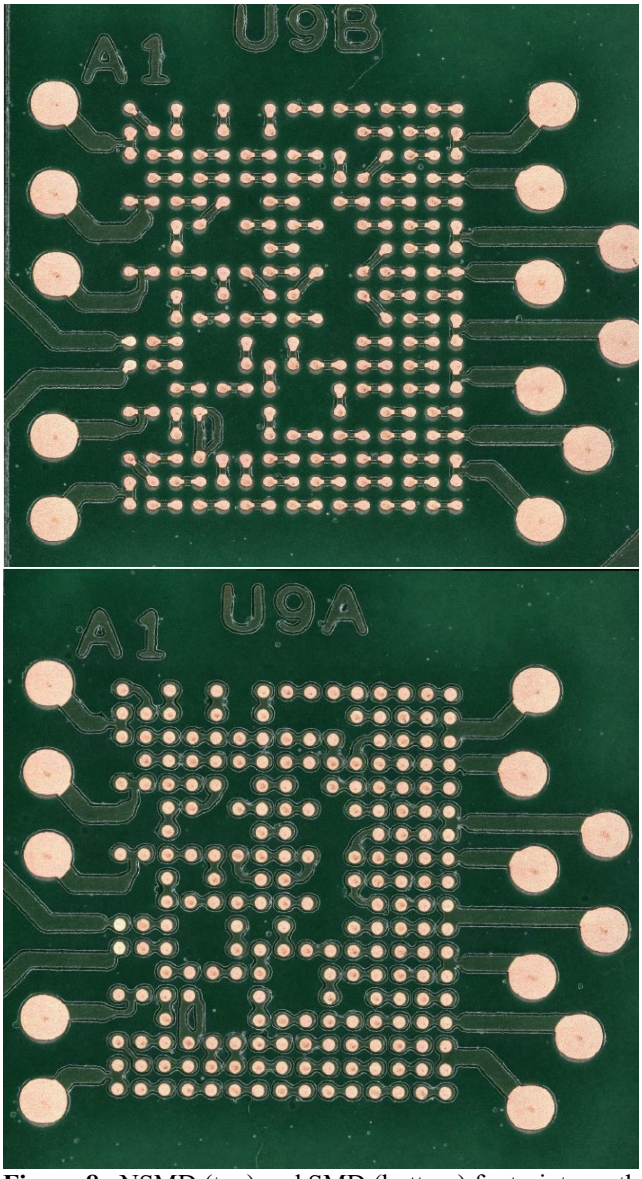

Figure 8. NSMD (top) and SMD (bottom) footprints on the same thermal cycling test board. Both footprints used a 0.25 mm solderable pad diameter and OSP finish. Note the test points around each footprint that are used for failure isolation.

Test Board Assembly

WLCSPs were assembled using SAC305 ROL0 no clean solder paste with Type IV solder powder. The stencil used was 100 microns thick, electroformed, nanocoated with 270 × 270 micron squircles, which are squares with rounded corner apertures. See Figure 9. Squircles are purported to result in less incidence of solder paste buildup in the aperture corners leading to more consistent solder volume [5]. Typical solder paste prints for NSMD and SMD pads are shown in Figure 10. 100% optical solder paste inspection and overall PCB weight before and after solder paste print was performed before component placement. No type of post assembly cleaning of flux residues was performed.

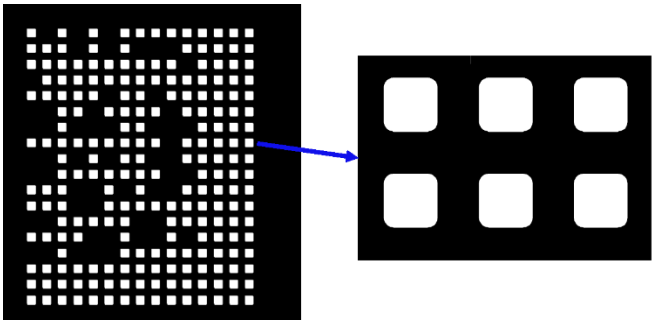

Figure 9. CAD image of the stencil showing the squircle pattern that was used.

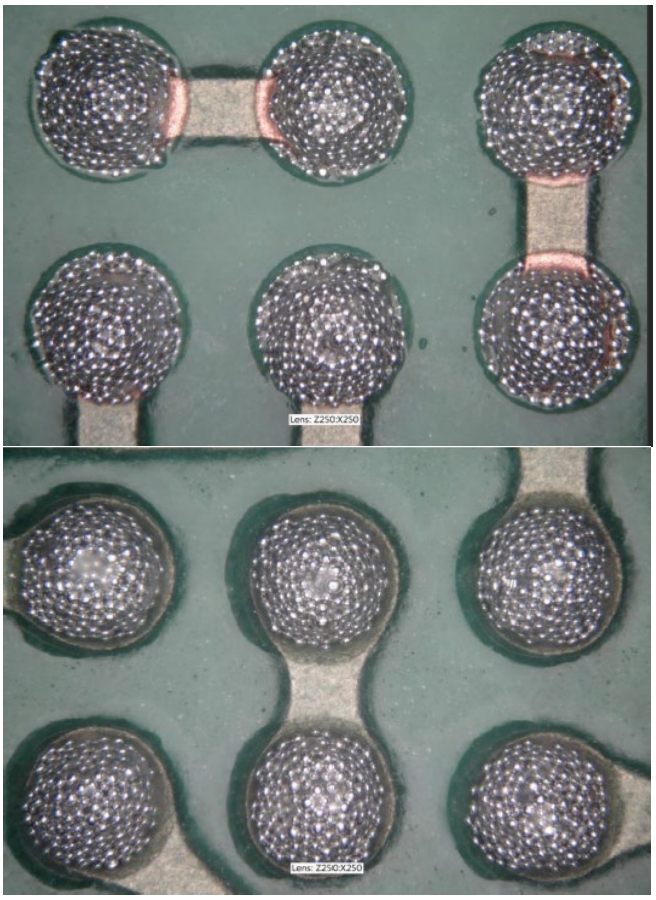

Figure 10. Typical solder paste prints for NSMD (top) and SMD (bottom) pads.

100% SMT assembly yield was achieved with no opens or shorts as determined by electrical test and 2D real time X-ray, respectively. The X-ray was also used to assess solder joint voiding using the application present within the X-ray tool software. The application was able to automatically

determine the % voiding within each solder ball. Example images of voiding are given in Figures 11 and 12. NSMD joints were found to have more voiding as a percentage of joint area with an overall range of 2-12% versus only 0-3.4% for SMD PCB pads.

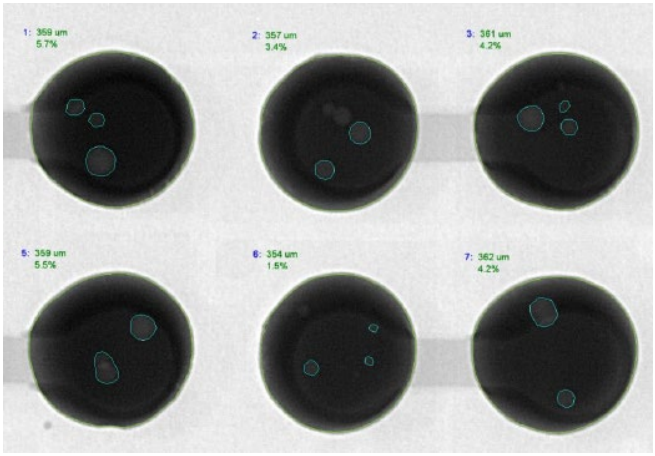

Figure 11. Typical x-ray of joints on NSMD pads with solder joints voids detected. Overall voiding was determined to be 2-12% of joint area.

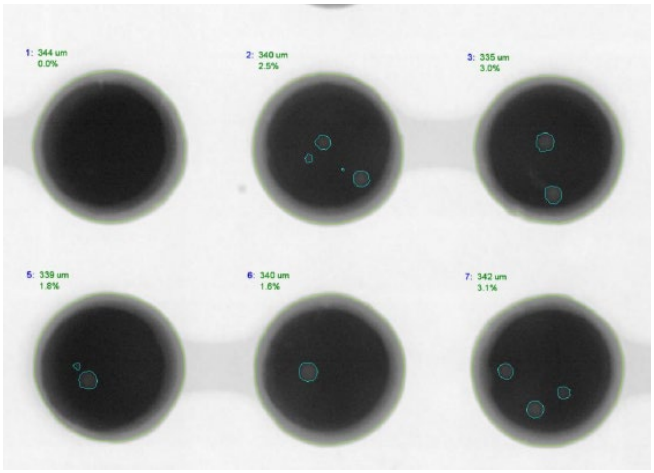

Figure 12. Typical x-ray of joints on NSMD pads with solder joints voids detected. Overall voiding was determined to be 0-3.4% of joint area.

Applying Underfill and Edge Bond

Since it was felt that achieving acceptable cycles to failure for some automotive applications and mission profiles in board level thermal cycling with such as large WLCSP may be challenging, a portion of the board-level reliability sample was underfilled and edge bonded. The materials used and their properties are listed in Table 1. The underfill was dispensed around three sides of the perimeter of the WLCSP and then wicked under device with capillary action. A seal pass was then carried out on the fourth side to achieve consistent filleting on all four sides of the WLCSP. A top view of the underfill filleting is shown in Figure 13 and a cross-section also showing the fillet and also showing the underfill enveloping the edge WLCSP sphere is shown in Figure 14. By contrast to the underfill, the edge bond material was much more viscous and only flowed minimally from the location it is dispensed. As recommended by the edge bond supplier, it was dispensed in an "L" shaped pattern in each corner of the WLCSP. Figure 15 is a 3D optical image following edge bonding and curing showing the representative amount of material that was dispensed. Both materials were snap cured as indicated in Table 1.

Table 1. Underfill and edge bond material properties.

UF or EB	CTE (ppm/ºC)	Modulus (GPa)	Tg (ºC)	Cure Profile Used
UF	28	10.5	161	7 mins@160ºC
EB	15	13.3	149	1.5 mins@150ºC

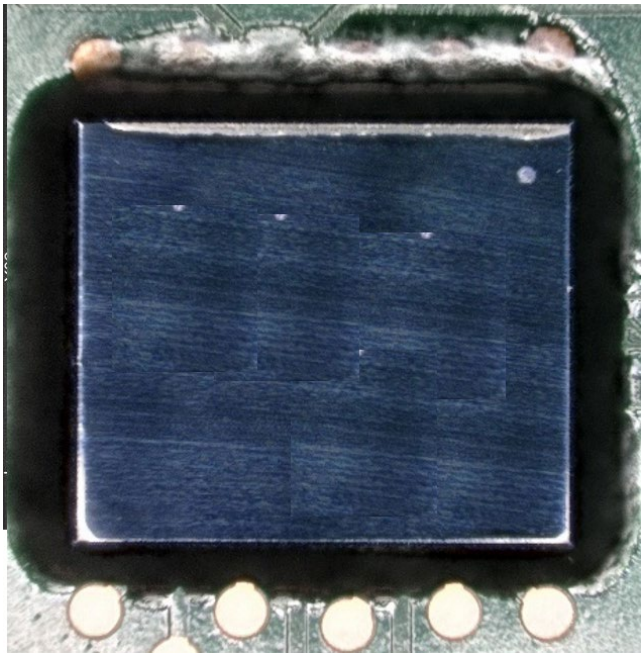

Figure 13. Top view optical image of WLCSP following underfill dispense and cure.

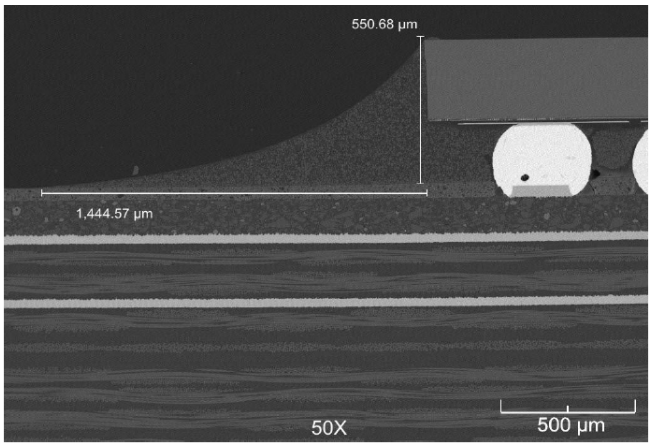

Figure 14. Cross-section of an underfilled WLCSP on NSMD PCB pad showing a typical fillet profile and overall mounted height.

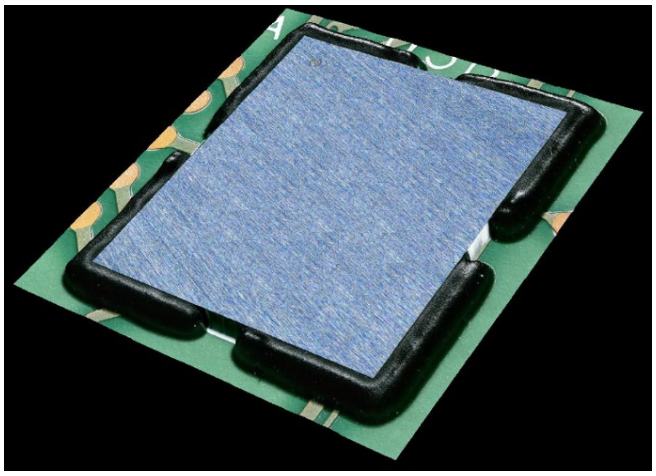

Figure 15. 3D optical image of WLCSP following edge bonding and cure.

Board-Level Thermal Cycling

Boards were placed in single chamber cycling from -40 to 125ºC with 15-minute effectively linear ramps and 15-minute dwells. Care was taken when profiling the chamber to ensure the PCBs saw the actual prescribed temperatures. A typical -40 to 125ºC temperature cycling profile is shown in Figure 16. All six cells were cycled until at least 63.2% failure which is the Weibull distribution characteristic life or eta. Then two parameter Weibull plots of the results were generated and failure analysis was performed. A summary of the results is presented in Table 2 and plotted in Figures 17 through 19. On these plots the y-axis is the CDF expressed in percent.

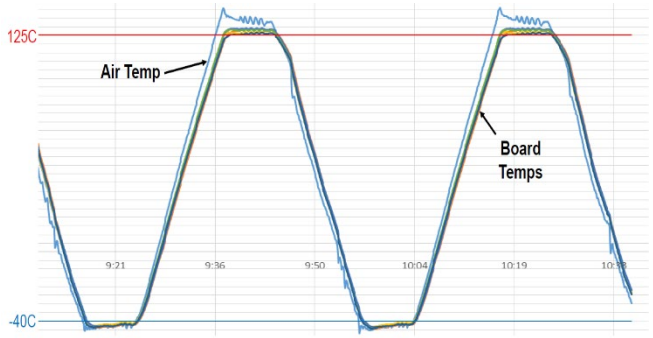

Figure 16. Typical -40 to 125ºC temperature cycling profile.

Table 2. Board-level thermal cycling results.

Cell	UF or EB	PCB Pad	Beta	Cycles to 1% Fail	Character-istic Life
1	None	SMD	3.7	95	332.8
2		NSMD	3.0	145	663.3
UF1	UF	SMD	6.1	1,800	3,509
UF2		NSMD	5.4	2,000	4,616
EB1	EB	SMD	8.2	590	1,031
EB2		NSMD	8.0	1,050	1,889

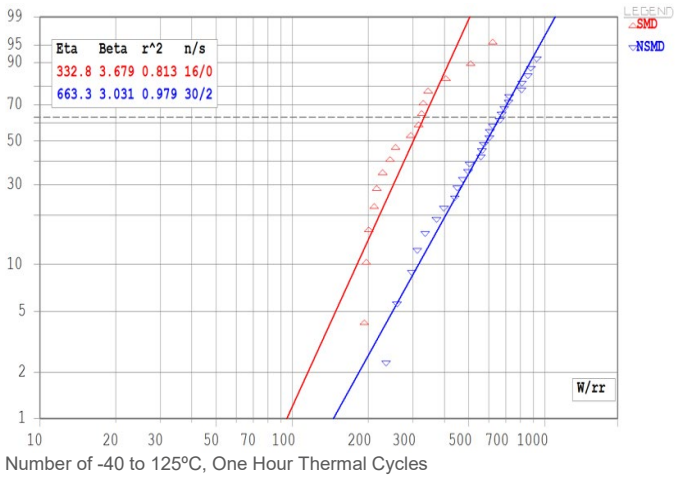

Figure 17. Two parameter Weibull plot showing the board-level -40 to 125ºC cycles to failure of WLCSPs with no underfill or edge bond and with both SMD (Cell 1) and NSMD (Cell 2) PCB pads.

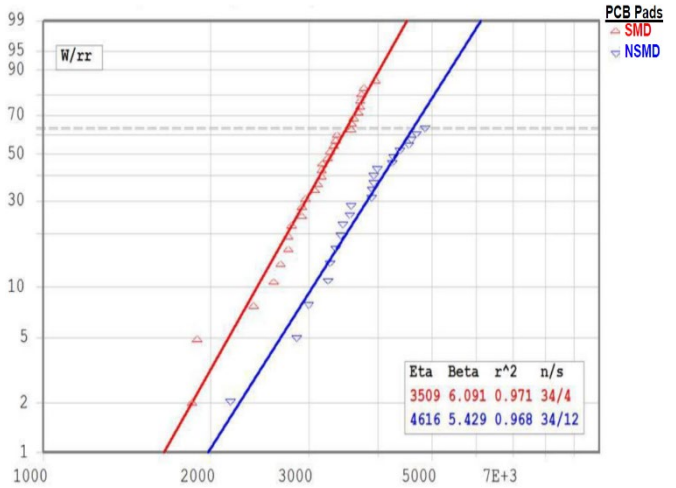

Figure 18. Two parameter Weibull plot showing the board-level -40 to 125ºC cycles to failure of underfilled WLCSPs with both SMD (UF1) and NSMD (UF2) PCB pads.

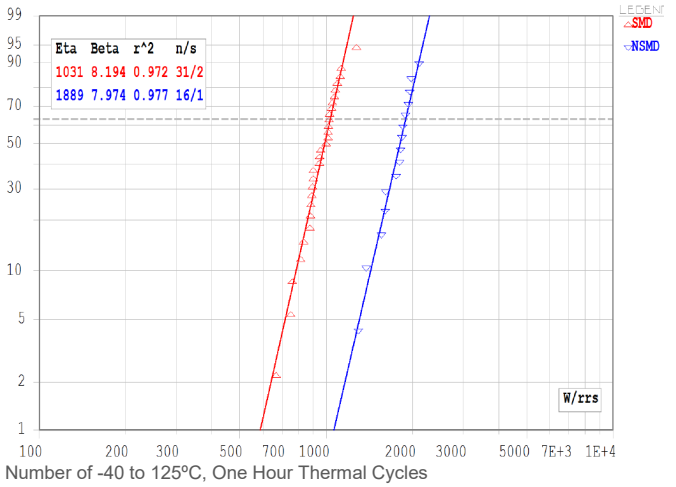

Figure 19. Two parameter Weibull plot showing the board-level -40 to 125ºC cycles to failure of WLCSPs with edge bond and both SMD (EB1) and NSMD (EB2) PCB pads.

Failure analysis was performed on every cell. Generally, the predominant failure mode was the same with bulk solder fracturing occurring through the SAC405 solder bump close to the WLCSP. For the NSMD pad cells, more fracturing was observed down at the PCB interface. Figure 20 shows a typical cross-section after failure, in this case of an edge bonded cell with NSMD PCB pads.

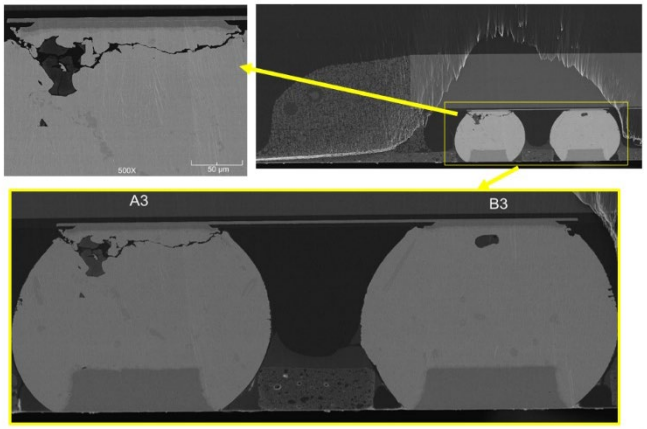

Figure 20. Cross-section of 1st failure at 1,293 cycles from cell EB2 (edge bond, NSMD PCB pad) showing corner ball fracture. Note the profile of the edge bond material.

Board-Level Drop Testing

Even though the target application for this WLCSP was not handheld electronics there was a desire to assess the drop performance. Additionally, due to the nature of automotive electronics, there is understandably no suitable industry drop test standard since products may not be designed to withstand drop events that may unpredictably occur during shipping and manufacturing. A 1.0 mm thick, 132 × 77 mm drop test PCB was designed based on the JEDEC JESD22-B111 standard for handheld electronics [6]. It should be noted that an update to this JEDEC standard released in 2016 calls for the use of a smaller 77 × 77 mm PCB. The JEDEC standard used for the current testing, released in 2003, calls for the use of an eight-layer PCB fabricated from specific resin coated copper or FR-4 materials. While maintaining the overall 1.0 mm thickness, it was decided to use a stack-up more typical of that used for mmWave automotive applications for this testing. To this end, similar to the thermal cycling PCB a 0.130 mm PTFE-based dielectric material was used for the outer layers. Additionally, even though the JEDEC standard allows for up to 15 footprints on each side of the PCB, it was chosen to only use five of those locations in order to achieve more consistency in terms of the amount and nature of PCB deflection seen by each location. The PCB is pictured in Figure 21.

The PCBs were SMT assembled similarly to the thermal cycling test boards and 100% yield was again achieved. No underfill or edge bond was applied for this initial evaluation. A total of 20 units on SMD PCB pads and 20 units on NSMD PCB pads were dropped in groups of five units from a height needed to achieve 1500 g's with a half-sine pulse width of 0.5 milliseconds. The resulting accelerometer measured pulse achieved is shown in Figure 22. The result of the testing was that all samples from both PCB pad types passed with no failures detected after 30 drops.

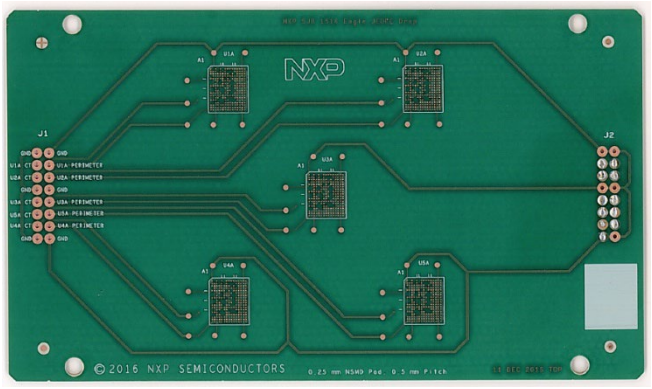

Figure 21. JEDEC drop test board.

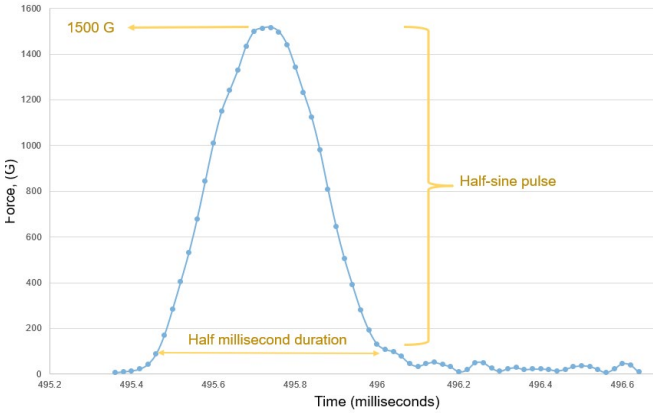

Figure 22. WLCSP drop test accelerometer pulse which meets JEDEC JESD22-B111 Condition B.

CONCLUSIONS

A large die 76-81 GHz transceiver WLCSP was successfully designed and tested for automotive ADAS applications. Board level reliability testing showed that the WLCSP could be qualified for automotive. Specifically, it was shown that board level underfill and perimeter edge bonding could be used when needed to achieve greatly improved board-level reliability results to meet the most challenging applications. The specific underfill evaluated was shown to increase board level reliability characteristic lifetime by as much as 10× while the edge bond was shown to increase lifetime as much as 3×. When SMD pads were used on the PCB it reduced the reliability by as much as 2× across all cells. This is due to the higher stress associated with SMD pads that drove bulk solder joint fracturing at that interface. Even though drop testing is not necessarily typical for automotive products, the WLCSP with no underfill or edge bond present passed 1500 g drop testing.

ACKNOWLEDGEMENTS

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