Assembly and Reliability of a Novel High Density Dual Row MaxQFP

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ABSTRACT

Plastic Leaded Chip Carrier (PLCC's) packages with J leads were developed during the time of widespread adoption of surface mount technology (SMT) in the 1980's [1]. By the 1990's, Quad Flat Pack (QFP) packages with gull wing leads had become the mainstream SMT packaging technology for products with pin counts ranging from 40 to 200 plus leads [2]. Many improvements have been made to QFP's over the decades including increased thermal performance with bottomside exposed pads and other enhancements, automotive reliability with MSL3 performance, stacked die, lead pitch decreases down to 0.4 mm and even 0.3 mm and pin counts as high as 304. This paper will discuss a novel QFP package called the MaxQFP [3-8] which combines the J leads of a PLCC with the gull wing leads of the traditional QFP within the same package to result in a cost-effective solution with roughly twice the IO density of a standard QFP at a given body size. The MaxQFP package also provides the cost benefits of a leadframe based package on products that would normally be packaged in a plastic BGA. Typically, a singular MaxQFP leadframe design can be used to accommodate multiple SoC designs. The package construction and some of the unique component assembly challenges will be discussed, but the paper will focus primarily on all aspects of SMT assembly of the MaxQFP. Additionally, the robustness of the assembly in automotive type board-level thermal cycling will be demonstrated.

Key words: MaxQFP, SMT, J lead, gullwing lead, QFP, PLCC, hybrid, leadframe.

INTRODUCTION

MaxQFP is a new high density quad flat pack (QFP) based package that combines both gullwing (GW) and J-leads in an overmolded package body. An example of a 16×16 mm body, 172 lead MaxQFP is shown in Figure 1.

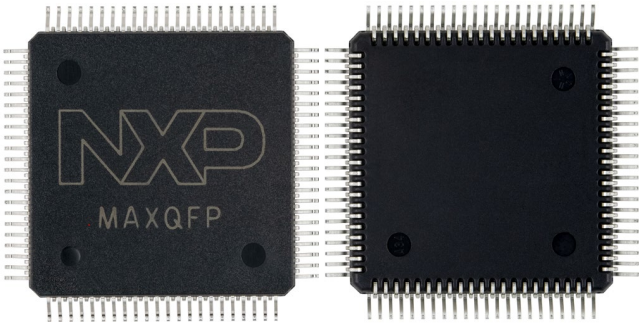

Figure 1. 0.65 mm lead pitch, 16×16 mm body, 172 MaxQFP package topside (left) and bottomside (right).

The leads on the outer row are traditional QFP gullwing leads, with the J-leads located inward towards the center of the package and interstitially between the GW leads. The external lead pitch between adjacent leads of the same type (J-leads or GW) is 0.65 mm and therefore the pitch between adjacent J-lead and GW leads is 0.325 mm. This is illustrated in Figure 2. Additionally, Figure 3 is a side view in the corner of the package. Note the offset of the leads in this image.

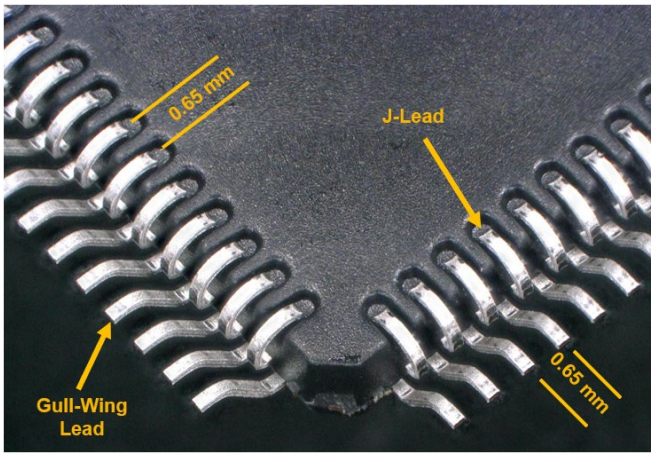

Figure 2. Higher magnification of the MaxQFP bottomside showing the interstitially placed J and GW leads.

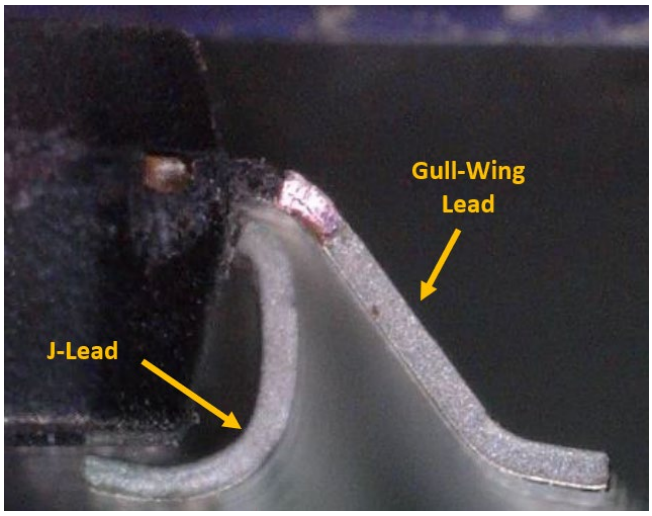

Figure 3. MaxQFP package corner showing GW and J-leads.

As an example, on the 16x16 mm body, 172 lead MaxQFP each side of the package has 22 GW leads and 21 J-leads resulting in a total of 43 leads per side and 172 leads total for the package. One notable feature of MaxQFP is that these two rows of leads are not located on the same plane during molding and there is no dam bar on the lead frame strip. This design allows the leads to be vertically displaced from each other even at the position of the molded body. The resulting separation reduces the chances of shorting between leads and effectively enables almost the entire perimeter of the package to be used for IO. Two MaxQFP body sizes have been tooled and developed to date, a 16x16 mm, 172 lead and a 10x10 mm, 100 lead. Together, these are able to potentially replace up to five JEDEC compliant QFPs with lead counts of 64, 80, 100, 144 and 176 as illustrated in Figure 4.

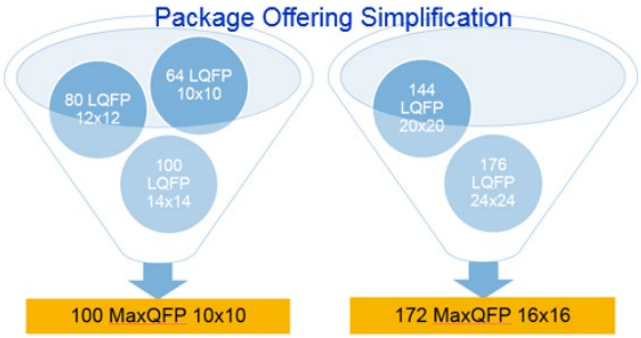

Figure 4. MaxQFP simplifies package portfolios as 100 MaxQFP can replace 64, 80 and 100 LQFP, while 172 MaxQFP can replace both 144 and 176 LQFP.

For higher power applications, MaxQFP with exposed pad (EP) has also been developed as shown in Figure 5. In this configuration, the die attach flag is exposed on the bottom of the package enabling it to be soldered to the customer printed circuit board (PCB) resulting in a robust, efficient thermal connection between the PCB, package and die. This thermal performance is significantly better than can be achieved by a similar leaded package without an exposed pad. The additional of the exposed pad can decrease the JEDEC thermal metric of $\boldsymbol{\theta}_{JA}$ of the MaxQFP by approximately 25% [9]. Additionally, whether an exposed pad is present or not, the MaxQFP's greater metal density affords it superior thermal performance relative to conventional QFPs.

Figure 6 compares the IO density of full array BGA at 0.65 and 0.8 mm pitch with conventional QFP and MaxQFP at 0.5 and 0.65 mm pitch. The QFP and MaxQFP body sizes on the x-axis include the GW lead extension from the package body which is 1.5 mm per side. All the body sizes and IO counts shown are taken from current or proposed JEDEC registrations for those packages. At most body sizes, the 0.65 mm pitch MaxQFP offers over 50% more IO density versus conventional, 0.5 mm pitch QFP.

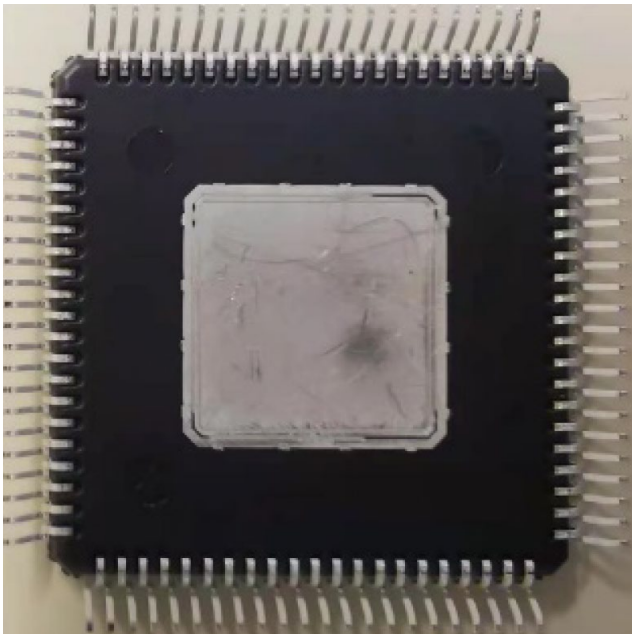

Figure 5. Bottomside of the exposed pad version of the MaxQFP slated for more demanding thermal applications.

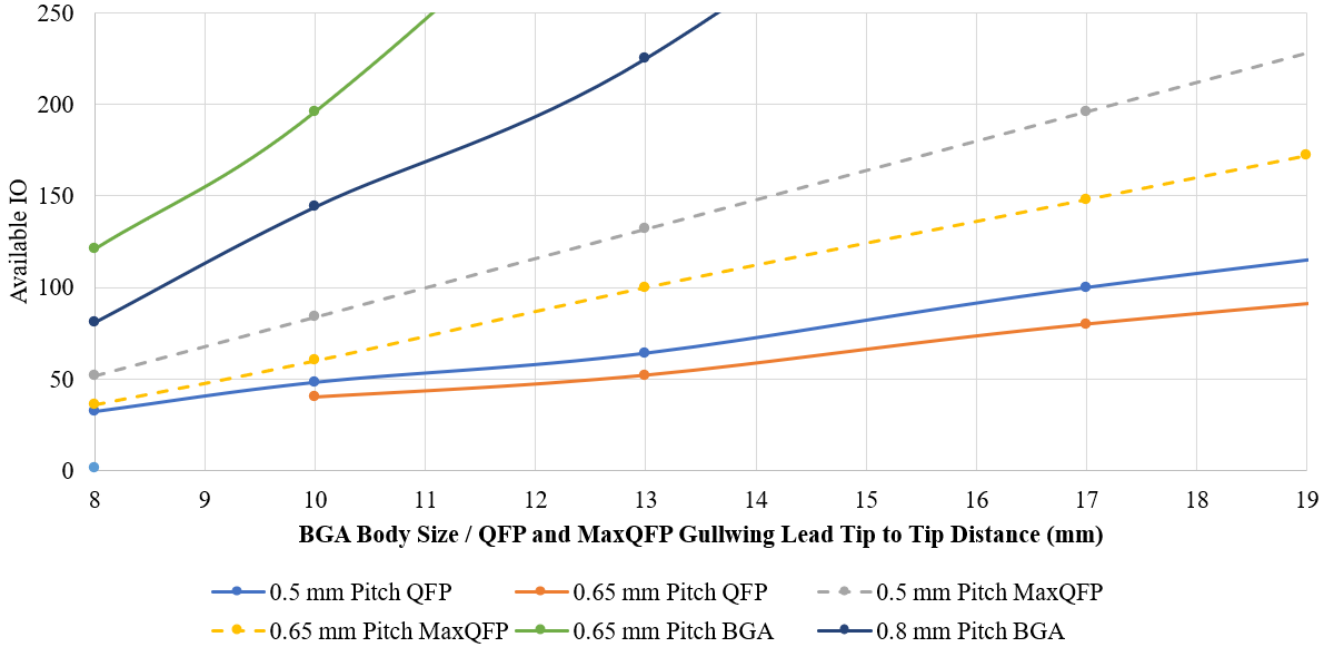

Figure 6. IO density comparison between 0.5, 0.65 to 0.8 mm pitch full array BGA and 0.5 and 0.65 mm pitch conventional QFP and MaxQFP. Note that QFP and MaxQFP body size includes the gullwing leads coming out from the package body.

ASSEMBLY AND RELIABILITY ASSESSMENTS

Component Level Reliability

Since one of the primary applications targeted for the MaxQFP is automotive, demonstration of component level reliability stressing to Automotive Electronic Council Q100 Grade 1 was a requirement [10]. Additionally, since MaxQFP devices are targeted for copper (Cu) wirebond interconnect, additional requirements imposed by AEC Q006 were also applicable [11]. Prior to eventual product qualification, two different test vehicles (TV) were assembled and subjected to component level stressing. The two TV die, one that was four metal level (4ML) CMOS90 and one seven metal level (7ML) CMOS40 were both assembled into a 172 MaxQFP using 20 µm diameter PdCu wire. As can be seen in Table 1, all stresses passed including the required post-MSL and post-temperature cycling (TC) C-SAM to ensure no delamination. Typical C-SAM results on the same unit time zero, post-MSL and post-TC are shown in Figure 7. An example of an AEC required post-TC Cu ball bond cross-section is also shown in Figure. 8.

Table 1. 172 MaxQFP AEC Grade 1 stress results with CMOS90 4ML and CMOS40 7ML TV die. Underlined readpoints are required. ML = die metal layers.

TV	Reliability Stress	Sample	Readpoints Passed
C90 4ML	-55 to 150ºC TC	4 × 90	1000/2000/3000 cyc
	110ºC/85%RH uHAST	4 × 90	264/528 hrs
	85ºC/85%RH THB	4 × 90	1008/2016 hrs
	150ºC HTSL	4 × 90	1008/2016 hrs
C40 7ML	-55 to 150ºC TC	3 × 109	1000/2000 cyc
	110ºC/85%RH uHAST	3 × 80	264/528 hrs
	150ºC HTSL	3 × 85	1008/2016 hrs

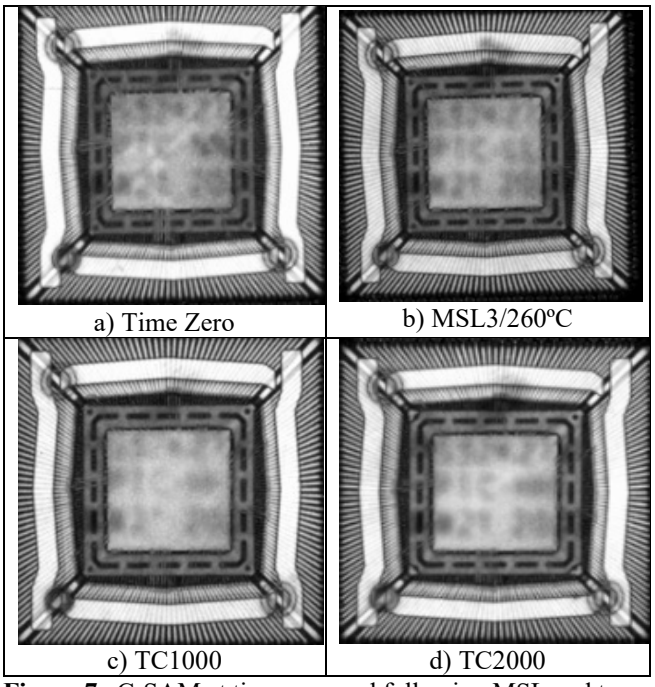

Figure 7. C-SAM at time zero and following MSL and temp cycle stressing of the 172 MaxQFP with CMOS40 4ML TV showing no delamination.

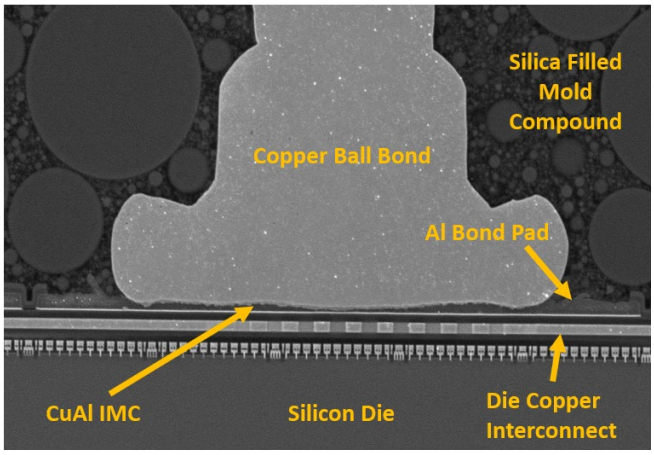

Figure 8. Cu ball bond on 172 MaxQFP following TC2000.

PCB Board Assembly

A six layer, 1.57 mm thick test board with OSP pad finish was designed and fabricated to carry out SMT assembly and board-level reliability evaluations. The daisy-chain test board was designed such that the J and GW leads were independent nets to allow checking for both solder joint shorts and opens. 172 MaxQFPs with Sn plated leads were assembled with lead finger to lead finger daisy-chains connections formed by wire-bonding. The test board was designed with four different PCB pad geometries (A through D) on the same PCB. It was decided to only utilize three of these (A, B and D) for SMT assembly and stressing. PCB footprint type D, where PCB pads for both J and GW leads were 1.40 × 0.28 mm, was considered as the recommended plan of record. Table 2 lists key attributes of the PCB, stencil, solder paste and reflow. The PCB is shown in Figure 9.

Table 2. PCB, stencil, solder paste and reflow attributes.

Item	Attribute	Value
PCB Dimns	L × W (mm)	114.3 × 251.4
	Thickness (mm)	1.57
Material	Tg (ºC)	180
	x/y CTE < Tg	13/14 ppm/ºC
	Cu Layers	6
PCB Pad	Type	NSMD with 0.050 mm soldermask clearance
	Pad Dimns (mm × mm)	A: GW: 1.45 × 0.28 J-Lead: 1.0 × 0.28 B: GW: 1.45 × 0.30 J-Lead: 1.0 × 0.30 D: Both: 1.40 × 0.28
	Surface Finish	OSP
Stencil	Thickness (mm)	0.125
	Aperture Dimns	1:1 with Cu Pads
	Material	Fine Grain Stainless Steel with Nano Coating
Solder Paste	Alloy (Wt %)	SAC305
	Type	No clean, ROL0, Type IV
Reflow	Atmosphere	Air
	Peak Temp (ºC)	240

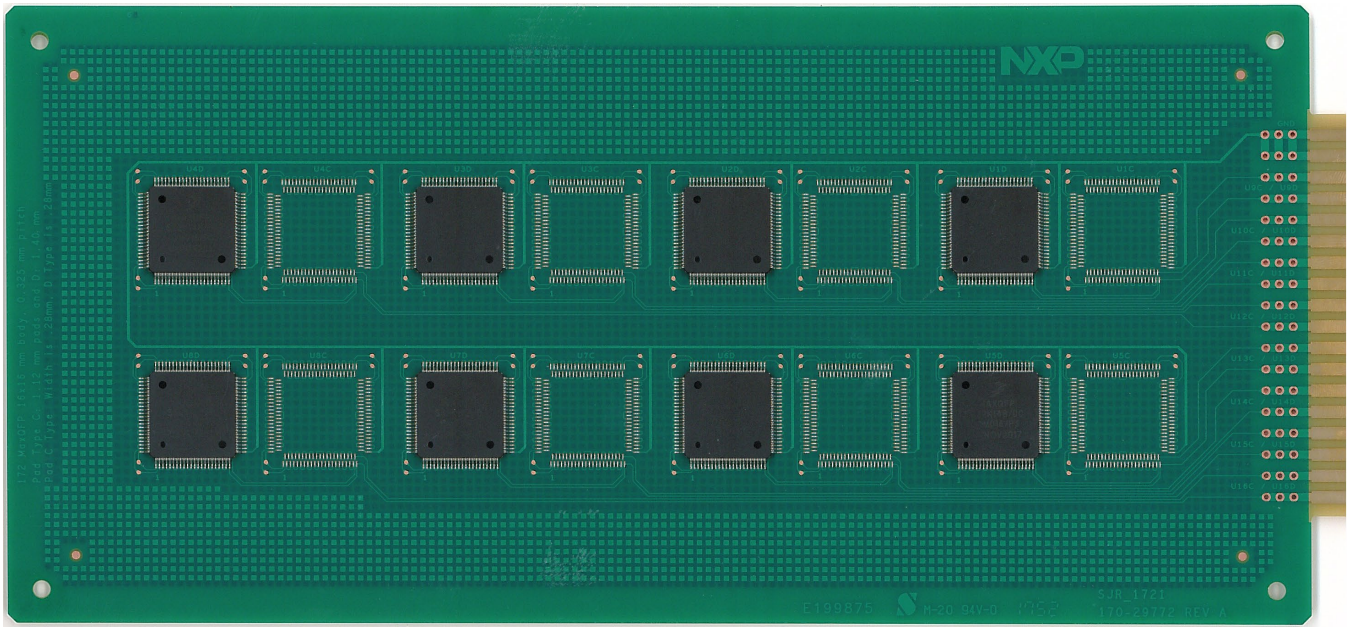

Figure 9. Fully assembled 172 MaxQFP test board with all eight type D footprint sites populated. Note edge fingers for in-situ resistance monitoring during thermal cycling.

Figure 10 shows two images of the preferred PCB pad type D prior to solder printing. An example of the solder paste printing achieved with the 0.125 mm thick stencil is shown in Figure 11. Approximately 100 units were SMT assembled across all three PCB pad geometries. SMT assembly resulted in 100% soldering yield. No shorts or opens were observed visually or detected by probing each unit on all three pad geometries. Figure 12 shows various images of solder joint formation after assembly. 100% X-ray was also carried out

which confirmed no solder shorts as shown in Figure 13. Time zero cross-sectioning was also performed (Figure 14).

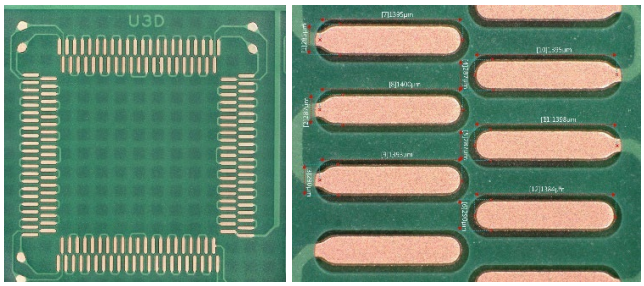

Figure 10. PCB type D footprint overall (left) and higher magnification image (right) showing actual measured pad dimensions of these 1.40 × 0.28 mm pads.

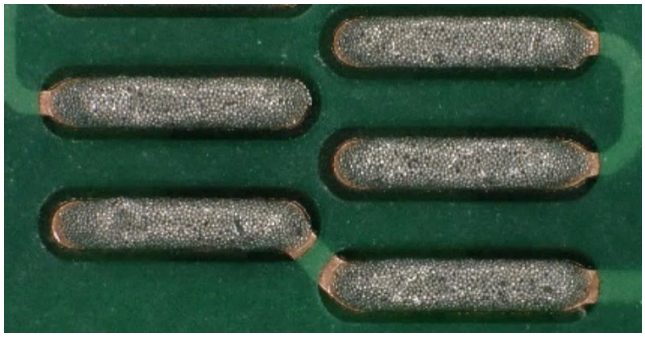

Figure 11. PCB type D footprint typical solder paste print.

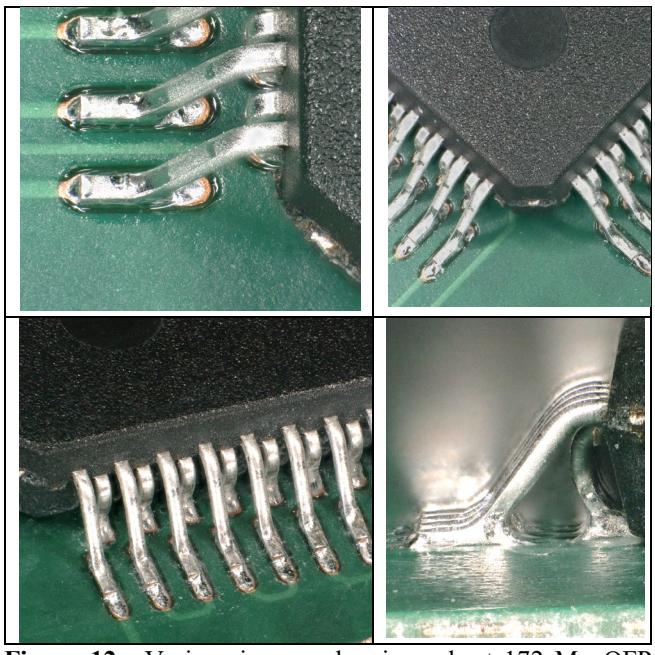

Figure 12. Various images showing robust 172 MaxQFP solder joint formation following SMT assembly.

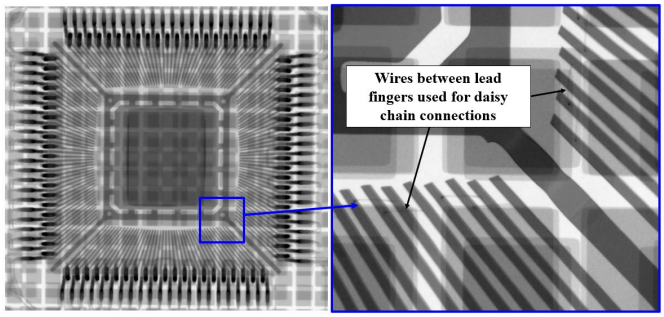

Figure 13. Typical X-ray of the overall 172 MaxQFP (left) and package level jumper wires (right) following SMT assembly.

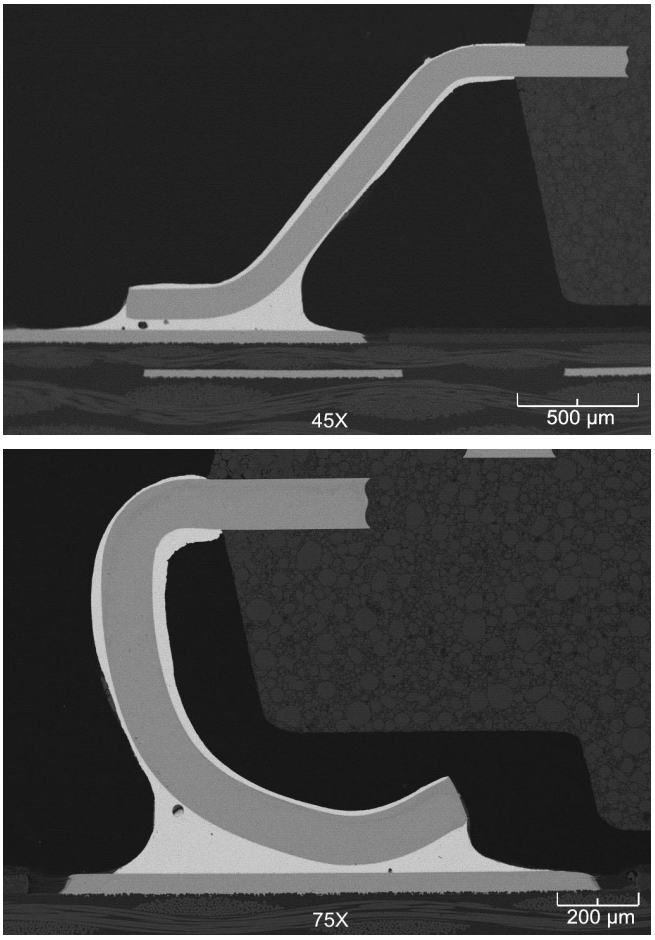

Figure 14. SEM images of cross-sections of the gullwing (top) and J-lead (bottom) solder joints of the 172 MaxQFP following SMT assembly onto pad type D.

As a follow on SMT study, the original PCB in Figure 9 was redesigned as a two layer PCB with 16 type D footprints per PCB. A total of 124 PCBs were assembled by a contract manufacturer and again no 172 MaxQFP solder joints opens or shorts were observed. The 1,984 parts assembled represented 341,248 total solder joints. Applying a 90% confidence limit, this indicates a worst-case 6.75 ppm SMT assembly yield loss for this technology. It is believed that with a robust and well characterized SMT assembly processes including the use of 3D solder paste inspection

(SPI), MaxQFP assembly yields approaching zero defects are likely achievable.

Board Level Reliability

The assembled thermal cycling PCBs were placed into single chamber, 15 minute ramps and dwells, one-hour total, -40 to 125°C thermal cycling. A typical requirement for a product in this cycling condition would be to achieve 1,000 to 2,000 failure free cycles depending on the AEC grade and specific customer requirements. The daisy-chains PCBs were continuously monitored using high speed event detectors. The event detectors were set to record failures at 1000Ω resistance or greater per IPC-9701 [12]. The event detectors detected events with a minimum detectable event duration of 200 nanoseconds. Thermal cycling continued beyond approximately 12,000 cycles until all three footprint types had enough failures to analyze with Weibull statistics. All three PCB pad types lasted well over 6,000 cycles, which exceeds any known reliability requirements. PCB pad type D, where the GW and J-lead pads are equal length, performed the best with no failures detected until 9,791 cycles. A summary of the failures at the conclusion of testing is shown in Table 3. The thermal cycling results are also plotted by pad type on two parameter Weibull axes in Figure 15. Additionally, cross-sectioning was carried out post-cycling to observe the failure modes (Figure 16).

Table 3. Summary of board level thermal cycling results.

Pad Type	Pad Dimns (mm × mm)		Cycles to 1st Fail	Charac-teristic Life (Eta)
	Gullwing	J-Lead		
A	1.45×0.28	1.0×0.28	6,837	10,546
B	1.45×0.30	1.0×0.30	6,545	12,044
D	1.45×0.28		9,791	13,049

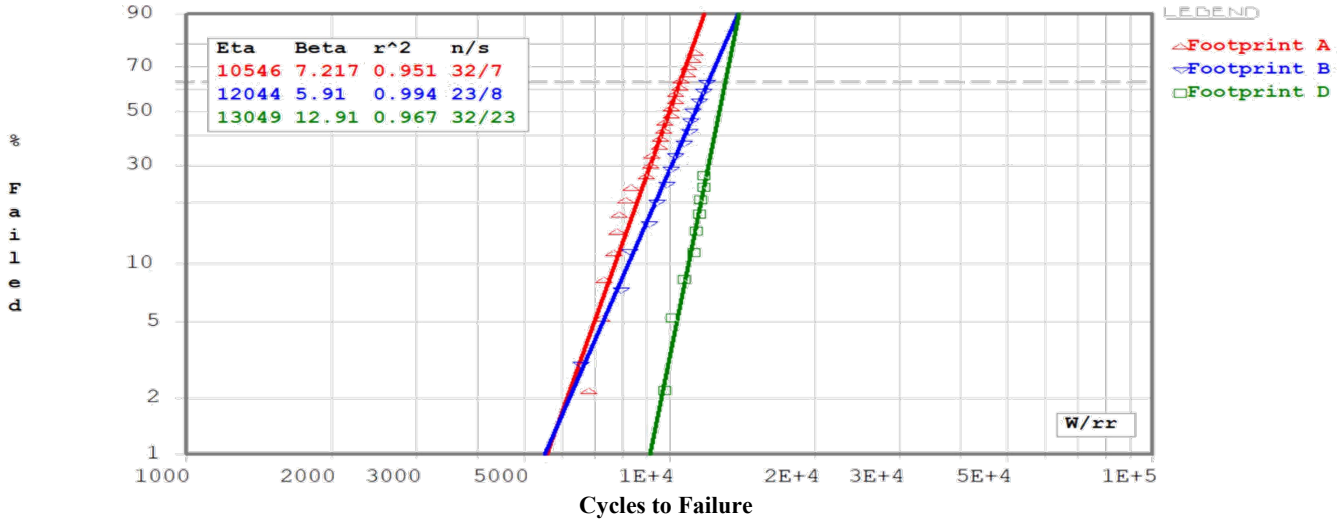

Figure 15. Two parameter Weibull plot of board level thermal cycling results for all three PCB pad types.

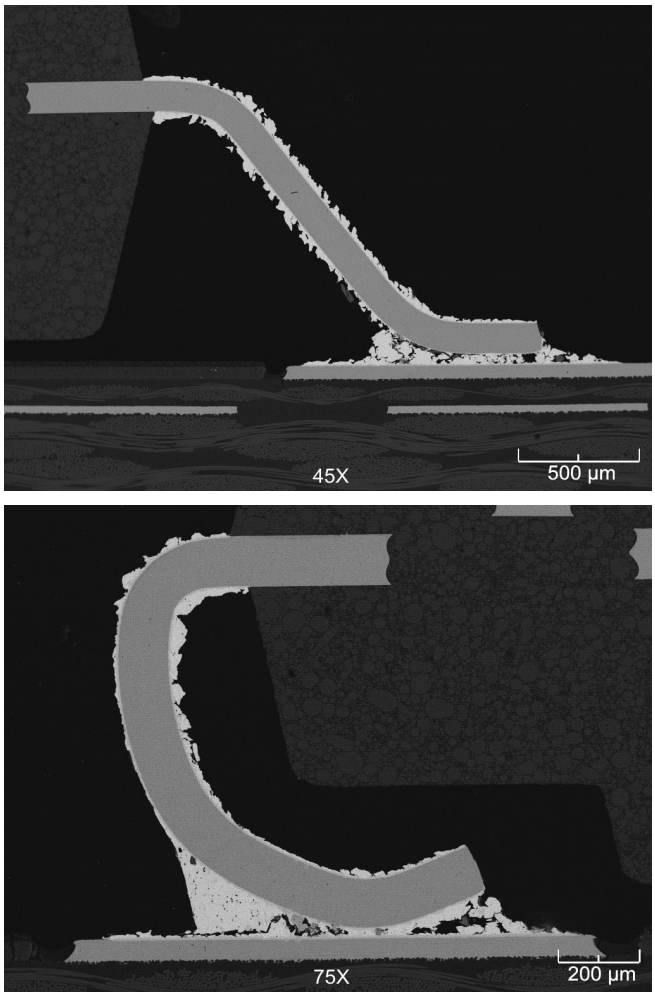

Figure 16. SEM images of cross-sections of the gullwing (top) and J-lead (bottom) solder joints of the 172 MaxQFP from Pad D following cycling to failure. Cross-sections were performed at 12,018 board-level -40 to 125ºC thermal cycles.

SUMMARY AND CONCLUSIONS

The following can be concluded as a result of this MaxQFP package development effort and associated assembly and reliability evaluations:

- A novel and evolutionally package was developed that combines the J-leads of a PLCC and the gullwing leads of a conventional QFP to greatly increase IO density.
- Besides being a potential replacement for conventional QFP where increased density and/or smaller form factor are required, MaxQFP may also provide an acceptable and more economical packaging solution than BGA at lower lead counts.
- MaxQFP has been demonstrated to meet or exceed AEC Grade 1 component-level reliability requirements including the additional requirements placed upon Cu wirebond devices.
- SMT studies showed that excellent soldering yields and robust solder joints could be achieved. Three different PCB pad geometries were evaluated and all resulted in 100% SMT yield. A PCB pad geometry where the gullwing and J-lead pads were both 1.45×0.28 mm resulted in the best cycles to first failure.
- Future extensions of the technology may include an exposed pad for better thermal performance, finer pitches including 0.5 mm and additional body sizes than the 10×10 and 16×16 mm that have been implemented to date.

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