Assembly Optimization for Thin Flip-Chip Chip-Scale Packages

Trent Uehling, CS Foong
NXP Semiconductors
TX, USA
Trent.uehling@nxp.com

ABSTRACT
Coreless embedded-trace flip chip package substrate technology has emerged as an effective solution for Bond-on-Trace (BoT) chip attach in Flip-Chip Chip-Scale Package (FCCSP) technology. With this substate technology comes a reduction in package substrate thickness by 75% or more. Since the semiconductor die and package mold cap thickness do not scale at the same rate, the resulting coreless package has a higher die and mold cap thickness to substrate thickness ratio than conventional cored packages. In this situation, the silicon die and mold compound mechanical properties become more dominant in affecting package warpage both at room temperature and during PC board assembly reflow. The differences may manifest in shape, magnitude and direction of package warpage. In Surface Mount Technology (SMT) board attach, the impact of package warpage can be most observed at the package corners. Bending of the corners towards the PC board, sometimes referred to as "frowny face" at peak reflow temperature can result in bridged solder joints, while lifting of the corners, often referred to as "smiley face" can result in Head in Pillow (HiP) defects. In this study, PC board design and solder stencil designs are evaluated for board attach defectivity for core-less FCCSP packages. It is observed that with properly engineered package materials and mechanical configuration, as well as optimization of PC board pad design, a robust board assembly solution exists for thin FCCSP packages.

Key words: SMT, BGA, FCCSP, coreless.

FLIP CHIP – CHIP SCALE PACKAGE (FCCSP)

The term "FCCSP" defies succinct definition. While the name implies a package with a size the same as the semiconductor chip within, in many cases the package is considerably larger than the chip. For the purpose of this discussion, FCCSP is defined as a small BGA package with size and BGA pitch on the order of what one would find with a semiconductor chip, not larger than 15mm x 15mm. FCCSP packages are typically overmolded and underfilled with epoxy mold compound in a single step, resulting in a structure as shown in figure 1.

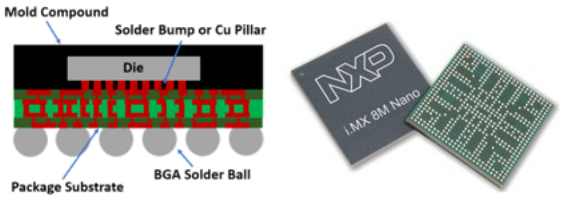


Figure 1. FCCSP Cross-Section and Package View

FCCSP packages are assembled in what is known as a 'strip format". In this format, multiple package substrates are contained in an array, referred to as a "strip". The semiconductor die are placed on the array, reflowed and then overmolded with an epoxy mold compound. In many cases the die is underfilled with the epoxy mold compound during the same process step. Solder balls are then added prior to singulation of the strip into individual packages. Figure 2 illustrates a high-level FCCSP process flow. Measures are taken in the substrate strip design and manufacture, as well as in the package assembly process to minimize strip warpage. Once the completed FCCSP strip is sawn into individual packages, internal mechanical stresses will cause the packages to warp to some degree.

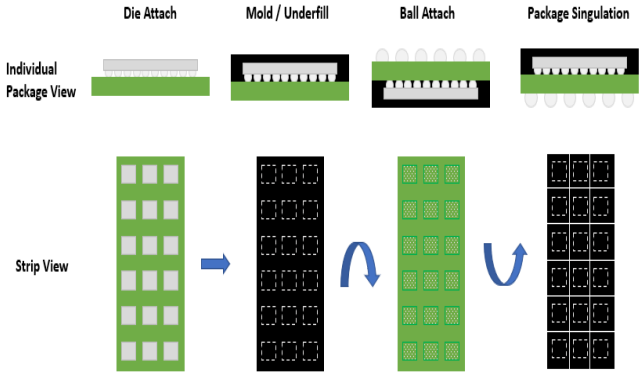


Figure 2. FCCSP Process Flow

Coreless package substrate technology offers advantages over traditional "cored" technology such as lower parasitic resistance, inductance and capacitance, as well as higher interconnect density for fine pitch and high I/O applications [1]. The higher interconnect density can lead to an opportunity to reduce package layer count, as more signals can be routed per layer, and in some cases all signals can be escaped in a single layer (figure 3). These advantages are derived from the inherently thinner layers and overall thickness of the coreless substrate as shown in figure 4. While offering significant electrical benefits, the thin coreless substrate technology does introduce package and board assembly challenges as will be discussed later in this paper.

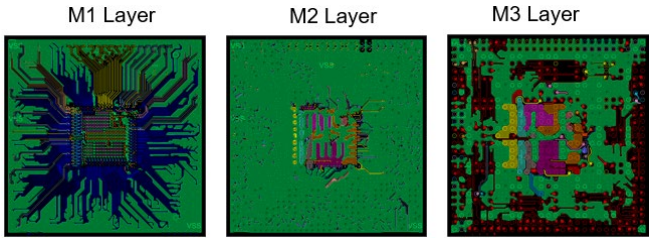


Figure 3. 3-layer coreless substrate 1-layer signal escape example

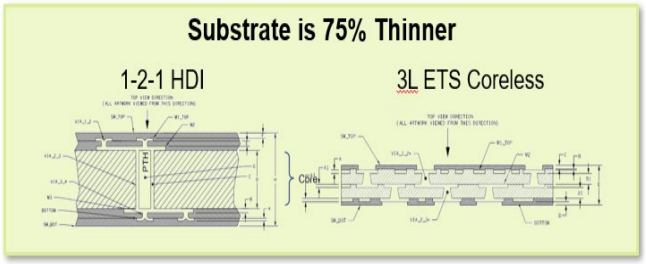


Figure 4. 3-layer coreless substrate thickness compared to 4-layer HDI

THE PACKAGE WARPAGE CHALLENGE

While coreless substrate technology offers improved performance and higher routing and escape density, the stiffness of the substrate core is sacrificed, which has negative influences on strip and package flatness. The thinner substrate amplifies the effects of the silicon die area and thickness. Figure 5 shows a partial cross-section of a typical coreless FCCSP package, illustrating the relative thicknesses of the die and substrate. On the one hand, the silicon die thickness can be increased to "stiffen" the package and keep it flatter. This is only beneficial in a "window" of die to package size ratio. On the other hand, the thicker die increases stress at the Cu pillar interface on the die, and can lead to delamination within the die, sometimes referred to as "ghost bumps" because of the resulting acoustic microscopy image.

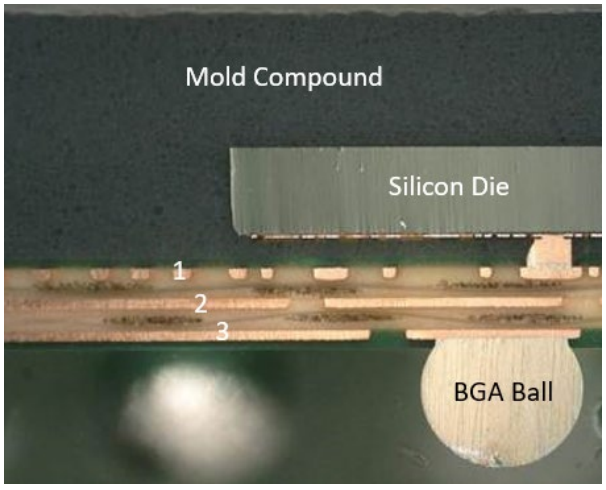
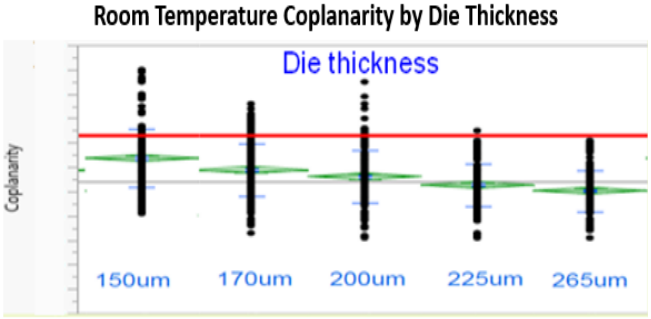


Figure 5. Partial cross-section of 3-layer coreless FCCSP package

In figure 6 is shown the effect of die thickness on package coplanarity at room temperature and also the impact of die thickness on die delamination under the Cu pillar. It can be observed that thicker die does result in a flatter package. But at the same time, the thicker die increases the risk of die delamination in accelerated stress testing. The die thickness must therefore be optimized to compromise both package warpage and die stress.



Die Delamination under Copper Pillar

Die Thickness (um)	As Assembled	3x Reflow	5x Temp Cycle
150	0/89	0/89	0/89
175	0/89	0/89	1/89
200	0/89	0/89	1/89
225	0/89	0/89	1/89
265	0/89	6/89	10/89

Figure 6. Relationship between die thickness, package flatness and die delamination under the CuP

In addition to room temperature BGA coplanarity, another perhaps greater concern is package warpage during board assembly reflow. The difference in material mechanical properties between the package substrate, silicon die, and epoxy mold compound create a dynamic situation where the package will change shape during the reflow process. Figures 7 and 8 show 3-D and diagonal thermal shadow moiré warpage plots of a coreless FCCSP package at room temperature, 150ºC and 245ºC. These measurements are taken with the package in the "dead bug" orientation, BGA-side up. Note that package corners bend slightly toward the PC board at room temperature. At 150ºC the package is in its flattest state, as it is close to the stress-free state of the package. With further heating to a peak temperature of 245ºC, the corners then bend further (compared to room temperature) toward the PC board. With the Pb-free solder balls molten at peak temperature, the bending of the corners in the direction of the PC board may cause solder to push out to its nearest neighbor, resulting in a solder bridge (Figure 9). Once the solder bridge is formed with the solder in its molten state, surface tension makes it nearly impossible to break the bridge as the package flattens during cooldown to solder solidus temperature.

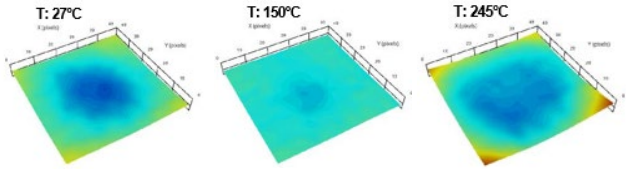


Figure 7. Typical out of plane displacement 3-D plots of a coreless FCCSP package at three temperatures. Package is "dead-bug", BGA-side up.

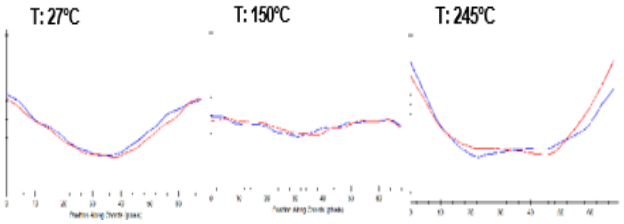


Figure 8. Typical out of plane displacement diagonal plots of a coreless FCCSP package at three temperatures. Package is "dead-bug", BGA-side up.

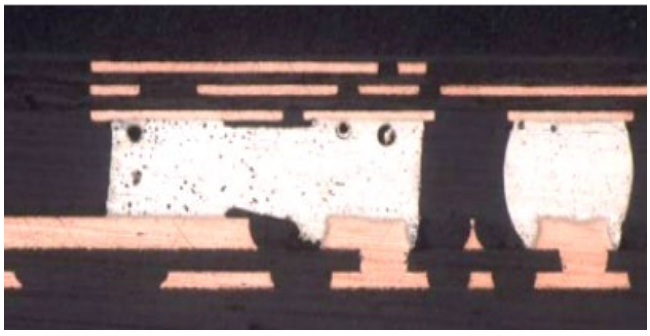


Figure 9. Example of solder bridge between soldermask-defined and non-soldermask-defined BGA pads.

Several factors in the FCCSP process and materials can be adjusted to minimize the amount of package warpage during reflow. Even with an optimized recipe, thin FCCSP packages will tend to warp more during reflow than thicker packages.

EXPERIMENTAL BOARD DESIGNS

Three PC board BGA pad designs are evaluated with the output being solder bridging detected by x-ray. The pad designs are summarized in table 1, and images of each design are shown in figures 13 through 15. For all board designs, signal pads are NSMD. Only the GND pads differ.

Table 1. Experimental board designs

Board Design	Corner GND	Corner Signal	Center GND Plane
Mixed SMD/NSMD	SMD	NSMD	SMD
Corner NSMD	NSMD	NSMD	SMD
Full NSMD	NSMD	NSMD	NSMD

The first of the designed experiment board designs is referred to as "mixed SMD/NSMD". The corner GND BGA pads are SMD. Center GND pads are SMD with 13mil soldermask opening.

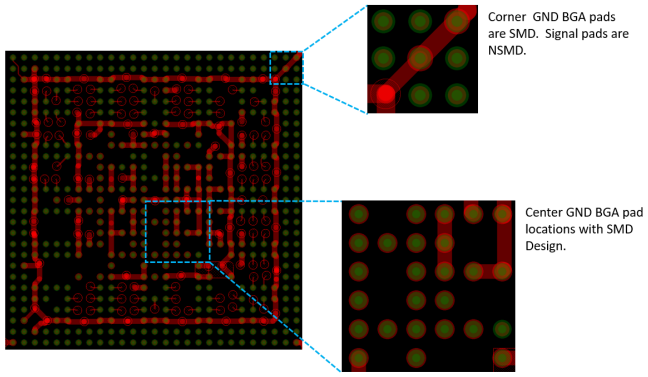


Figure 13. Mixed SMD/NSMD BGA pad design.

The "Corner NSMD" board design has all pads in the corner 3x3 array designed as NSMD. GND pads are connected with a 4mil line, similar to the signal pads. Center GND pads are SMD with 13mil soldermask opening.

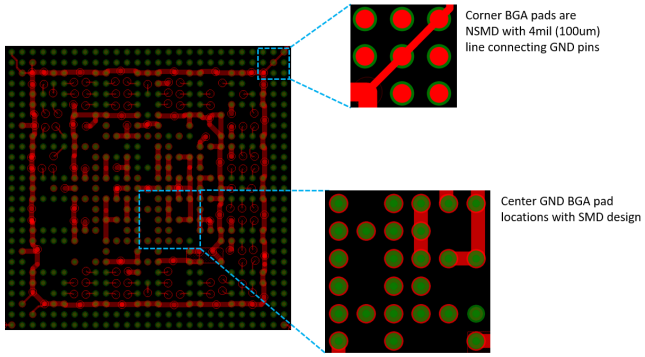


Figure 14. Corner NSMD BGA pad design.

The "Full NSMD" board design has all pads designed as NSMD. GND pads are connected with a 4mil line, similar to the signal pads.

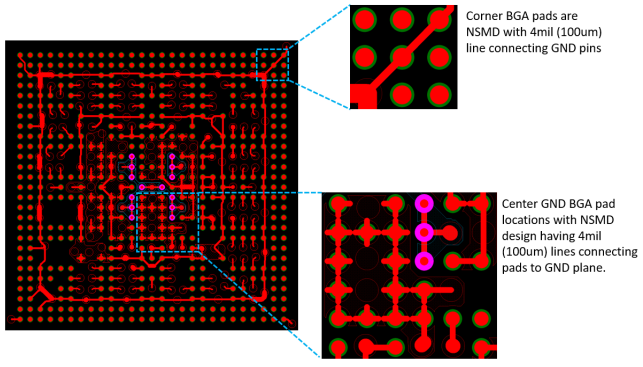


Figure 15. Full NSMD BGA pad design.

Two instances of the three BGA pad designs are placed on a single PC board for the board assembly evaluation. The final PC board layout is shown in figure 16.

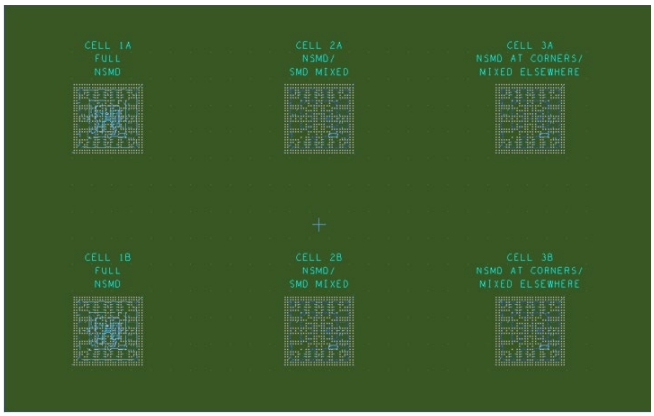
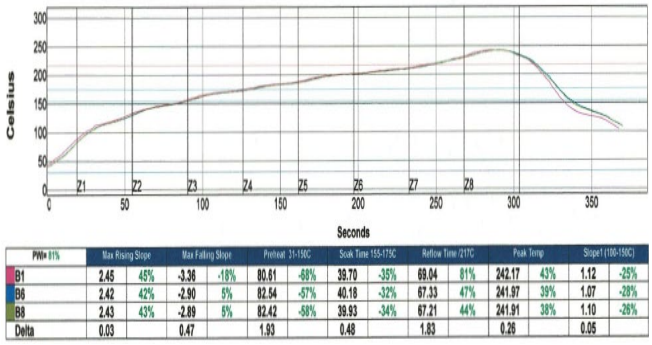


Figure 16. Experimental PC board layout.

RESULTS AND DISCUSSION

FCCSP packages were assembled using various recipes which are known to produce different characteristic warpage at 245ºC. Thermal moiré was performed on a subset of each lot to characterize the package warpage at 245ºC. Based on the warpage values, 3 populations were selected based on characteristic warpage at 245ºC. The 3 populations were < 110µm, < 120µm and > 120µm 245ºC warpage.

Board assembly was performed by standard Pb-free SMD process. The peak solder joint temperature was kept between 240ºC and 245ºC (figure 17) to minimize package warpage during reflow. The solder stencil was 4mil thick with 10mil round apertures.



PWI= 81%	Max Rising Slope		Max Falling Slope		Preheat 31-150C		Soak Time 155-175C		Reflow Time (217C		Peak Temp		Slope1 (150-150C)	
B1	2.45	45%	-3.36	-18%	80.61	-68%	39.70	-35%	69.04	81%	242.17	43%	1.12	-25%
B6	2.42	42%	-2.90	5%	82.54	-57%	40.18	-32%	67.33	47%	241.97	39%	1.07	-28%
B8	2.43	43%	-2.89	5%	82.42	-58%	39.93	-34%	67.21	44%	241.91	38%	1.10	-26%
Delta	0.03		0.47		1.93		0.48		1.83		0.26		0.05	

Figure 17. Experimental reflow profile.

Each location was subjected to x-ray to detect solder bridging between locations. Solder bridging can easily be detected by x-ray as shown in figure 18 which shows 3 corner BGA locations bridged in an "L" shape.

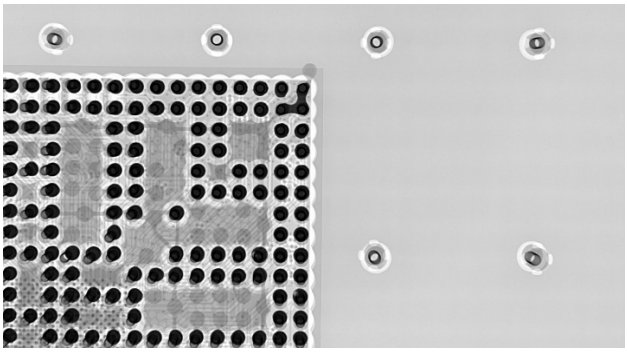


Figure 18. X-ray image of solder bridging

The x-ray results are summarized in table 2. The assembly recipe with < 110µm warpage at 245ºC had no solder bridging regardless of PC board BGA pad design, while the recipe with < 120µm warpage had one unit bridge with the "mixed" pad design. The units with > 120µm warpage had significant bridging on the "full NSMD" and "mixed" design, but still yielded 100% with the "corner NSMD" design.

Table 2. Solder bridging count by warpage and design

Results by 245C Warpage and Board Design			
	<110um	< 120um	> 120um
Full NSMD	0/148	0/18	5/30
Mixed	0/148	1/18	6/30
Corner NSMD	0/148	0/18	0/30

The results for the "mixed" board design met the expectation that this design would have the largest fallout for solder bridging. If an SMD BGA pad configuration is adjacent to an NSMD pad near the package corners, the potential for solder bridging exists while the solder is molten, as the solder from the SMD pad can flow on top of the soldermask to the adjacent pad. (Figure 19).

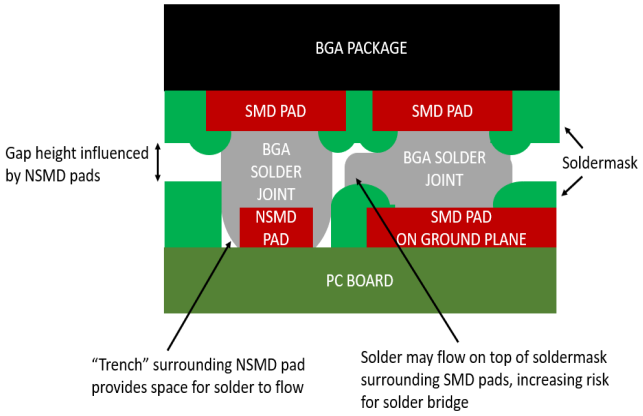


Figure 19. Combination of SMD and NSMD pads, especially at package corners may create a potential for solder bridging.

The "full NSMD" design was expected to result in the lowest incidence of solder bridging since this configuration creates a "reservoir" into which molten solder can flow during the dynamic movement of the package which may compress the gap distance between the package and PC board temporarily at the corners. In fact, the "full NSMD" design showed significant bridging in the population of packages with 245°C warpage > 120µm.

The "corner NSMD" design performed the best with no solder bridging regardless of characteristic package warpage, which was quite unexpected. This design was included because often manufacturing or electrical constraints prohibit the use of NSMD pad design over ground planes, for this reason, a "compromise of mixed SMD and NSMD design may be used outside of corner regions which are defined by a 3 × 3 BGA array at each of the four package corners. See Figure 20.

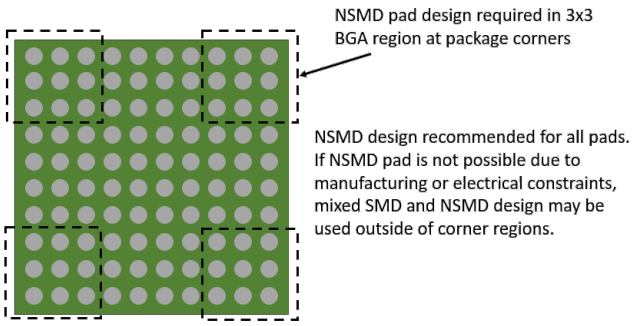


Figure 20. Corner NSMD design.

The reason for the superior performance of the "corner NSMD" design is not yet fully understood. One theory is that the central SMD pad locations on the GND plane control the gap height between the package and PC board, preventing total collapse of the corner NSMD pads. The full NSMD design would have a lower average gap height, increasing the potential for bridging at package corners where gap height is even lower. To validate this theory, a surface evolver simulation of the NSMD and SMD solder interconnects was performed. The simulation results shown in figure 21 did show that the SMD configuration would result in a larger gap height, but only by 4µm (138µm vs. 134µm for NSMD design).

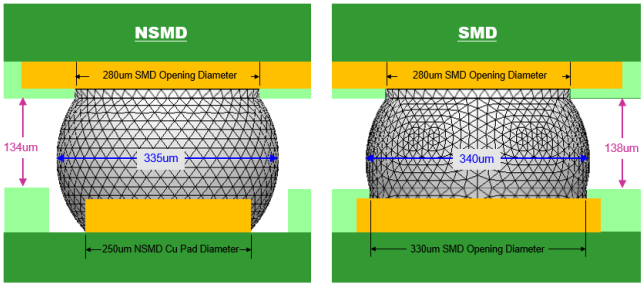


Figure 21. Surface Evolver simulation of NSMD and SMD solder interconnect shape and gap height.

As a 2nd verification, mechanical cross-sections of "full NSMD" and "corner SMD" designs were performed. The "corner SMD" design resulted in a higher average gap height of ~182µm compared to ~172µm for the NSMD design (figure 22). These cross-sections do validate the theory that the central SMD pads do increase average gap between the package and the PC board.

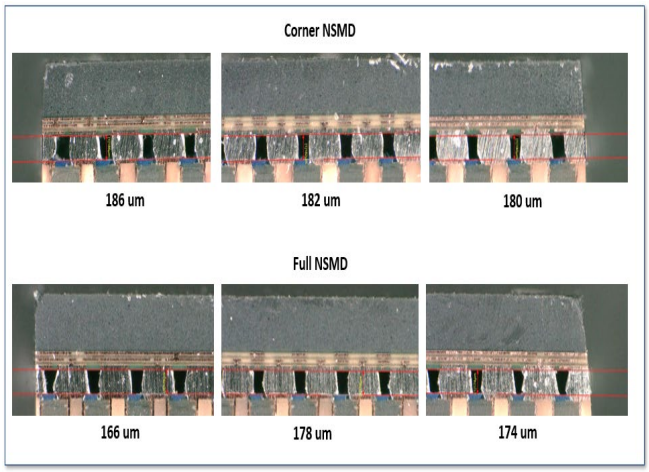


Figure 22. Cross-section and gap heigh measurements of "corner SMD" and 'NSMD" board designs.

CONCLUSIONS

A robust board assembly recipe is demonstrated for thin FCCSP packages with reflow warpage values of up to 110µm or higher. Keys to a robust board assembly process are:

1. Board reflow profile verified with temperature sensors located at package top and BGA solder joint.
2. Component top and BGA solder joint temperatures less than 245°C during reflow.
3. Non-soldermask defined PC board pad design at a minimum in package corners.
4. Solder stencil aperture diameter matching PC board pad diameter or slightly reduced.
5. Stencil apertures in corner regions reduced by 10% to 15%.

Best results were achieved with NSMD board pad design in corner regions which are defined by a 3 × 3 BGA array and all other BGA pads designed with a mix of SMD on ground planes and NSMD elsewhere. This "corner NSMD" design results in higher overall gap height while still creating the "reservoirs" in the corner locations into which molten solder can flow during the dynamic movement of the package. Where SMD pads are used, it is recommended that the SMD solder resist opening is 0.050mm larger than the NSMD pad diameter used elsewhere.

The infrared or convection reflow requires a solder joint temperature (SJT) of 235 - 245°C, not exceeding 245 °C, and should follow the recommendation of the solder paste manufacturer, including the solder alloy being used. NXP recommends that Package Peak Temperature (PPT) should not exceed 245 °C, as higher temperatures may contribute to soldering defects.

ACKNOWLEDGEMENTS

The authors would like to thank Phyllis Vasquez, Mike Fuller, Alvin Youngblood and Roy Arldt for thermal moiré, x-ray and failure analysis support, and Betty Yeung for Surface Evolver modeling. We also would like especially acknowledge Jeff Davis and the team at ATE Design for PC board design, assembly and analysis support.

REFERENCES

[1] Wang, James, et al. "Coreless Substrate for High Performance Flip Chip Packaging." *2010 11th International Conference on Electronic Packaging Technology and High Density Packaging.* (2010).