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# Aerosol Jet Printing SIR Patterns on Real World Components – The Potential for Value-Added Real-World Data

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## ABSTRACT

Cleanliness validation of printed circuit assemblies has become more and more important as electronics progress to becoming smaller, denser, and more difficult to clean, prompting an increase in reliance in custom solutions. With increasingly fast paced development cycles, long lead times and costs of quality custom surrogate test boards become prohibitive in obtaining cleanliness data that is a true representative of the final product. In this study, aerosol jet printing, an additive manufacturing technology for electronics, was used to manufacture surface insulation resistance (SIR) test structures that were tested in the ability to detect cleanliness defects and provide stable results when none are present, as well as their survivability to standard electronics wash processes. Additionally, SIR test structures were printed directly onto ball-grid-arrays (BGAs) and tested the survivability of conformally printed leads for data acquisition. SIR test structures displayed good wash survivability on standard FR4 and BGAs, including wraparounds for on-component prints, and high sensitivity to cleanliness defects. The presented results demonstrate the feasibility of printed SIR structures as a quick-turn, highly customizable solution with potential for high fidelity cleanliness testing.

Key words: SIR, Additive Manufacturing, Printed Electronics, Aerosol Jet Printing

## INTRODUCTION

Cleanliness in printed circuit assemblies (PCAs) is essential to the reliability of electrical systems, especially when the device is required to be in operation for a long life without failure. Through rapid evolution driven by technological advances in fabrication, PCAs have been moving towards miniaturization of commercial off the shelf (COTS) components, increased board population density, as well as increased array of processing materials, presenting challenges to current methods for cleanliness testing [1]. Surface insulation resistance (SIR) testing on surrogate test boards is one of the most widely accepted cleanliness testing methods to detect the presence of processing soils such as fluxes, cleaning solutions, and foreign contaminants that can result in immediate and latent functional failures in the form of leakage current, dendritic growth, and shorted circuits [2]. While COTs SIR testing boards provide a cheap solution to gain a sense of how effective the wash process can be, they are not fully representative of the cleanliness of actual product due to differences in vendor, board type, material, and effects of neighboring components on the ability to clean underneath components. The need for higher reliability in test results has led to a growth in demand for custom solutions, however, long lead times and higher costs for custom test boards can be prohibitive for rapid development cycles that require a faster paced solution. Additive manufacturing (AM) of electronics, better known as printed electronics, present an avenue for rapid prototyping due to the speed and control of fabrication, made possible through computer aided design (CAD)[3].

In this study, SIR test structures manufactured through Aerosol Jet Printing (AJP), a material jetting AM technology, on standard boards were evaluated on their ability to withstand the rigorous cleaning process and performance under standard testing conditions. Preliminary test results revealed the potential for use of printed SIR test structures as an alternative method to evaluate the cleanliness of boards, performing on par with traditionally manufactured test boards by capturing cleanliness defects when present and reporting stable results when clean. Additionally, development efforts were made to print SIR test structures on the underside of COTS components such as BGAs and PBGAs, PATENT PENDING. By wrapping testing pads around the components and through the use of a custom test clip, SIR test data could be obtained from the underside of components without the need of an SIR test board, making printed on-component SIR test structures a prospective solution for quick turn testing on production parts. Furthermore, printed SIR test structures provided a repeatable platform for initial evaluation of designs to study the performance difference in terms of capacitance across boards and components in an effort to develop a standardized approach to cleanliness evaluation.

## SIR PATTERNS PRINTED ON BOARDS

### Aqueous Wash Survivability

Printed SIR test structures need to survive the wash process that standard SIR sensors are exposed to and produce reliable data regarding the cleanliness conditions of the packages they are monitoring. For initial wash testing experiments, SIR test structures were printed onto a borosilicate glass substrate, PATENT PENDING (Figure 1), soldered onto a custom SIR test board, and subsequently subjected to multiple cleaning cycles. The printed SIR test structures were characterized before and after the wash process to inspect for degradation and damage. Results revealed mechanical failure at the joints of the digitations in the sensor due to delamination of the printed silver from the glass substrate (Figure 3) as a result from weak adhesion between the silver traces and the substrate.

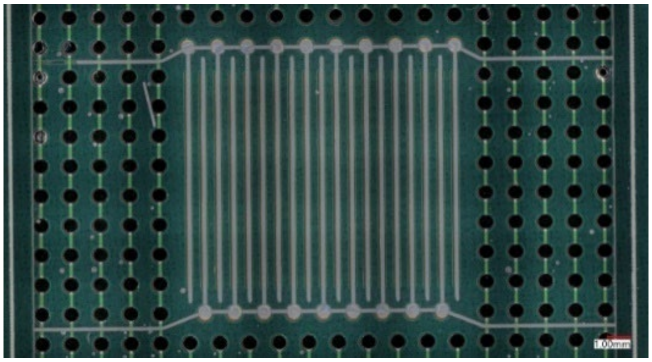

**Figure 1.** Micrograph of printed SIR test structure on glass substrate, post-wash.

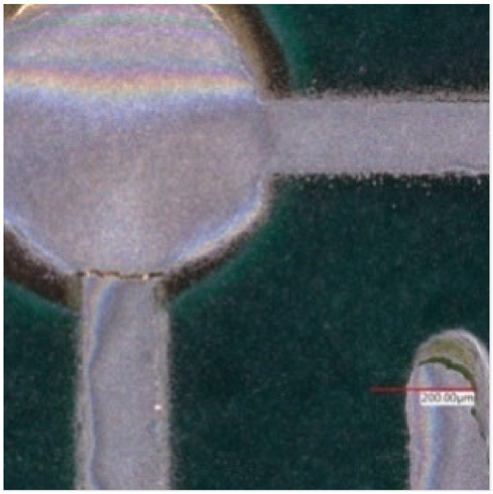

**Figure 2.** Micrograph of printed SIR test structure, post-wash.

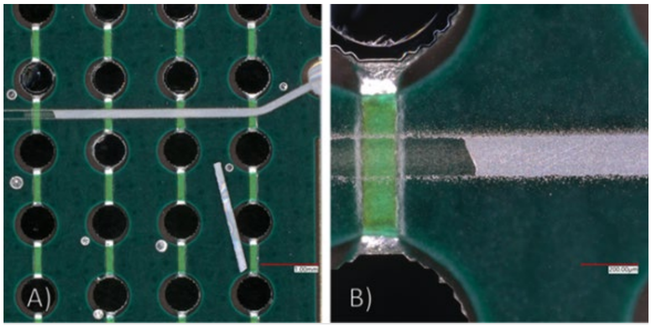

**Figure 3.** a) Fracture of printed SIR test structure and b) close-up of the fracture surface

In subsequent wash test experiments, SIR test structures printed on standard FR4 boards with vias (Figure 4) were subjected to multiple cleaning cycles at an Electrovert AS200DWASS Aqueous Cleaner. Additionally, the boards were printed with variation in the number of layers used to print the SIR sensors. The printed SIR sensors and the connection vias were characterized before and after the wash process to inspect for degradation and damage. Results revealed that the printed silver has significantly better adhesion to FR4 in comparison to the glass substrates. While continuity was preserved at the vias, improvements need to be made at the interface between the silver trace and the vias. Furthermore, there was no notable difference between the SIR test structures printed in multiple layers in terms of process survivability, however, some degradation was noticeable in one of the printed SIR pads made from multiple layers which can be improved through sintering optimization.

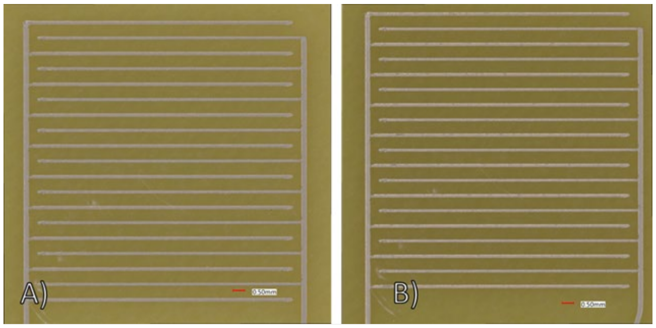

**Figure 4.** Micrograph of printed SIR test structures printed on FR4, post-wash.

**Surface Insulation Resistance Testing**

Printed SIR test structures need to perform reliably and provide accurate data when exposed to the temperature and relative humidity used to test traditional SIR sensors. SIR test structures were printed onto three FR4 boards that were not cleaned and placed inside an environmental chamber for seven days at 60 °C and 80% RH. The response of the printed SIR sensors and their potential to survive the testing environment were evaluated by analyzing resistance changes. The summarized results in Figure 5 demonstrate three different cases observed. SIR test structures that underwent the wash process prior to testing (Clean) show stable results and high resistance above $10^{12}$ Ohms. Two separate cases of failure were observed on test boards that were not washed. In the first instance, leakage current and oxidation of the printed SIR test structure (Figure 6.A) was observed. These type of cleanliness defects were likely due to the presence of residual fluxes from prior usage of the test boards. In the second instance, a short was observed in the measurement readings. Further inspection revealed a fiber through which silver migrated through (Figure 6.B), creating a wire that shorted the SIR test structure.

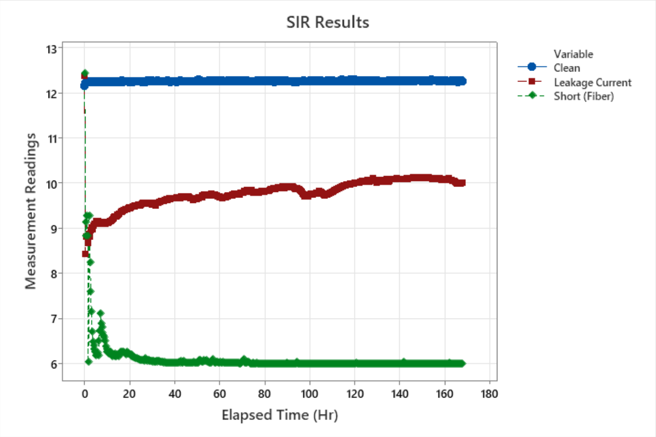

**Figure 5.** Summarized result of SIR testing for three cases, clean test structures, test structures with evidence of leakage current, and short circuits.

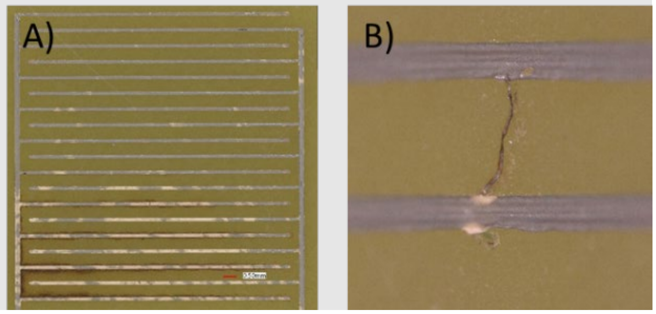

**Figure 6.** Micrograph of defects in printed SIR test structures demonstrating A) leakage current events as well as B) short circuits caused by the presence of a fiber.

A second study (Figure 7) was done on a set of SIR test structures printed on FR4 boards that were processed through the wash to compare the response of printed SIR patterns to commercially available test boards. Anomalies in the response of the printed SIR patterns were observed on 042-PAD-4 where resistance started in the $10^9$ Ohm range and did not go above $10^{11.5}$ Ohms. Inspection revealed manufacturing defects from the printing process in the form of streaking at the edges of the left comb structure (Figure 8.A) which were addressed through toolpath design and parameter optimization.

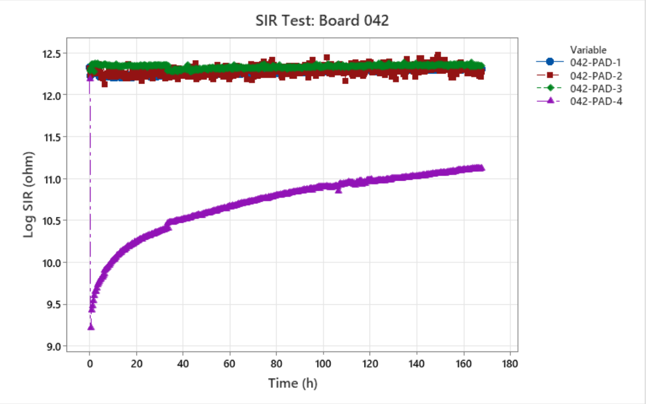

**Figure 7.** SIR testing results for printed test structures on washed test boards.

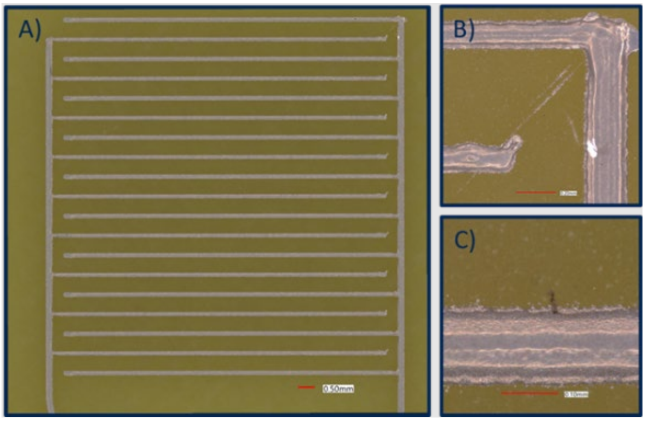

**Figure 8.** Streaking defect observed on printed test structure 042-PAD-4 of Figure 7 due to printing parameters.

Initial tests revealed the potential for printed SIR test structures to capture events cause by cleanliness issues such as short circuits and leakage current from the presence of foreign contaminants. Additionally, these tests show stable performance in the absence of cleanliness defects, demonstrating the potential for printed SIR test structures to be used as an ancillary cleanliness test.

## SIR PATTERNS PRINTED ON COMPONENTS

The ability to print SIR patterns directly onto a component, whether on a "practical component" or a production part, enables the testing of production assemblies. With testing on actual product, greater assurance that cleanliness requirements are being met rather than just assuming that the test coupon is representative enough of your production part. Additionally, these can be fabricated in a matter of hours versus the weeks and high costs of obtaining custom designs from an outside vendor. Through continued printing, testing multiple design aspects, as well as testing in comparison with traditional methods, this has proven to be a very effective way to perform SIR cleaning testing.

Aerosol Jet Printing's ability to pattern in high resolution along with its contactless deposition method, helped extend the application space of printed SIR test structures beyond boards and onto various components such as ball-grid arrays (BGA), quad flat no-lead packages (QFNs), and quad flat packages (QFPs). Furthermore, the thickness of printed traces (100-200 nm) allowed for the printing of SIR test structures that do not interfere with mounting and standard processing of the component, including washes. As an initial proof of concept, SIR test structures were successfully printed on the underside of plastic ball-grid arrays (PBGAs), PATENT PENDING (Figure 9). Resistance and capacitance measurements were obtained from the landing pads on the edges of the PBGA.

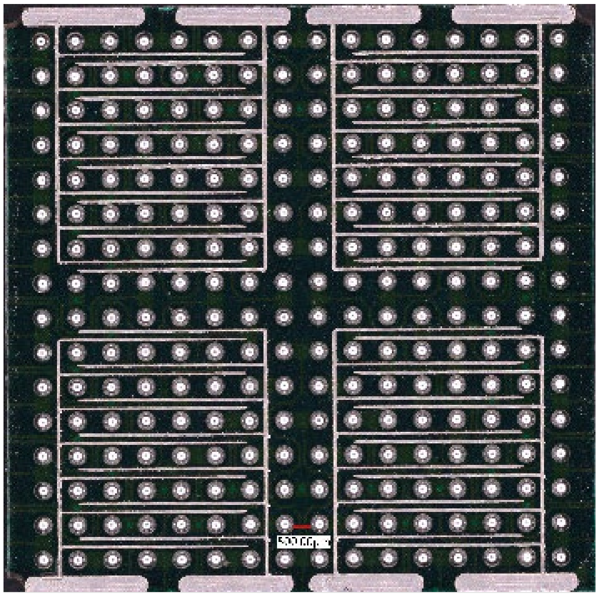

**Figure 9.** Micrograph of printed SIR test structure on a ball grid array.

While printing on the component provides valuable information, obtaining data from the component through this method proved to be impractical for probing the underside due to the limited space between the board and component. By taking advantage of the 5-axis capability of the aerosol jet printer, the probing pads were wrapped around the PBGA. To enable the integration of the printed test structure with the SIR tester, a small profile test clip was developed to securely latch onto a device under test. The test clip relied on a compliant mechanics to provide enough gripping to remain secure through the entirety of the test and used pogo pins to ensure proper contact of the test leads to the wrapped pads, PATENT PENDING. Additionally, tests were done to evaluate the survivability of the wrap arounds, especially in tight bends. Initial results demonstrate good adhesion without any noticeable degradation of the traces.

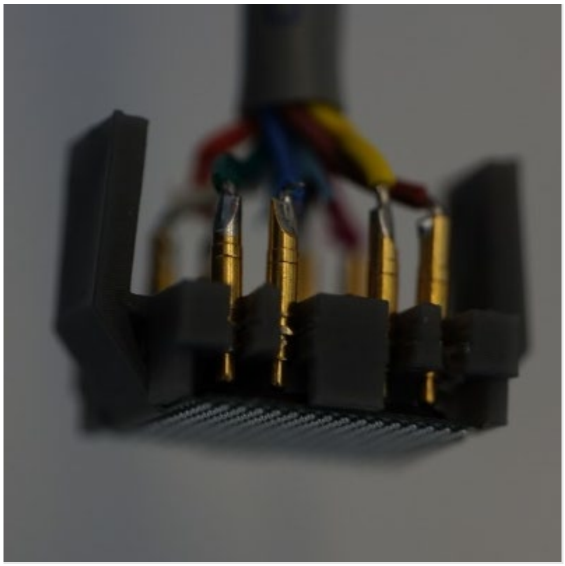

**Figure 10.** SIR test clip prototype gripping a ball grid array.

## DESIGNING PRINTED SIR TEST STRUCTURES

The rapid manufacturing approach and customizability of printed SIR test structures offer a platform to begin understanding how the factors of the design of the comb pattern influence the capacitive response and create a model to tailor these factors and achieve a target response.  A design of experiment was run on SIR structures printed on standard FR4 boards to analyzing the effects of number of fingers, gap, overlap, and width on the capacitive response. From the design of experiments results demonstrated in the Pareto Chart of the Standardized Effect (Figure 9), it was determined that the number of fingers in the SIR pattern and the overlap between fingers are the most significant factors to influence the capacitance of the printed SIR test structures. Additionally, there is a strong interaction between both, followed by the effect of gap length between fingers. While the width of the fingers had a significant effect on the capacitance of the printed SIR test structures, its effects along with the interactions are not as impactful as the other three factors and can be reduced from the model. A confirmation run was done on a standard FR4 board, using the PBGA dimensions as geometrical constraints and produced results that were within the 95% prediction interval.

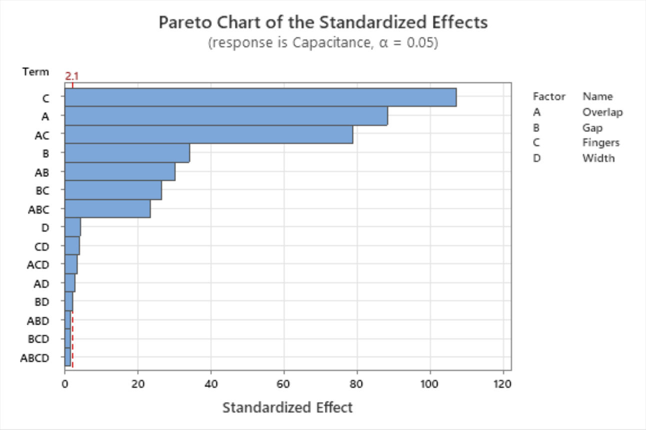

**Figure 11.** SIR test clip prototype gripping a ball grid array.

The model created through the design of experiments serves as the first step towards standardization and producibility of printed SIR test structures. As the design effects begin to be better understood, printed SIR test structures have the potential to provide custom solutions to get closer to answering the question of how clean is clean.

As the design influences on the response of printed SIR test structures become better understood, it is important to also consider how material choices affect the capacitance, especially when translating the same design across various components. The mean capacitance response of SIR test structure printed on a standard FR4 board and PBGAs were compared using the same pattern shown in Figure 12. From the test results (Figure 13), it was determined that the two have statistically significant capacitive responses which would benefit from further testing to discretize the effects of the solder balls from the capacitance measurements.

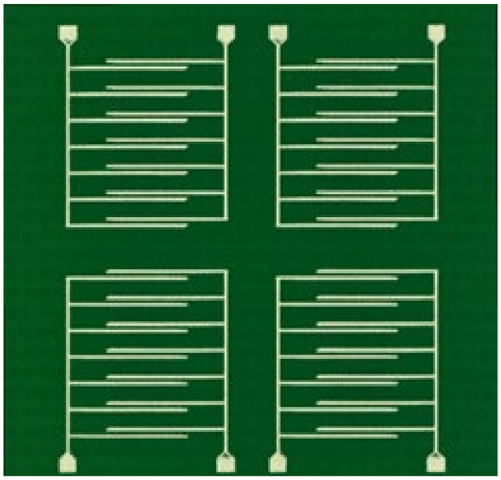

**Figure 12.** SIR test pattern designed to test differences in capacitance across substrates.

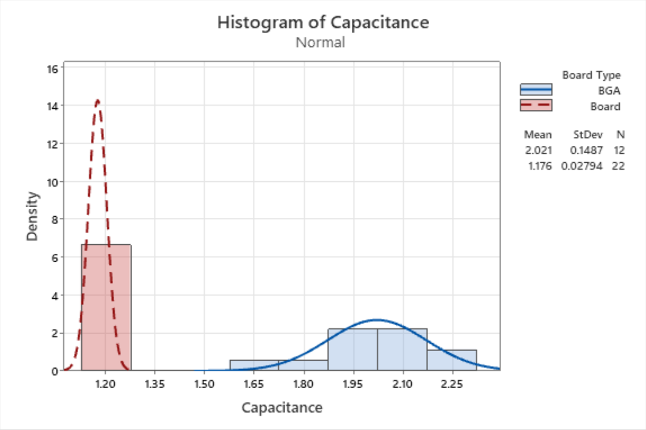

**Figure 13.** SIR test pattern designed to test differences in capacitance across substrates.

## CONCLUSIONS

Printed electronics, or additive manufacturing of electronics, enables enhanced capabilities not available through traditional electronics manufacturing processes and offers a quick turn, custom solution to the manufacturing challenges of surface insulation resistance testing. Aerosol jet printing, a contactless deposition method, has been demonstrated to be a reliable method for fabricating custom SIR test structures that cannot only survive the harsh wash processes electronic boards go through, but also perform up to par with standard SIR sensors by providing high stability when clean and high sensitivity to common processing soils. Furthermore, by employing this technology onto components, these SIR test structures present opportunities for more readily available evaluations alongside current wash validation test methods.

## FUTURE WORK

As printed SIR test structures begin to scratch the surface of the possibilities printed electronics can bring to cleanliness testing, there is still work that needs to be done before the technology can be fully adopted. The correlation between the data obtained from these sensors needs to be made to real-world information to have a better understanding of what each hour of testing translates to in terms of aging and lifetime of the product it is attached to. For this to happen, the differences between the materials used for printing and bulk materials needs to be studied. Once the capability of printed SIR test structures is proven in, then incorporation of other sensors for on-component testing could begin to provide a bigger picture of how clean is clean.

## ACKNOWLEDGMENTS

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