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Advanced Interconnect Process Enables Very High-Density PCB Structures

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Abstract

The need for increasingly complex electronics combined with the obsolescence of larger component packages is driving innovation to provide alternatives to the traditional subtractive-etch fabrication process to reliably and repeatedly provide circuit layers with 25 micron or finer feature size. Liquid Metal Ink (LMI™) technology is one of those innovations.

LMI™ allows a very dense thin catalytic seed layer which results in a very dense thin electroless copper layer that can then be used as a base for a much thicker electrolytic copper layer. Because the electroless copper can be so thin (0.1 µm) compared to the electrolytic copper (> 10um) very fine geometries can be defined with a simple flash etching process without risking undercutting the traces. This is the core technology that allows Averatek's Semi-Additive Process (A-SAP™) to realize very fine feature sizes.

This process is compatible with most printed circuit board (PCB) processes and utilizes conventional PCB equipment. The resulting circuit features can resolve to 25 microns or below, providing a cost-effective solution to complex routing constraints that currently result in multiple lamination, stacked and staggered micro via solutions. LMI™ enables the mixing of a subtractive process with advanced processes such as A-SAP™ in several different ways. This mix and match approach can be used to build a Substrate Like PCB (SLP) and these combinations expand the practicality and performance of the circuit. These very high-density circuit layers can stand alone or can be combined with layers created by the subtractive etch process that do not require such fine pitch. This combination efficiently results in the reduction of total number of layers and lamination cycles.

A higher manufacturing feasibility results from selecting the best manufacturing methodologies for each portion of the target system. This unique ability to combine standard and advanced processes will leverage the current domestic manufacturing infrastructure while extending capabilities well beyond the next generation interconnect.

Introduction

The PCB industry is continuing to grow globally, with High Density Interconnect (HDI) comprising the fastest growing segment. At this pace, HDI will be a $22 billion market by 2025 with >11% CAGR. With the right technology, this growth could occur even faster.

The PCB industry is unavoidably linked to the Semiconductor industry. Dr. Robert Doering of Texas Instruments recognized as a person with "a long and distinguished history as a technologist in the semiconductor industry" stated that progress on … technology will end not because engineers run out of ways to make it still smaller or faster, but because the cost of manufacturing outstrips the value of the advantages. We find that to be true for many technologies in the electronics industry including the PCB industry. It isn't that we can't make progress with the subtractive technologies of today, but these advances are getting to be less and less practical due to increased complexity of the subtractive process to obtain fine lines and features. mSAP, once thought to be imperative for the new age of 5G, has not been able to deliver on the promise of driving down costs as it matures. An alternative is needed that will leapfrog the existing technologies and provide a cost-effective path to the future while generating enough profit to fund investment future advances in technology.

Methodology

A-SAP™ is an additive technology that doesn't depend on expensive thin copper foils. Not only does this allow the standard PCB shop to implement it with only minor changes to the infrastructure used today, but also at a low infrastructure cost apart from equipment to enable the fine line capability of the A-SAP™ process. (Figure 1)

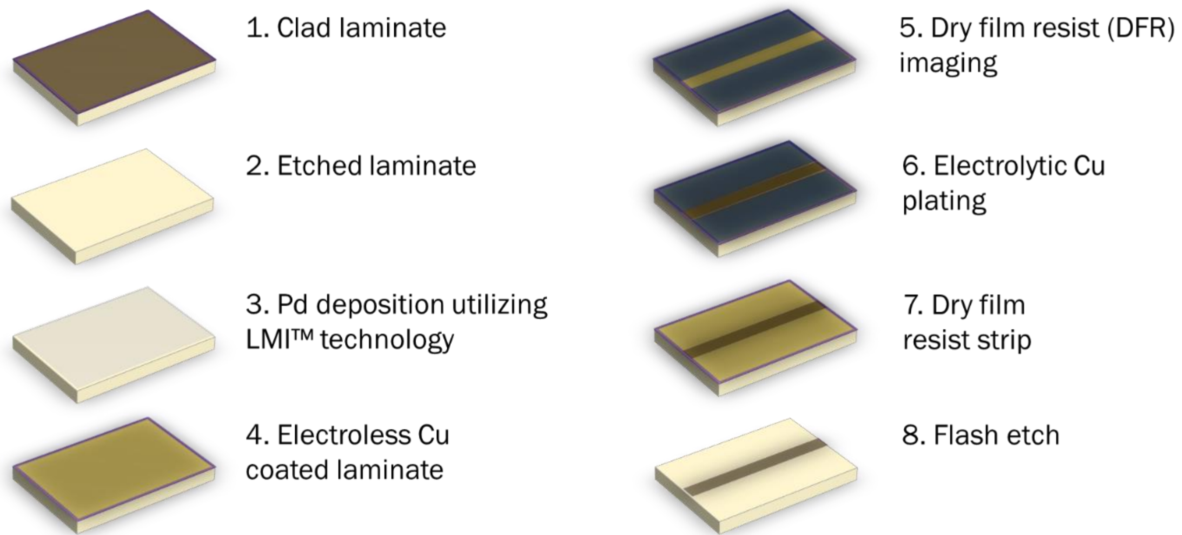
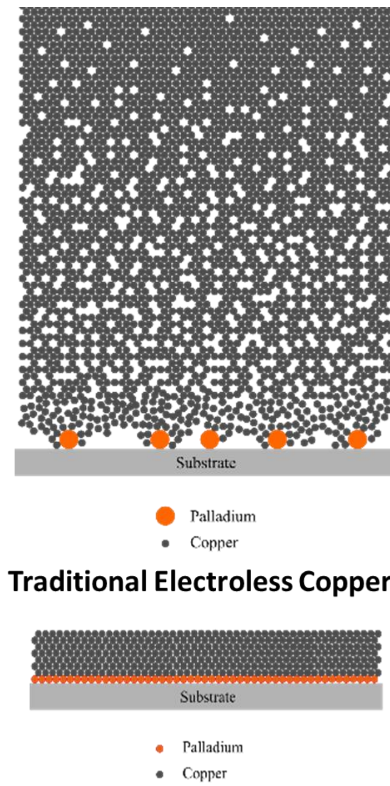


Figure 1 - Averatek Semi-Additive Process (A-SAP™)

The only new step for most PCB shops is the application of the palladium using LMI™. This can be applied by dipping, rolling or spraying. Currently dipping is the most popular method. Next steps of drying and curing can be accomplished in a standard convection oven. Keeping the substrate clean and uncontaminated is important as always, but particle size and contamination levels require more attention than other areas in a conventional shop. The other steps use a different process flow from the subtractive method but are essentially the same steps.

Developing the Dry Film Resist (DFR) can be more challenging but DFR products have been developed for SAP such as RY-5325 from Hitachi and more are being introduced. Stripping is a different challenge since the resist is now embedded between the traces instead of on the top in the subtractive process. Careful process control can overcome these issues on most modern equipment, but each DFR/equipment combination requires process development for optimum performance.

Electroless plating is an auto-catalytic or chemical plating that does not require the use of external electric power. Many modern electroless copper baths are formulated to take advantage of colloidal palladium. However, the LMI™ palladium deposition is uniform, compact and thin, making a thin electroless metal layer conformally on the surface of the dielectric material. This will allow for the use of a broad range of electroless formulations. **Error! Reference source not found.** illustrates conventional electroless and palladium versus the dense Pd seed layer which creates a dense electroless copper layer. This will provide a solid conductor for subsequent additive electroplating. This is a critical characteristic of the A-SAP™ process.



Thin Electroless Copper

Figure 2 - Thin Catalyst Benefits

The dense palladium layer is only nanometers thick and is largely transparent both visually and electrically. This is a result of the LMI™ (ink) and the cleanliness of the coating. The ink and subsequent palladium layer can penetrate the finest features, creating a coating that is both uniform and dense.

These few simple steps are the only additional process requirements in the fine line factory implementing A-SAP™ enabled products.

Data

The thin layer of Pd is often hard to detect, with the best detection method being plating with electroless copper. The following test illustrates the thin dense nature of the ink, but a thicker layer than normal was used so as to be detectable in the transmission electron microscope (TEM), shown in Figure 3.

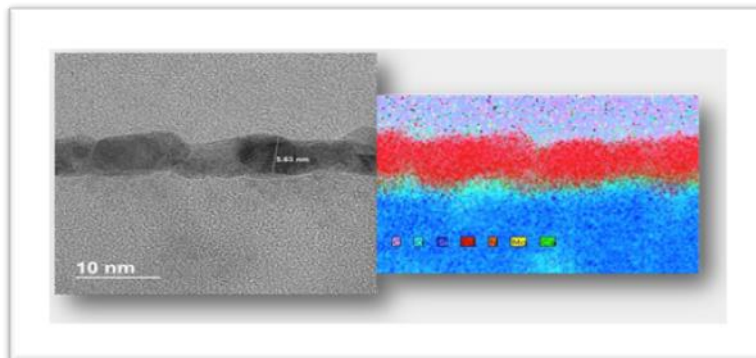


Figure 3- Thin palladium layer shown in red

This example is on a glass sheet that shows the silicon below and the carbon above. The 5 to 6 nm layer is still very conformal to the surface of the glass. Normally in PCB manufacturing the layer is ~2 nm thick, which is barely perceptible.

When used to support thin copper plating using the A-SAP™ process, the dense ink allows us to apply a sub-micron thickness of electroless copper, usually 200 to 400 nm, that gives us a base for copper electro plating of the traces. Figure 4 shows an example of the A-SAP™ method prior to striping the electroless copper.

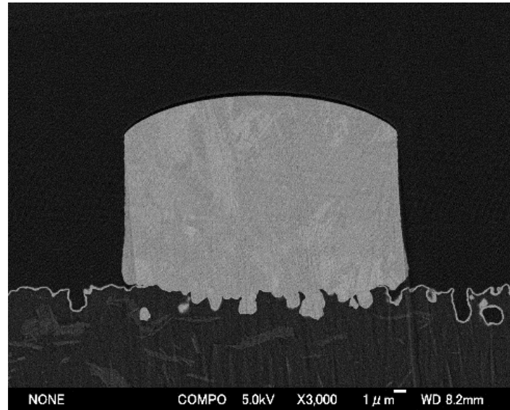


Figure 4 - Thin electroless copper base with electroplated trace

In contrast, copper foil 3 µm thick is widely used for the mSAP method, will require a great deal more etching and will reduce the trace width as a result. The reduced trace width of several microns, along with the removed trace height creates smaller traces than what was originally formed, prior to etching. Very fine spacing, required for coplanar waveguides for example, will benefit from narrower and more accurate trace formation.

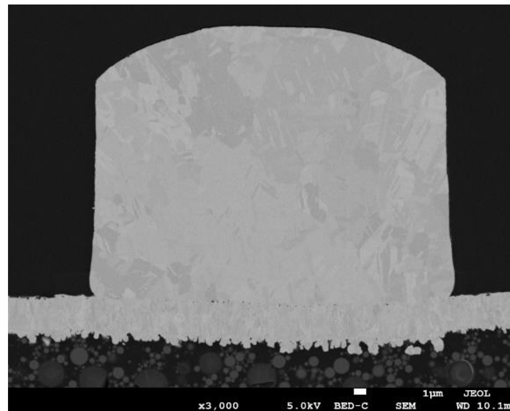


Figure 5- - mSAP with 3 um copper foil

In many examples, 0.4 µm of copper was etched away from the top of the copper trace in the A-SAP™ method but only 0.04 µm was removed from the sides of the trace, shown in Figure 6.

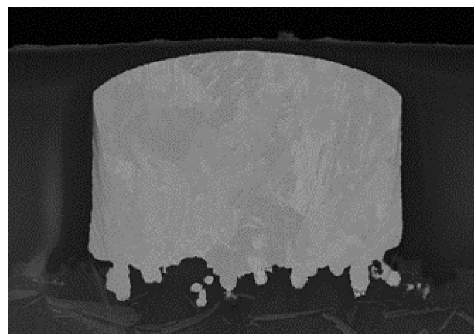


Figure 6 - Etched A-SAP finished trace

The conformal nature of the base copper provides for several manufacturing advantages. The ability to penetrate the cavities in the surface even beyond the line of sight is a distinct advantage over other thin coating methods such as sputtering. Some

applications require finer features on the sides of the trace including the bottom. A very fine topography of the surface can easily be processed and will have some advantages for high frequency circuits, but the lower cost, rougher substrates are more suitable for most applications and can be easily processed as shown here.

Results

The effects of a more efficient HDI technology are sure to trickle down to the entire system. Lighter and smaller devices will use less energy and provide more utility than the heavier and bulkier counter parts. Reduction of layer counts will lead to higher yields and lower material costs in addition to an efficient reduction of the real-estate. Advanced RF products can operate at higher gains and over longer distances.

A-SAP™ results in a process that can be introduced into a shop quickly, though process refinements to achieve the ultimate yield will take a bit longer. The effects will also take time to work into the market place, and be implemented largely with new product introductions. Luckily, new products are being introduced all the time.

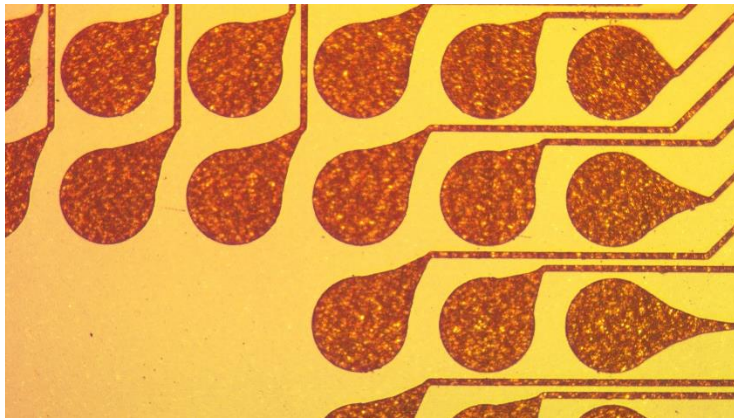


Figure 7- 20 um signal traces for reduced layer count

Conclusion and summary

Subtractive methods where foil is etched away to form circuits are established processes that will continue for quite some time into the future but uses for this technique will be limited in the fast-growing High-Density Interconnect (HDI) market. A new leapfrog technology, A-SAP™, is available to accelerate the adaptation HDI solutions through efficient methods and materials, requiring minimal investment in readily available equipment.

Some markets such as substrates for ICs can tolerate the higher costs typically associated with mSAP. The commercial-volume scale of smartphones and other system level PCB manufacturing is far less forgiving where costs and production efficiencies are concerned.

Acknowledgement

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