Acid Copper Electroplating Processes With Excellent V-Pit Resistance for Flash Etching

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ABSTRACT

Driven by rapid changes and markets, the electronics industry has seen massive growth over the past few decades. The short product life cycle has pushed PCB fabrication technology to its limits. Industry leaders continuously push innovations to be more competitive in the electronics manufacturing market space. In this era of electronics miniaturization, technologies that generate high yields with lower costs, such as High-Density Interconnects (HDI), Semi-Additive Processing (SAP), and Modified Semi-Additive Processing (mSAP), are widely utilized. Most of these technologies are not new to the electronics industry, but are common processes in IC substrate and PCB fabrication. They help maximize the PCB real estate usage by allowing fabricators and designers to build up multilayer devices. Figure 1 shows examples of multilayer designs that require multiple metallization and etching steps to achieve the desired designs and thicknesses.

Etching has become a crucial aspect of PCB fabrication. With the increasing number of layers, the risk of failure grows exponentially. Hence, a great deal of attention has been paid to the Cu deposit and how it reacts to etching. Higher technologies require many etching steps, during which uneven etching, pinhole formation, pitting or V-pitting, become significant issues [1]. These defects can cause severe reliability issues for the final product [2]. Innovative Cu electroplating solutions are required that produce Cu deposits with higher resistance to V-Pitting. Fabricators currently resolve these issues by baking the plated panels for several hours, which increases the process cost and negatively affects production output. The focus of this study was to investigate the underlying mechanism of V-pitting and to develop a process to withstand or resist the pitting. This phenomenon is called “V-piting“ due to the characteristic shape of the pits.

The process discussed here also showed excellent via fill and through hole (TH) plating capability in the same plating bath for core layers of HDI and IC substrates in a one-step DC process. Vias were filled with <5 microns or zero dimple and no voids or defects. Mechanical properties met and exceeded the IPC class III standards thus satisfying the requirements of a highly reliable copper electroplating process (tensile strength => 49,000 psi, elongation > 25%). A bath aging study and a DOE were completed for the process. SEM, XRD, and FIB data will also be presented

KEYWORDS: Flash Etching, V-pit, Reliability, Via Fill, Trough hole, Pattern Plating, Metallization.

INTRODUCTION

Usage of copper as the base metal for circuitry and methods of electroplating it have grown immensely over the last few decades. This is primarily due to several advantages of copper such as its low cost and relatively high electrical and thermal conductivity. Cu electrodeposition is one of the crucial steps in developing a circuit board, as most modern-day advanced board designs consist of intricate current routing networks, including fine line patterns, small vias, and through holes connecting multiple layers. Multilayer PCB construction utilizes technologies like High-Density Interconnects (HDI), Semi-Additive Processing (SAP), and Modified Semi-Additive Processing (mSAP) to achieve desired connectivity and

design. These technologies are essential for consumers to get more and more functionality from their electronic devices, while keeping the device smaller and faster with more components. These processes also offer high yields and competitive costs for manufacturing electronic devices.

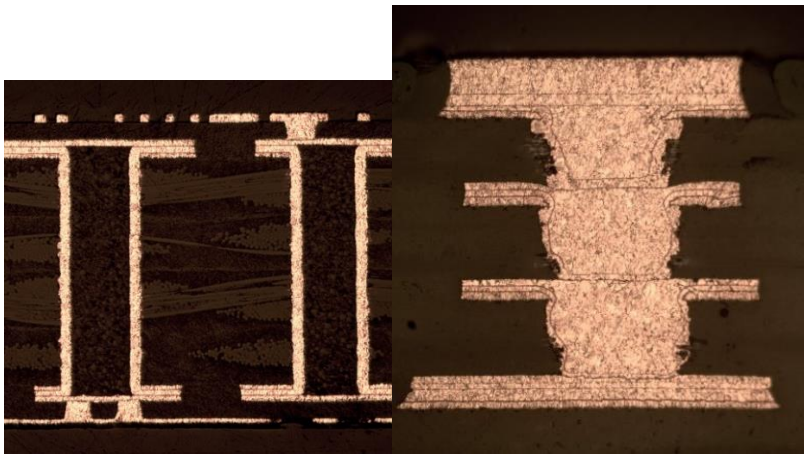


Figure 1. Multilayer buildup. Several processing layers are visible in the cross-section.

However, with these advantages come unique challenges linked to these fabrication technologies. Wet chemical etching, flash etching, or chemical Cu reduction, is a common practice during multilayer PCB fabrication utilizing the afore-mentioned techniques. One of the major issues during the Cu reduction step is uneven etching. Figure 2 shows an example of uneven etching, V-pitting, or pinhole formation during the chemical reduction step. The pits have a distinct "V" shape when they are cross-sectioned, as shown in Figure 2. Therefore, the phenomenon is also known as "V-pitting".

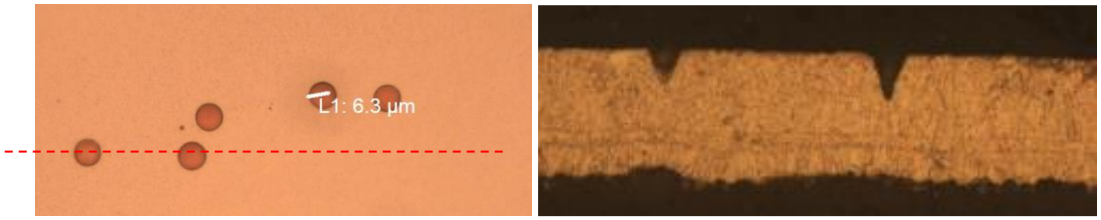


Figure 2. Surface with typical pitting on the surface and a cross-section of the pit showing the characteristic "V" shape.

These pinholes typically have a diameter of 5-10 µm and a depth of 5−10 µm. The formation of these "V-pits" is undesirable for the mechanical/electrical reliability of the Cu interconnects.[2] This is especially the case when the line/space dimensions are brought down to 10 µm. In order to reduce the pits, the plated panels are baked at 100-200° C for 1-3 hours in an oven. This energy intensive baking step is a bottleneck for the manufacturing process and reduces throughput, which makes it a huge hurdle for high volume production. Hence, development of copper plating solutions for advanced electronics manufacturing with deposits that etch evenly and resist pitting without requiring an extra baking step is highly desirable to the industry.

ACID COPPER VIA FILL

Filling small features in PCBs known as "vias" with copper to form connections between layers has become standard practice in the electronics industry. The most economical and practical way to fill these vias is by using acid copper electroplating. These features come in various sizes and shapes, making the filling extremely challenging in some instances. Typical via filling baths have high concentrations of copper (up to 200 - 250 g/L copper sulfate) and lower concentrations of

acid (approximately 50 g/L sulfuric acid) to promote rapid filling of these features. Organic additives are used to control the plating rate and obtain acceptable physical properties. These organic additives must be designed and synthesized carefully to achieve the desired performance. Each plating bath is tailored to the specific application requirements. These requirements are typically sizes of the vias to be filled, acceptable % yield, surface Cu thickness, Cu distribution tolerance throughout the panel, the shape of the via after plating, and the behavior of the deposit upon etching. A typical system will contain 3 organic components: wetter, brightener, and leveler.

Both wetter and leveler are suppressors but they are categorized into two different types, depending on how they interact with the brightener. Type I suppressors, also known as carriers, can be deactivated by the brightener. Type II suppressors, also known as levelers, do not undergo this deactivation. Carriers are usually high molecular weight polyoxyalkyl compounds which get adsorbed on the surface of the cathode and form a thin layer by interacting with chloride ions. [3] This interaction decreases the plating rate by increasing the effective thickness of the diffusion layer, normalizing the energy level over the cathode surface and making the same number of electrons available for plating at any spot on the cathode. [4] This allows the Cu deposit from the bath to become more uniform and evenly distributed. Levelers typically consists of nitrogen-bearing linear/branched polymers, heterocyclic or non-heterocyclic aromatic compounds, being typically quaternized (positively charged). These compounds will adsorb selectively on high current density sites such as edges, corners, local protrusions and prevent copper over plating in high current density areas. [5] Conversely, brighteners, also called grain refiners, increase the plating rate by reducing activation energy and are typically sulfur-containing compounds.

In this study, tests were carried out in an 8-liter cell, and 200-liter pilot tanks. Insoluble anodes were used due to higher current densities, maintenance, and a uniform copper surface distribution. Each bath was made up, dummy plated for 1 Ah/L, analyzed, adjusted to recommended additive levels, and then the test panels were plated. Each test panel went through a pre-clean cycle of 3 min acid cleaner to wet the hole and remove any organic contaminants, 2 min DI H_2O rinse, 1 min 10% sulfuric acid to acidify copper surface prior to plating shown in Figure 3.

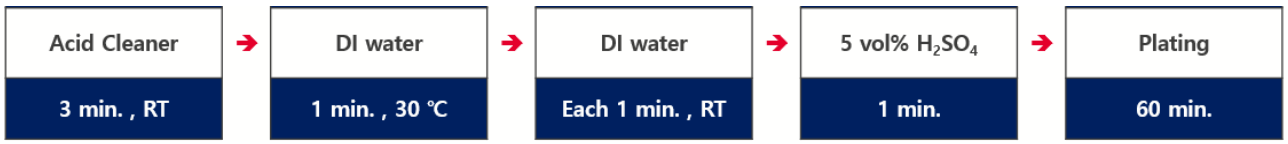


Figure 3. Process flow

CONDITIONS AND BATH COMPONENTS

Table 1 shows the operational conditions and optimum additive levels. Typically, via fill baths have high copper and low acid to achieve the desired bottom-up fill.

Table 1. Bath components and plating conditions

Parameter	Range	Optimum
Anode Current Density	1.0 – 3.5 ASD (10-32 ASF)	2.2 ASD (20 ASF)
Temperature	20 - 27ºC (68 - 80ºF)	23ºC (73ºF)
Wetter	9 - 25 mL/L	10 mL/L
Brightener	0.25 - 1.0 mL/L	0.5 mL/L
Leveler	15– 35 mL/L	25 mL/L
Copper Sulfate ($CuSO_4$.**5** H_2O)	230 - 250 g/L	250 g/L
Free Sulfuric Acid Electronic Grade	45 - 65 g/L	50g/L
Chloride Ion (Cl^-)	40 – 60 ppm	50 ppm

FLASH ETCHING PROCEDURE

A peroxide-based etching solution was used to etch the Cu to the desired thickness. The etching solution was comprised of 10%(V/V) peroxide, 15%(V/V) sulfuric acid, and 4%(V/V) stabilizer. Prior to etching, the solution was heated to 30(±2) °C. Within 15 minutes after plating, flash etching was carried out on the fresh deposit. The etching rate for this solution was ~ 3µm/27 sec. Two samples from the panel were placed in the etching solution for 27 and 54 seconds, respectively, in order to reach 3, and 6 µm of etch depth. Finally, the pieces were dried with air and analyzed immediately under a microscope.

CROSS SECTION ANALYSIS

Sample preparation for the cross-section analysis was started by punching or routing sections from a desired area on the board or test panel. Pre-grinding of the coupon was done to get a flat surface closer to the features. Plastic index pins were used to align the coupon perpendicular to the grinding surface. A fast-cure acrylic resin was used to mount the coupons. A ratio of 1-to-1, hardener-to-resin, was used to provide optimum penetration and a quick cure rate (10-15 minutes). After the sections hardened, they were subjected to grinding, polishing, and microscopic inspection.

TEST VEHICLE

Test panels with different via sizes were used during the evaluation. The thickness of the test vehicles used in the process evaluation was 0.8 mm with via diameter range from 75 – 175 µm, and the via depths 75 and 100 µm. All geometries for each test board thickness were plated at the same time in the same tank and later the fill ratio was calculated by using cross-section analysis. The fill ratio is defined in Equation 1.

$$Fill\ Ratio = \frac{B}{A}\ X\ 100\ \% \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots Eq1$$

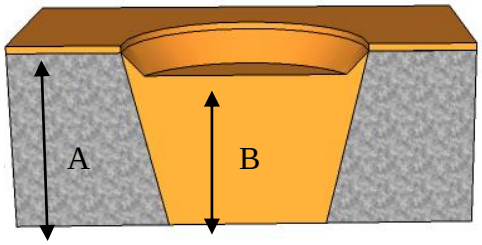


Figure 4. A typical cross-section of a filled via with a dimple, dimple is the fill difference A-B.

The two most important aspects when discussing the TH plating are Microdistribution% and Knee%. The Microdistribution% is defined as the ratio of the average copper deposit thickness in the center of the through-hole to the average copper deposit thickness at the surface. It is calculated according to Equation 2:

$$Microdistribution = \frac{(C+D)/2}{(A+B+E+F)/4}\ x\ 100\% \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots Eq\ 2$$

The Knee% is defined as the ratio of the thickness at the knee and the thickness on the surface and is calculated using Equation 3. This is an essential metric for the formulations capable of filling vias and plating THs at the same time.

Typical via fill baths have a Knee% below 50%. However, this innovative formulation can yield more than 80% Knee% for 4:1 aspect ratio TH while filling a 120x100 µm via with a dimple of less than 5 µm.

$$Knee\ \% = \frac{\left(\frac{C1}{A}\right)+\left(\frac{C2}{B}\right)+\left(\frac{C3}{E}\right)+\left(\frac{C4}{F}\right)}{4} x\ 100\ \% \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots Eq\ 3$$

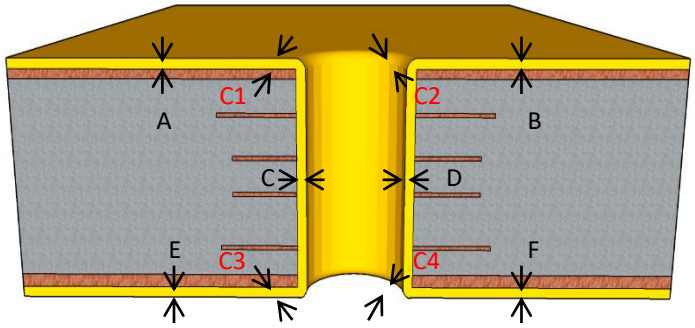


Figure 5. Microdistribution% and Knee%

RESULTS AND DISCUSSION

Initial results showed that the new formulation was a vast improvement over the conventional formulation in terms of pit resistance.

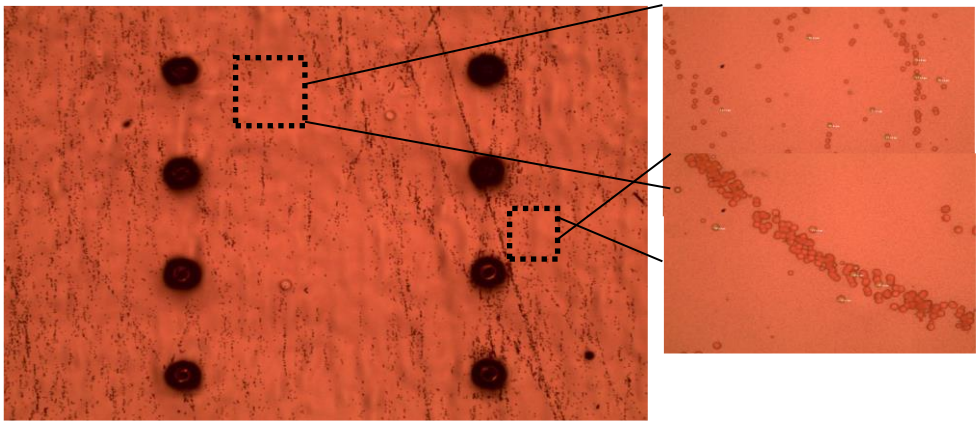


Figure 6. Conventional Cu deposits after 3 µm flash etching. Isolated and bundled V-pits were observed.

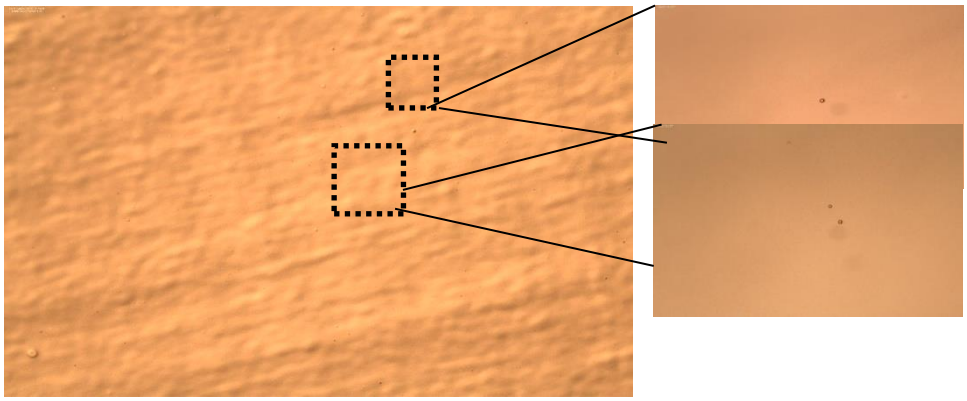


Figure 7. Cu deposit after 3 µm flash etching, electroplated with the new formulation. Hardly any V-pits were observed.

Figures 6 and 7 are a direct comparison of the etching performance of the conventional plating process and the new plating process. Images were taken at 50X and 500X magnification. The small black spots scattered over the area of the plated board are pits after 3 µm of flash etching. The frequency of pits varies over the surface, some areas with isolated pits, and others with clusters of pits. A vast improvement in the pitting performance can easily be seen. Figure 8 shows the via fill and TH performance of the new process.

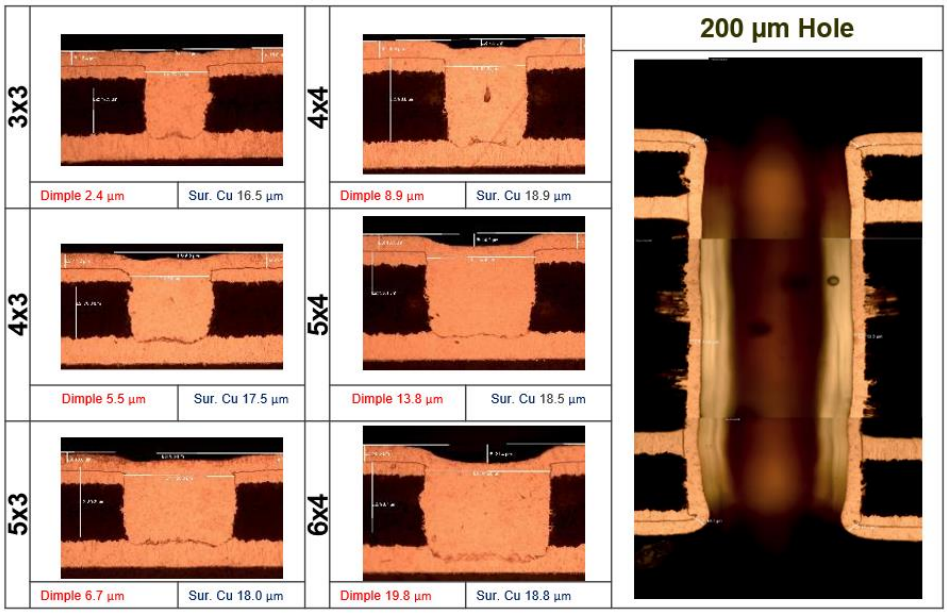


Figure 8. Initial viafill and TH plating performance

DESIGN OF EXPERIMENT(DOE)

Design of Experiment has become a vital step during new process development. A DOE was conducted to further optimize the process and to identify the cross interactions between additives. Stat-Ease® Design-Expert version 10 was used to develop and analyze the data for the DOE. During the DOE, two factors were varied (Brightener and Leveler), while the Wetter was kept constant.

Table 2. Factors and range for DOE.

Factor	Name	Units	Minimum	Maximum
A	Brightener	ml/L	0.25	3
B	Leveler	ml/L	20	50

Table 3. Responses and target for the DOE

Response	Name	Range	Target
R1	Dimple 125 x 75 (µm)	-	<10µm
R2	Dimple 125 X 100 (µm)	-	<10µm
R3	Dimple100 x 100 (µm)	-	<10µm
R4	V-Pit, 3 µm etch	0 to 10 (0 being best)	<4
R5	V-Pit, 6 µm etch	0 to 10 (0 being best)	<4
R6	Surface roughness	0 to 5 (0 being best)	<2

Selected responses in this DOE were Dimple size for 125x75, 125x100, 100x100 µm vias on the samples, V-pitting severity for 3, 6 µm etch depth samples, and surface roughness. V-pitting was evaluated on a scale from 0-10. For reference an incumbent copper deposit from a bath similar to those currently offered in the industry falls in 9-10 range of severity of V-pitting when both 3, and 6 µm etches are applied. The surface roughness was evaluated on a scale from 0-5.

Figure 9 shows the six surface plots that correspond to the six responses mentioned above.

The data showed that the leveler had a large operating window for both dimple and V-pit resistance.

A dimple of less than 10 µm could be obtained with 20-50 mL/L leveler concentration in the bath. However, the brightener required more disciplined control for 0.25 – 1 mL/L in order to achieve less than 10 µm dimple for all the vias. Leveler had a higher impact on the V-pitting and surface roughness than the dimple size. Despite this, the effect of the brightener concentration appears to have the largest impact on the magnitude of the V-pitting and surface roughness.

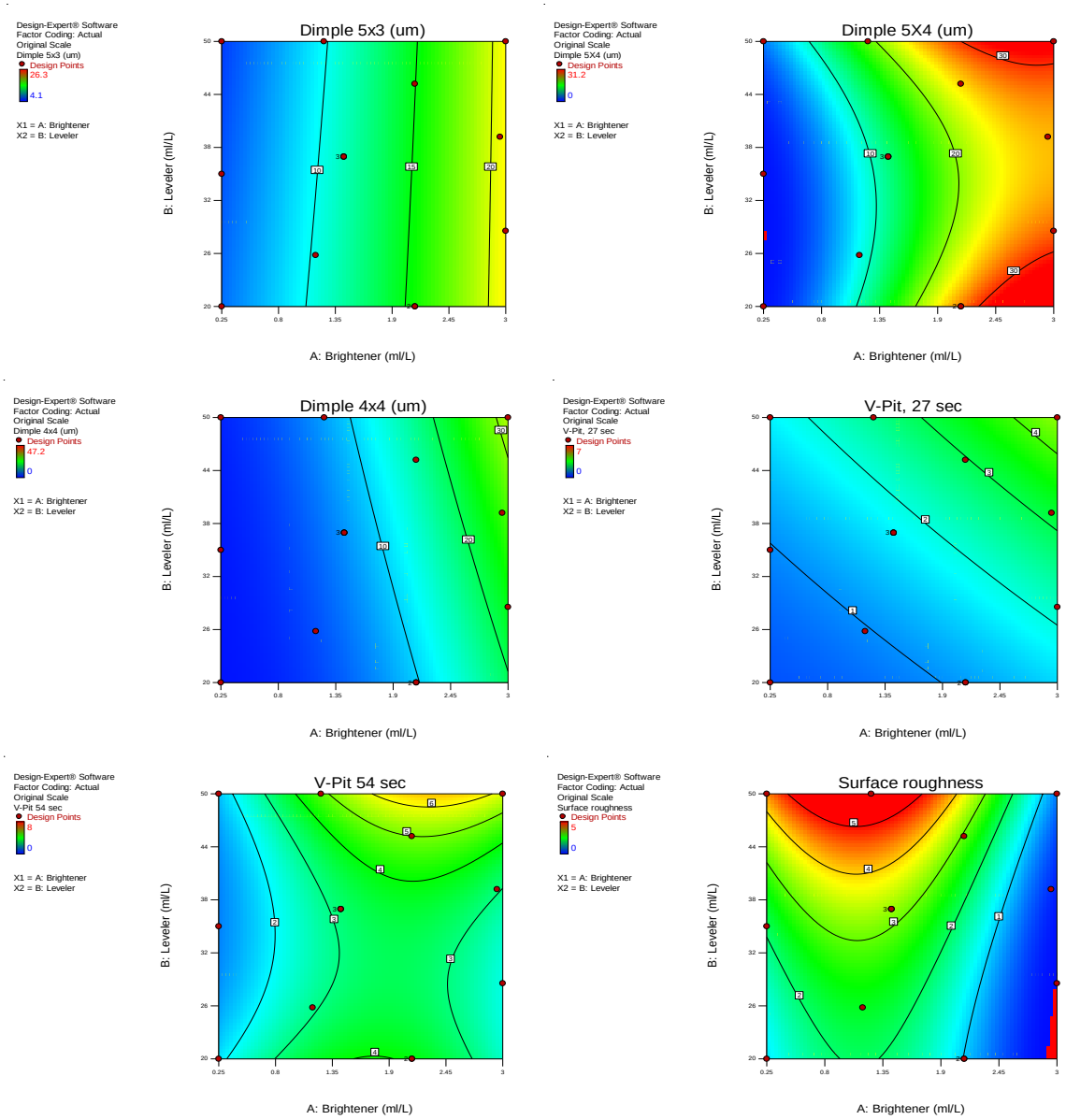


Figure 9. Surface plots for different interactions of leveler and brightener.

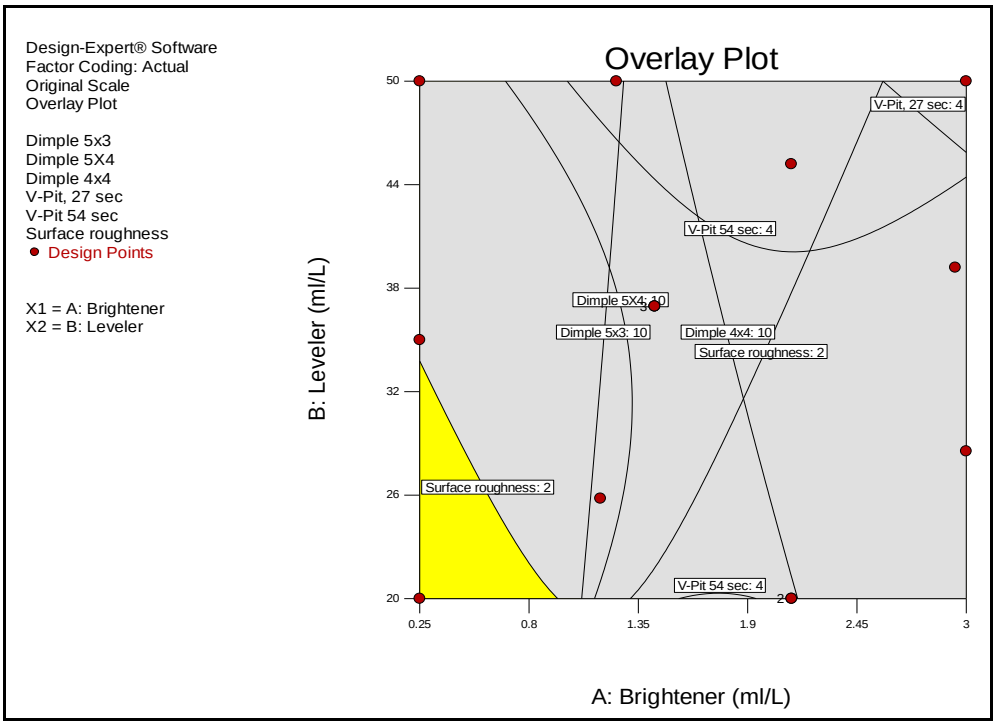
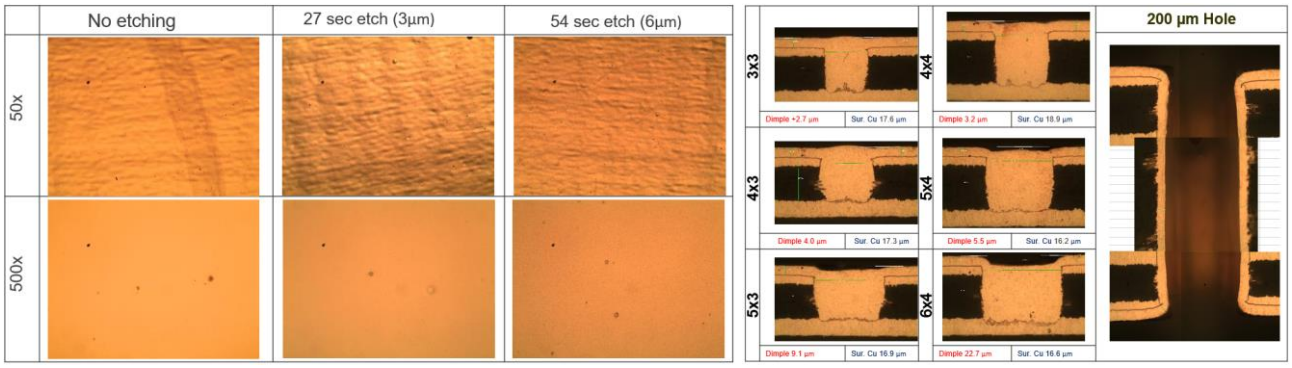


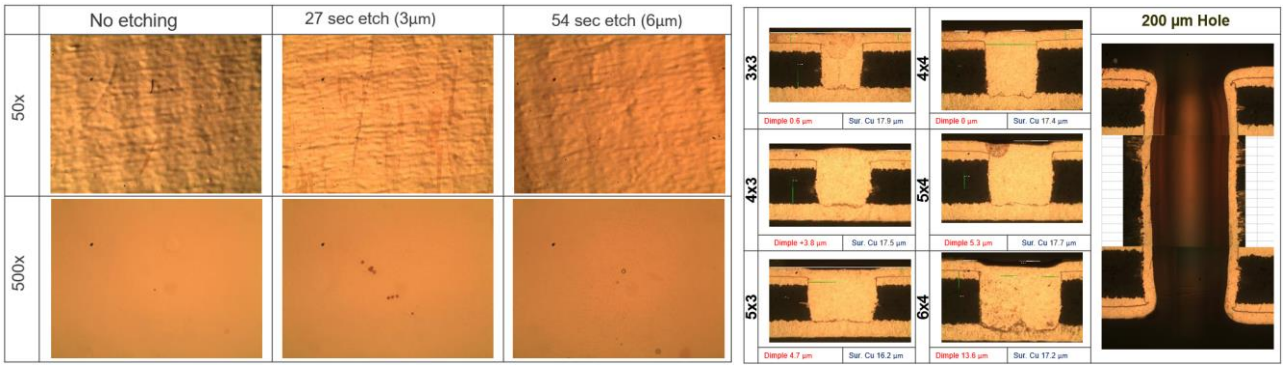
Figure 10. Overlay plot for the optimized additive range.

The results for combined responses are shown in the overlay plot in Figure 10, where the optimum operating window for the process is shown in yellow. Two confirmation experiments were carried out as shown in Figure 11. Results show condition 2, derived from the DOE, had the best via fill performance and lowest magnitude of V-pitting. Optimized conditions gave much better via fill performance and V-pit resistance over the initial test results. TH plating was not significantly affected and in all cases, both Microdistribution% and Knee% were above 80%.

	BRIGHTENER	LEVELER	WETTER
CONDITION 1	0.25 mL/L	20 mL/L	10 mL/L
CONDITION 2	0.5 mL/L	25 mL/L	10 mL/L



Condition 1: brightener = 0.25mL/L, leveler = 20.0mL/L, wetter = 10mL/L



Condtion 2: brightener = 0.50mL/L, leveler = 25.0mL/L, wetter = 10mL/L

Figure 11. Results for two confirmation tests derived from the DOE

BATH AGING AND V-PIT PERFORMANCE

Since this is a novel formulation, it was essential to evaluate the stability of the additives under real plating conditions. Therefore, a bath aging test was carried out in which samples were plated to assess pitting during flash etch every 50 Ah/L up to 150 Ah/L. Before each plating, the bath was analyzed for all the organic and inorganic components and adjusted as needed. Flash etching was carried out using the same procedure specified above. Figure 12 shows the results of the aging study. Each panel was evaluated under the microscope at 50X and 500X magnifications before and after etching. As mentioned above, the two etching levels evaluated were 3 and 6 µm.

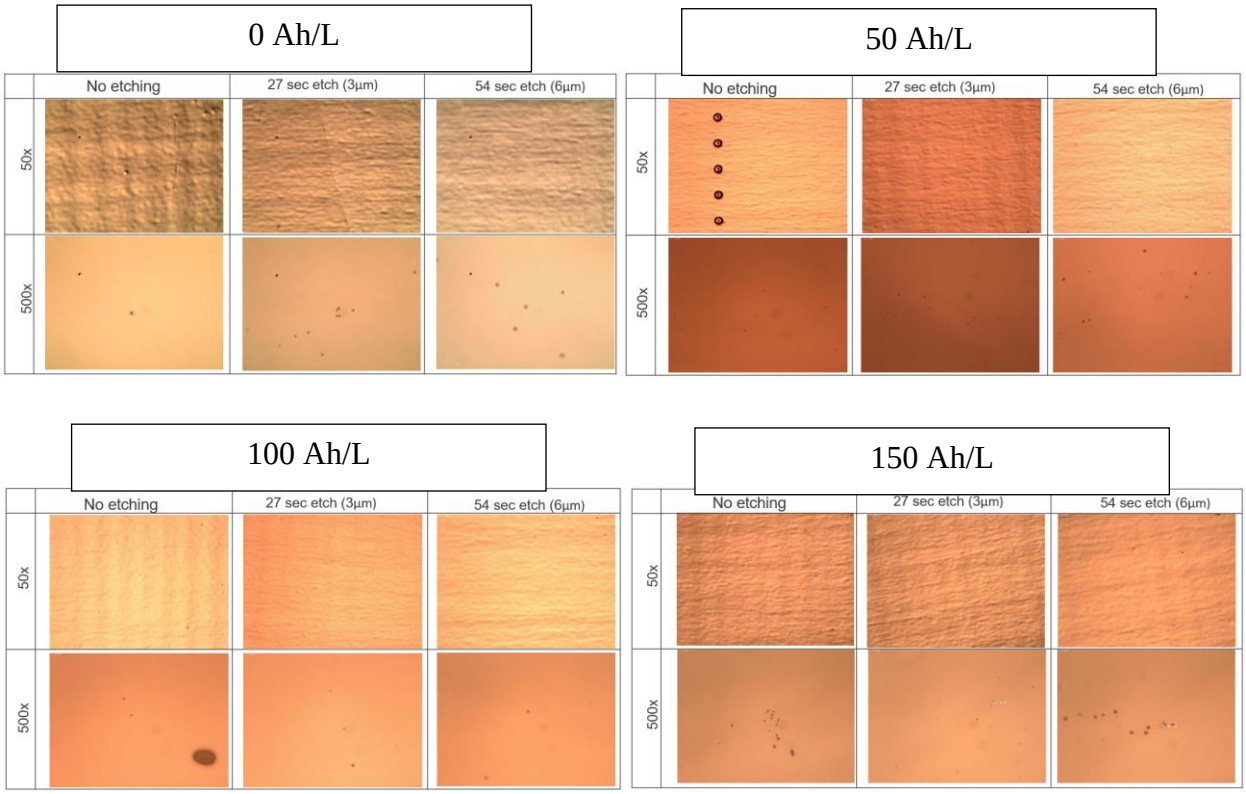


Figure 12. Bath aging vs pitting performance

The data showed that the bath performance was stable during aging. A significant improvement in surface uniformity was achieved over the conventional bath. Additionally, analytical techniques for evaluating organic additives by the Cyclic Voltammetric Stripping (CVS) method were able to accurately control the additives during the bath aging.

PHYSICAL AND THERMAL PROPERTIES

The two most important physical properties to PCB manufacturing are tensile strength and elongation%. These properties correlate to the deposit's thermal stress tolerance. The organic additives (suppressor, grain refiner, and leveler) will affect these characteristic physical properties.

$$\textit{Mean average cross sectional area } (in2) = \frac{\textit{Weight of the sample } (lbs)}{\textit{Length of tensile sample } (in) x \textit{ density of copper } (g/in3)} \quad \ldots\ldots\ldots \textit{Eq 4}$$

$$\textit{Tensile Strength} = \frac{\textit{Maximum load } (lbs)}{\textit{Mean cross sectional area } (in2)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \textit{Eq 5}$$

$$\textit{Elongation} = \frac{(\textit{Length at break} - \textit{Original gage length})}{\textit{Original gage length}} x\,100\% \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \textit{Eq 6}$$

Tensile strength and elongation were measured according to the IPC TM-650, 2.4.18.1 test method. A stainless-steel panel was plated with copper from the formulation. Sample strips were removed from the plated panel and baked in an oven at 125 °C for four to six hours. An Instron instrument was used to test the strips. The measurements were used to calculate tensile strength and elongation % using Equations 4, 5, and 6.

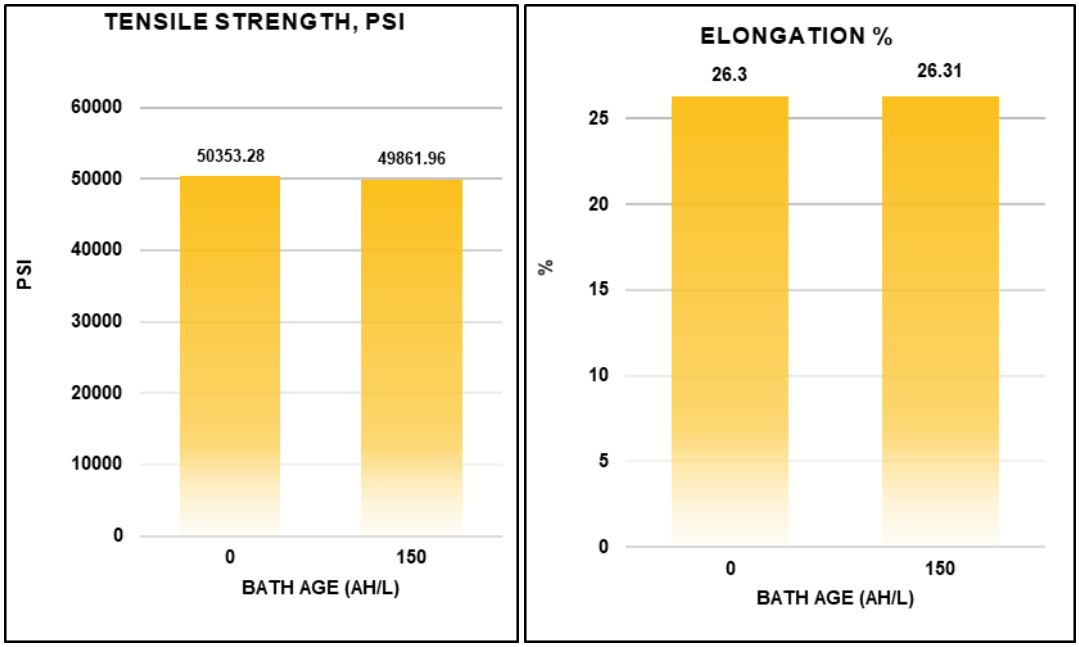


Figure 13. Physical properties of the deposit.

Tensile strength and elongation % of the bath were also measured during the aging study. Once before aging, when the bath was fresh, and once after aging was complete at 150 Ah/L.

Figure 13 compares the initial and 150 Ah/L tensile and elongation data. The bath showed stable performance during the aging test and surpassed IPC class III requirements (Tensile strength > 36000 psi, and Elongation > 18%) for both tensile strength and elongation%.

X-Ray Diffraction (XRD) and grain structure evaluation was performed for the plated deposits to identify the crystal phase and different planes. The typical diffraction pattern was obtained as the standard reported in the literature (Figure 13), with reflections from planes (111), (200), (220), and (311) observed. [5] Narrow sharp peaks in the XRD pattern were observed, which indicates highly ordered Cu crystals in the deposit. The focused ion beam (FIB) study showed the general grain structure of the deposit and show equiaxial grain structure without any preferred orientation.

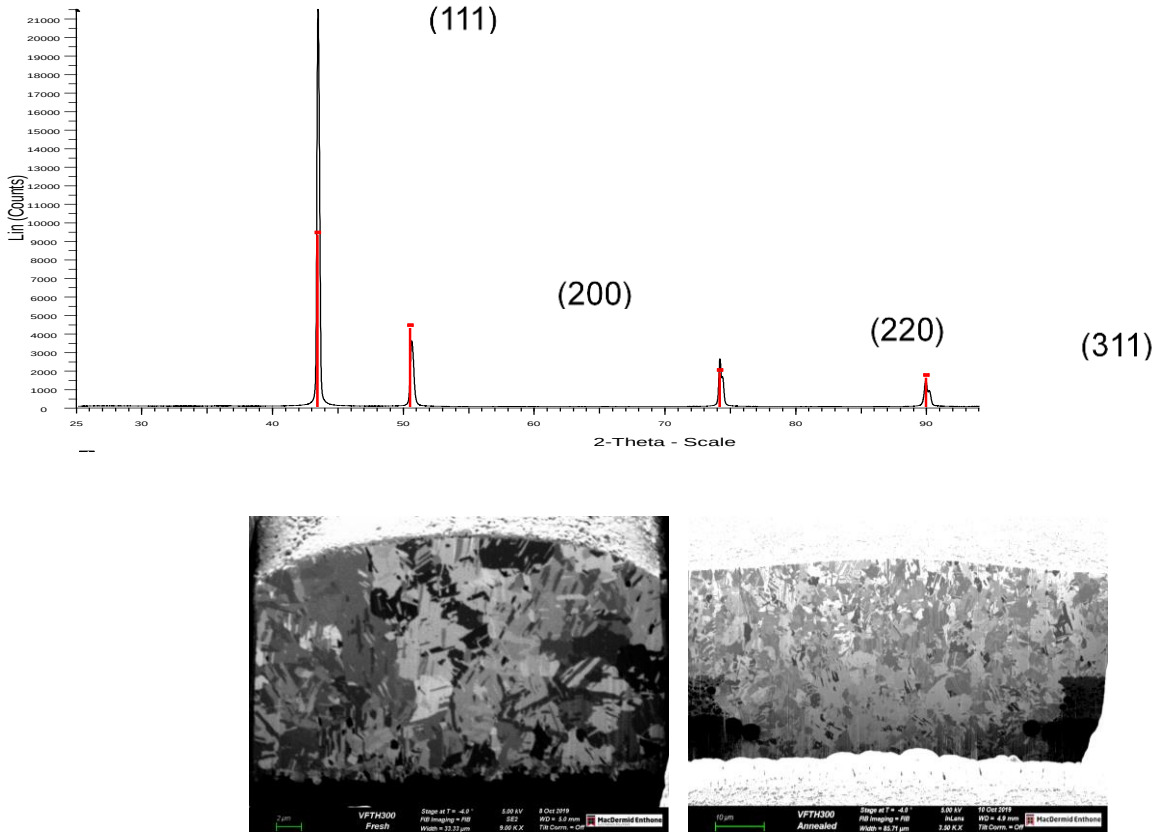


Figure 13. X Ray Diffraction (XRD), and grain structure

CONCLUSION

An innovative DC acid copper process for simultaneously filling vias and plating through-holes is introduced in this work. This new formulation shows excellent V-pit resistance during subsequent flash etching processes. A wide variety of via geometries can be filled with minimal dimple while maintaining excellent through hole plating performance. A DOE was conducted to further optimize the performance. Through varying the leveler and brightener concentrations, the DOE identified these two components as major contributors to the desired deposit properties. The tensile strength and elongation of these Cu deposits remained consistent as the bath aged and passed IPC Class III. All the additive components utilized in these processes can be analyzed with common analytical tools used in the industry

REFERENCES

[1] Chang-Chih Chen, Cheng-Hui Hsieh, Yu-Wei Lee, Cheng-Hsien Yang, Cheng-En Ho, the Formation mechanism of pinholes in electroplated Cu films and its mitigation, *Thin Solid Films* Volume 596, 1 December 2015, Pages 209-215

[2] Hsuan Lee, Chih-Ming Chen. Impurity Effects in Electroplated-Copper Solder Joints *Metals* 2018, *8*(6), 388;

[3] P.Broekman, A.Fluegel, C.Emnet, M.Arnold, C.Roeger-Goepfert, A.Wagner, N.T.M.Hai, D.Mayer, Classification of suppressor additives based on synergistic and antagonistic ensemble effects. Electrochimica Acta, Volume 56, Issue 13, 1 May 2011, Pages 4724-4734

[4] K. B. Herbert; S. Adhikari; J. E. Houser, Journal of the Electrochemical Society, 152 (5) C324-C329, 2005.

[5] S. Dharmarathna et. al. High Throw DC Acid Copper Formulation for Vertical Continuous Electroplating Processes. IPC APEX Expo 2017, San Diego, California, February 14-16, 2017.