3D Aerosol Jet Printed Interconnects on Bare Die

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ABSTRACT
Aerosol Jet [AJ] Printing can provide many enhancements over traditional bare die attachment techniques. Previous studies have shown [1] that that AJ technology offers advantages in the millimeter wave frequency range, such as a significant reduction of insertion loss and the ability to design the line impedance as required.

As more designs venture into the mm-Wave/5G frequencies and higher ranges [2], board real-estate will become a premium. Printed electronics can help alleviate this problem by allowing for bare die to be used instead of standard packaged components. By utilizing printed electronics to form the connection between bare dies and CCA an increase in space of up to 40% can be achieved. For this project the team of Lockheed Martin, Binghamton University, and Optomec worked together to assembly bare die RF beamformer assembly and provided interconnects to the underlying substrate. This report provides an overview of the reason for the printing these interconnects, the overall process of assembling the substrates, the 3D printing of the interconnects, and subsequent testing.

Key words: Aerosol Jet Printing, Conformal, Additive RF

INTRODUCTION
Additive manufacturing (AM) and direct write (DW) printing have seen significant growth in tooling over the past decade, ranging from large prototyping houses to consumer-friendly benchtop models and engineering grade tool sets. These methods enable the production of functional components in a layer-by-layer fashion or with high-resolution material deposition on various surfaces. These methods are particularly appealing because they eliminate the requirement for traditional manufacturing techniques used in radio frequency (RF) circuitry and electronics, enabling direct digital manufacturing of intricate objects without the need for complex tooling.[3][4] One type of printing that has seen increased popularity is Aerosol Jet [AJ] printing. AJ printing is achieved by atomizing a particular material and focusing the material through a narrow nozzle, allowing for deposition onto an underlying substrate. This process allows for fine features on the order of several microns wide (10 microns) and thicknesses down to several nanometers. The ultra fine resolution enabled by this process allows this technology to be a unique candidate for substitution of conventional wire bonding technology. The wire bonding process has been employed for many years but has limits when it comes to higher frequency applications.[3] While challenges in materials and performance still exist [4] the AJ printing process allows for printing of conformal traces and reducing potential issues with parasitic capacitance. Additionally, this project is focused on replacing not only the wire bonding process, but removing the soldering process by bonding the die directly to the underlying substrate and removing the packaged component. By doing this three goals are accomplished:

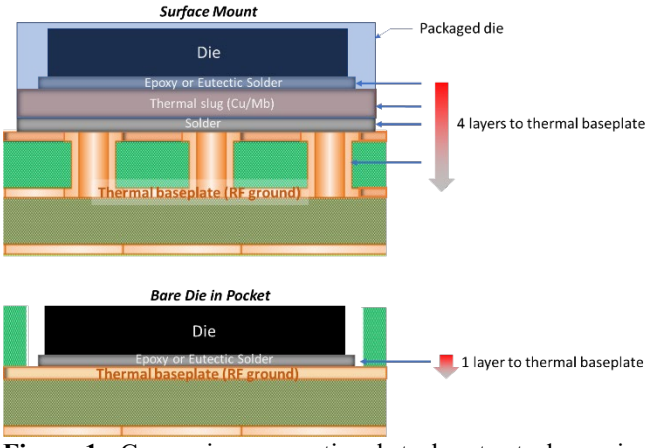


Figure 1 - Comparing conventional stackup to stackup using printed interconnects

Improving the RF performance of the device, by reducing the number of interconnects, eliminating opportunities for loss in the device. (from die to wire bond to substrate to solder interconnect to substrate; to die to AJ interconnect to substrate).

Improved heat dissipation. Heat generation from RF components, in particular amplifiers are a concern as higher frequencies require higher amplification of signals which leads to high temperature performance requirements. Reducing the layers required to get to the heat spreading source as shown in **Figure 1**, thermal improvement can be achieved.

Improved board real-estate. As frequencies increase, the spacing between antenna elements decreases, which further reduces the spacing between channels on a RF circuit design. This issue is further exasperated by the ever-increasing performance required of future RF systems. Conventionally packaged devices such as QFNs will be limited on higher frequency designs due to their size. Bare die components will allow for greater circuit density, provided we can create a reliable interconnect between chip and substrate.

There has been significant research into this AJ printing for RF performance improvements. Recent studies have demonstrated the ability to print interconnects in lieu of wire bonds for several PIN diode components whereas a device was placed into a pocket on a liquid crystal polymer (LCP) substrate, dielectric material was deposited into the pocket to provide a bridge to the conductive pin, and a conductive trace was printed, connecting the substrate to the diode.[2]

Additionally, other projects with NextFlex have demonstrated the repeatability and reliability of printing RF traces in the form of co-planar wave guides. These devices demonstrated consistent performance up to 20 GHz, even after thermal cycling from -40C to 125C for 500 cycles (**Figure 2**).

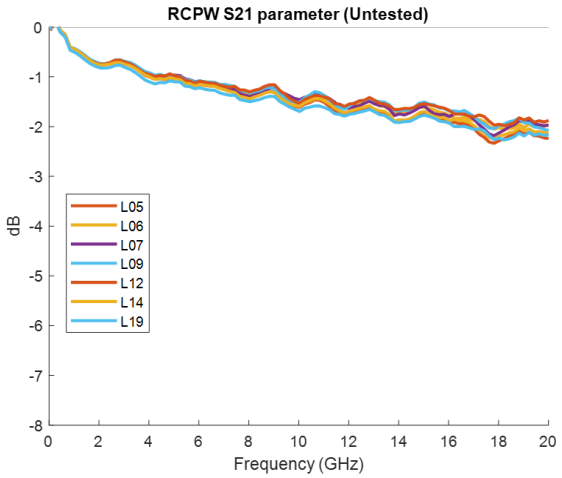


Figure 2 – S21 curve for printed coplanar waveguide traces

In this paper, we aim to build upon years of development and adapt our findings to a practical use case: a Radio Frequency (RF) chain. This RF chain will demonstrate the feasibility of implementing additive interconnects. The process of realizing this goal involves several key steps, which will be explored in detail throughout this paper. These steps include selecting and attaching the dies, choosing suitable materials, designing the RF, printing the components, conducting RF testing, and performing failure analysis.

A critical aspect of our investigation involves comparing RF test results of the printed interconnect die to those of a conventional packaged device. This comparison serves to highlight the advantages and potential improvements offered by the new approach, providing valuable insights for future RF designs. By examining these key areas. Our goal is to present a comprehensive analysis of the whole process, identifying the potential benefits and challenges of this innovative approach.

TEST METHODOLOGY

In our study we evaluated several UV-cured epoxies and urethanes, along with various cures profiles (see **Figure 3** and **Figure 4**). [3] Our primary objective was to identify a material with a dielectric constant (Dk) of approximately 3, which would be comparable to the underlying substrate's Dk. Among the materials assessed, Epoxy EMI3554 (yellow) demonstrated the most promising results, exhibiting a Dk of around 3 across the preferred frequency range. Moreover, it maintained a consistent loss tangent (Df) of approximately 0.07 throughout the specified frequency range which is considered adequate for a RF friendly material.

Given the stability of the process variables observed, we elected to utilize the UV-cure process for this project. This choice is primarily driven by its in-situ curing capability, which allows for controlled ramp buildup, thereby ensuring optimal results and alignment with our project objectives.

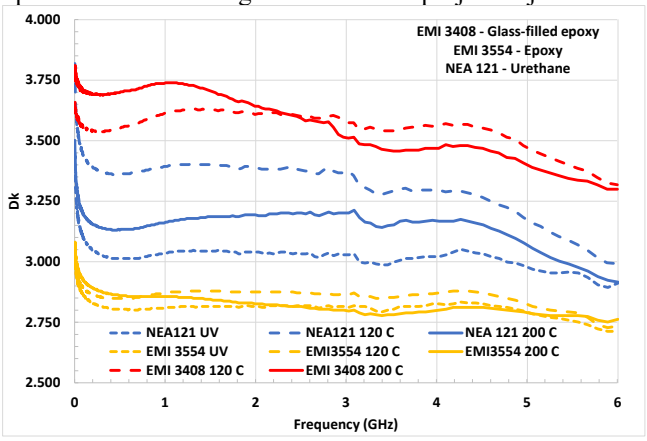


Figure 3 – Dk of several dielectric materials using different curing processes

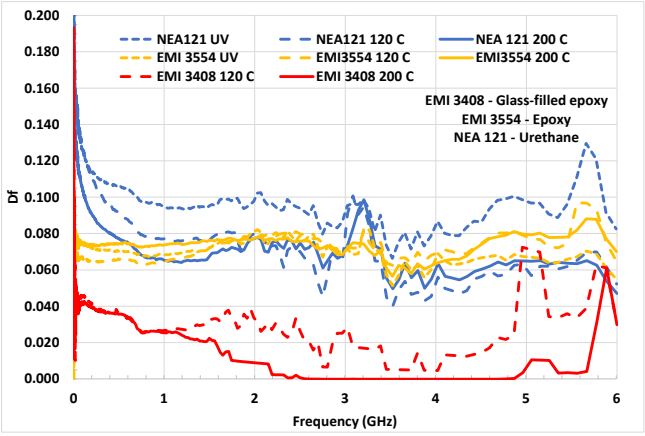


Figure 4 – Df of several dielectric materials using different curing processes

For this project an RF chain was designed for both receive and transmit signals, as shown in **Figure 5**. The transmit (TX) path, highlighted by the red arrows, consists of two switches and an amplifier. The receive (RX) path, represented by the green signal, follows a more simplified route, bypassing the amplifier and passing through both switches. To assess the RF performance of the device, an RF connector can be attached to each end of the RF chain. This configuration enables accurate measurement of the signal quality and performance, providing valuable insights for further optimization and development.

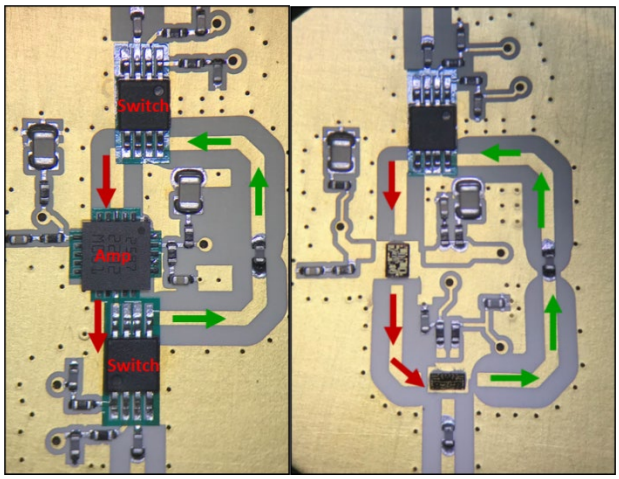


Figure 5 – SMT RF channel showing the path for Transmit (Red arrows) and Receive (Green arrows)

Figure 6 – Bare Die RF channel showing the path for Transmit (Red arrows) and Receive (Green arrows)

For this test design an additional RF channel was added to the test board only this time an amplifier and switch were removed and replaced with their die alternative. This design is shown in **Figure 6** once again using the red (Transmit) and green (Receive) arrows to indicate the different RF paths. To provide a similar comparison and limit design changes nothing else was changed in the overall design although the spacing could have been reduced.

Also as shown **Figure 7** the channels were placed adjacent to one another to limit any undesired differences in board fabrication.

The amplifier chosen was a 2-6 Ghz Gallium Nitride (GaN) driver amplifier **(Figure 7**) and a Gallium Arsenide (GaAs) Monolithic Microwave Integrated Circuit (MMIC) rated up to 20 GHz (**Figure 7**).

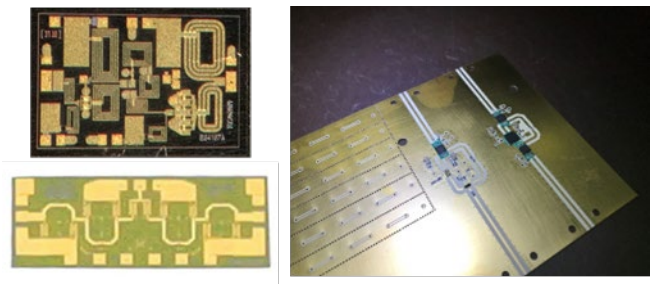


Figure 7 – (L) RF Circuit Test Vehicle (R) Amplifier and Switch Die

These devices were selected for their electrical properties and most importantly availability of standard package and bare die versions of each part. To better understand the size difference between the bare die and packaged devices the second switch in RF circuit is the same part as the bare die mixer just without the additional packaging.

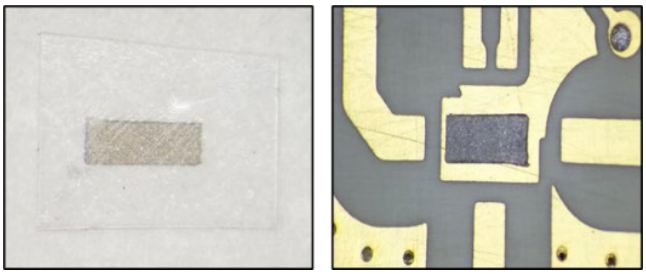


Figure 8 – (L) Precut film adhesive with backer (R) Film adhesive after being applied to the substrate

During our investigation, we evaluated various attachment options for securing the bare die to the heat spreader. We initially considered a reflow process, which would have provided a robust fillet, but raised concerns regarding potential damage to the die during placement and reflow, as well as the possibility of the die shifting during the reflow process. Another option we explored was the use of liquid epoxy; however, similar concerns regarding shifting of the device and consistent bond line thickness led us to abandon this approach.

Ultimately, we opted for a pre-cut film adhesive, owing to its ability to provide a consistent bond line thickness, minimize shifting, and ensure a repeatable and inspectable amount of material. To attach the die, we utilized a pre-cut conductive film adhesive with a b-stage cure process. The substrate was

pre-heated to 70°C, followed by placement of the film adhesive on the substrate using a double-sided adhesive as a backer, as depicted in **Figure 8**. The substrate was then cooled, enabling the removal of the backer. Subsequently, the substrate was reheated to 70°C, and the die was carefully placed into the film adhesive.

Following a cooling period, both dies were inspected before proceeding to the final cure step. The substrate was then enclosed in a vacuum bag for uniform pressure and cured at 125°C for 2 hours. Post-cure evaluation revealed a uniform bond line, which will be further confirmed with cross-section analysis. Most significantly, no damage was incurred to the devices themselves. **Figure 9** shows the bonded die prior to AJ printing.

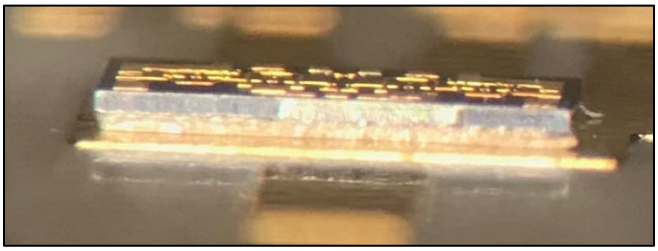


Figure 8 – Image of Switch attached to substrate

PRINTING STEPS

Fabrication of the printed interconnects involves two steps: dielectric ramp printing and conductive element printing. In the dielectric ramp printing stage, the EMIUV material is carefully AJ printed at a rate of about 1mm^3/min using a pneumatic atomizer. The material is printed in layers, followed by routine curing with UV light as the ramp is constructed. This ramp serves two critical functions: first, it facilitates the pathway for the conductive trace, and second, it prevents any unwanted shorting between the interconnect and nearby ground. As depicted in **Figure 10**, the dielectric material effectively creates a ramp to the top of the switch, simultaneously providing isolation from the ground situated beneath the device.

It is crucial to avoid overprinting of the dielectric, as this could lead to the covering of contact pads, ultimately resulting in poor connections. The dielectric ramp's precise design and execution ensure optimal performance of the conductive trace and reliable electrical connections, contributing to the overall functionality and success of the printed interconnects.

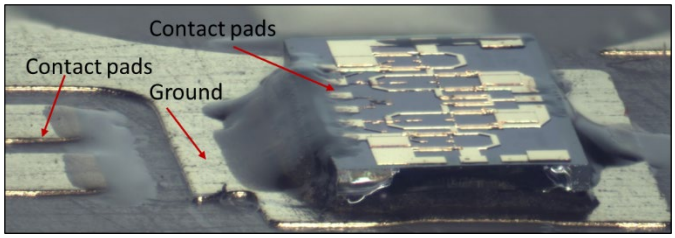


Figure 9 – Dielectric printed ramps on switch

Other examples of the dielectric ramp on the amplifier are shown in **Figure 11**.

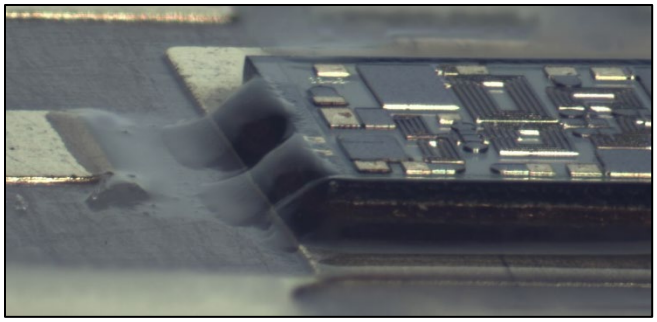


Figure 10 – Dielectric printed ramps on amplifier

Ramps were applied to all sides of the devices. It is important for these ramps to be smooth and gradual when transitioning from different surfaces, avoiding any possible stress concentrations.

A silver ink was utilized for printing the traces. These traces were also printed using a pneumatic atomizer and deposited at a rate of slightly under 1mm^3/mn. The speed of the printing is 10mm/s. After printing the substrate is cured at 150°C for a duration of 1 hour. Magnified views of the switch can be found in **Figure 12**. In total, seven connections were established. The conductive traces were printed in a triangular pattern, optimizing contact points on the substrate and providing a gradual change in the size of the interconnect. For size reference, 0402 chips are visible in the photograph.

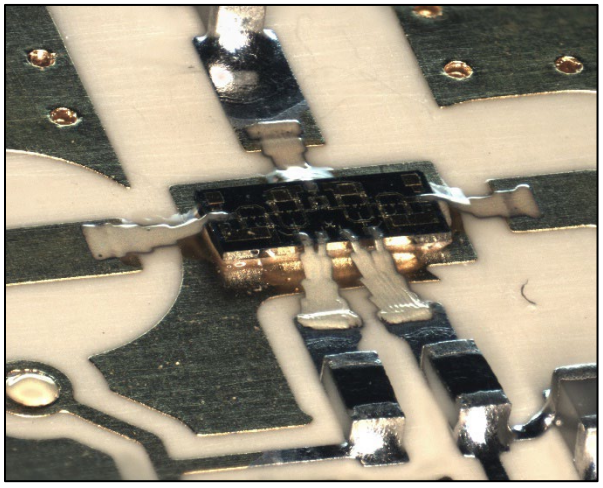


Figure 11 – Printed Ramps and Interconnects on switch

The amplifier is shown in **Figure 13**. Six connections were made on this device although some shared a common end point.

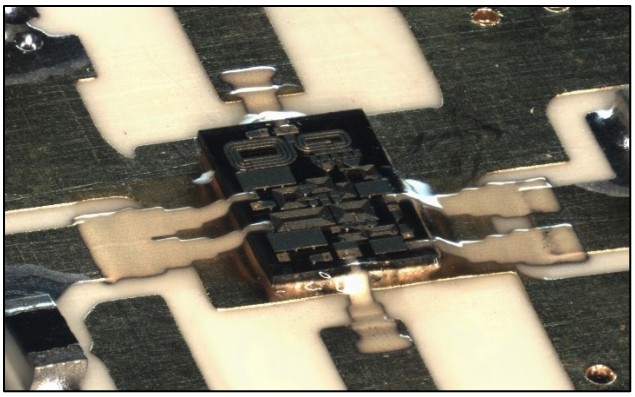


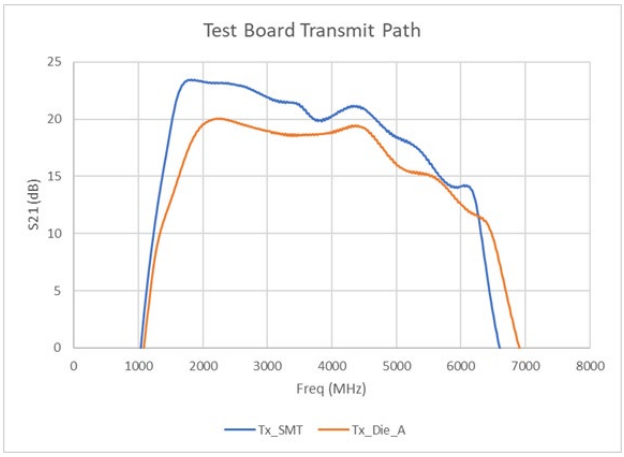
Figure 12 – Printed Ramps and Interconnects on amplifier

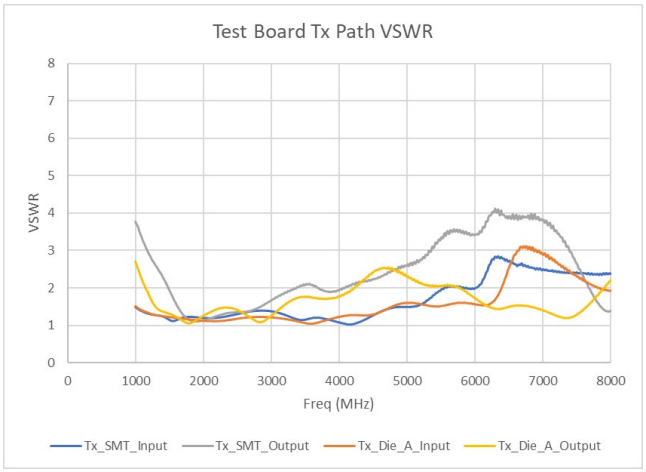
TEST RESULTS

The completed device underwent RF testing in the frequency range of 2-6 GHz, with the Surface Mount Technology (SMT) version also tested for comparison purposes. The results for the transmit path, which includes the amplifier, are displayed in **Figure 14**. Both the SMT and printed devices demonstrated comparable performance across the entire frequency range.

The Voltage Standing Wave Ratio (VSWR) for the transmit path is presented in **Figure 14**. The VSWR of the printed interconnect appeared slightly better in comparison to the SMT device [Note: Optimal VSWR is 1]. However, the Receive (Rx) path, which is significantly less complex and consists of only one printed trace that isn't shared with the Transmit (Tx) path, exhibited a significant difference of approximately 10dB between the SMT and printed channels.

Despite the reduced performance in the Rx path, the device remains functional, indicating that the printed interconnect is operational. Upon initial examination, no issues, such as cracked traces, were identified. Therefore, a cross-sectional analysis of the device was deemed necessary.





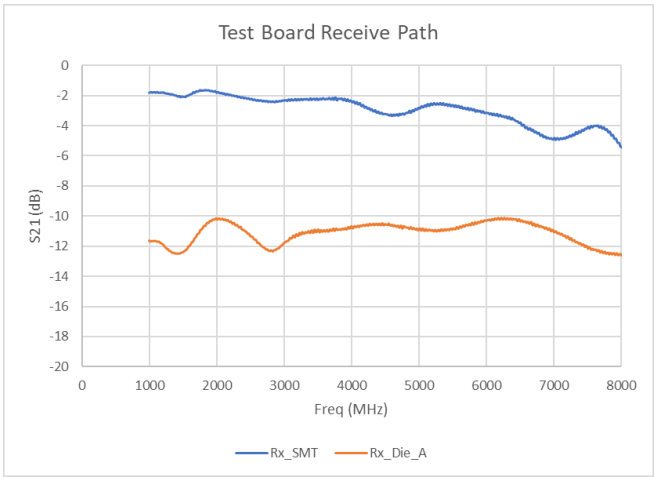


Figure 13 – RF test data showing S21 Transmit data from 2-6GHz, Transmit VSWR Data, and S21 Receive data from 2-6 GHz for both SMT and Printed RF Channels

CROSS SECTION RESULTS

To investigate the potential causes of the -10dB loss observed in the Receive (Rx) testing, a cross-section analysis was carried out on the switch. An issue was immediately noticed during the examination, as depicted in **Figure 15**. Specifically, multiple ground vias anomalies were identified

directly beneath the switch, with several of them appearing miss-drilled and not fully formed. This deficiency in via formation likely contributed to the suboptimal results observed in the Rx testing.

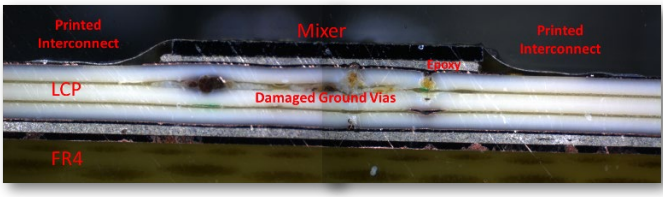


Figure 14 – Cross Section of Switch showing damage ground vias internal to substrate

Additional observations made during the cross-section analysis included an even and consistent appearance of the epoxy beneath the component and an intact switch. A closer inspection of the printed interconnects is presented in **Figure 16** and **Figure 17**, revealing their intact nature, smooth transitions, and a consistent thickness ranging from .0002" to .0003".

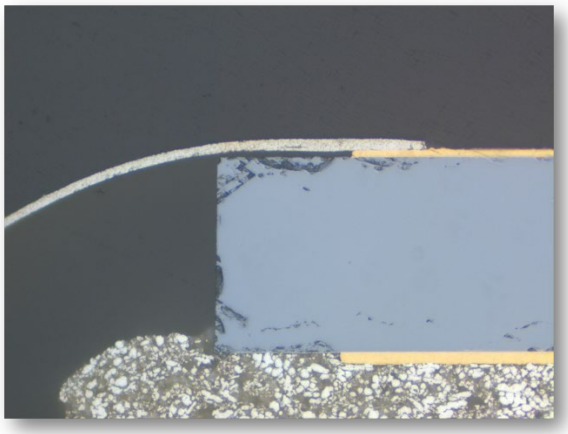


Figure 15 – 50x Magnified view of printed interconnect on switch

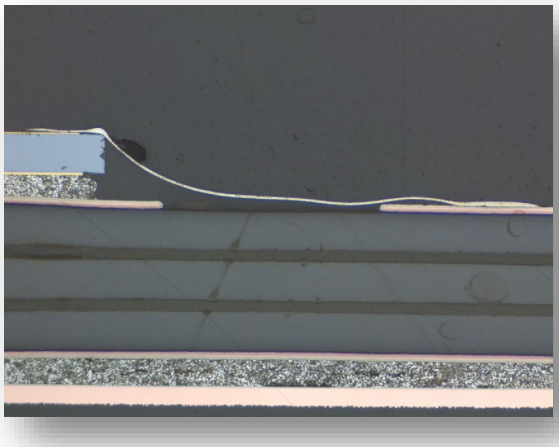


Figure 16 – 10x Magnified view of printed interconnect on switch

CONCLUSIONS

The process for printing interconnects to a bare die has been demonstrated, but there is still more work to be done to optimize the process. The RF results showed comparable performance to a packaged device, but the goal is to see results that show better performance than the packaged device. Unfortunately, failure analysis revealed that ground vias likely caused a 10 dB drop, and an issue with the substrate fabrication affected the receive (Rx) path. Despite these challenges, process parameters will be leveraged to produce a full up phased array.

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