

# THREE DIMENSIONAL INTEGRATION RESEARCH FOCUSING ON DEVICE EMBEDDED SUBSTRATE

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## ABSTRACT

The national research project on 3D integration technology had been carried on in Fukuoka, Japan from 2002 to 2012. The system-in-a-package (SiP) design tools STEERSIP and STEERMEMS, test element group (TEG) chips for evaluating the assembling process, and the evaluation equipment such as scanning electron and laser beams induced current (SELBIC) measurement system have been developed. In 2011, a new research center for 3D semiconductors was constructed, where the main research is on device embedded substrate and silicon interposer with through silicon via (TSV). According to the Japan Electronics Packaging and Circuits Association (JPCA) standard on device embedded substrate EB01 and EB02, the evaluation kits for device embedded substrate are developed in order for device companies to perform function test of embedded devices with the common substrate structure.

## INTRODUCTION

Device embedded substrates is believed to be a key technology for 3D integration as well as TSV technology[1]. Active and passive devices are embedded inside the substrate during the PCB process and connected three dimensionally. Then surface patterns are formed, and devices are mounted on the surface.

The national research project on system integration platform had been carried on from 2002 to 2012 in Fukuoka, Japan. There had been three main fields; one is to develop 3D system-in-a-package (SiP) EDA tool. The other was to develop test element group (TEG) chips and reference substrate (RS) for evaluating assembling process, and to develop evaluation equipment. EDA tools named STEERSIP and STEERMEMS were developed, and are now commercially available in Japan. TEG chips specially designed for assembling process have been used by many Japanese companies. In March, 2011, a new research center for 3D semiconductors was constructed in Fukuoka.

On the other hand, the Japan Institute of Electronics Packaging (JIEP) organized a technical meeting named Embedded Passive and Active Devices (EPADs) in April,

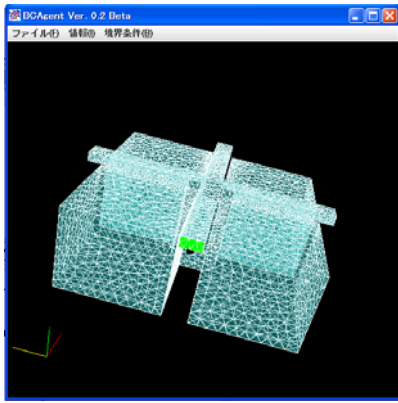
2007, and the academic discussion on the embedding technology started in Japan. Then the Japan Electronics Packaging and Circuits Association (JPCA) organized the standard committee on device embedded substrate in March, 2008. In June, 2008, the first standard on device embedded substrate EB01 (Edition 1) was published, and since then every year EB01 has been revised, and EB01 (Edition 5) was published in June, 2012[2]. In the standard, TEG chips developed in Fukuoka are used for reliability test. In terms of design format, JPCA published EB02 (Edition 1) in November, 2011[3],[4]. Currently EB02 is available by three CAD vender tools in Japan[5].

In this paper, EDA tools, TEG chips, and several evaluation equipment developed in Fukuoka are explained. The evaluation kits for device embedded substrate developed at the research center and the collaboration with JPCA on the evaluation method are also explained.

## EDA TOOLS

In order to design 3D SiP structure, not only the electrical connection but also thermal analysis and electromagnetic analysis are needed and the co-design is important to shorten the development time. The fully 3D EDA tool named STEERSIP was developed. It has the interface to IcePAK for thermal analysis, and the interface to HFSS for electromagnetic analysis. The feedback of simulated data to STEERSIP is possible, making co-design system.

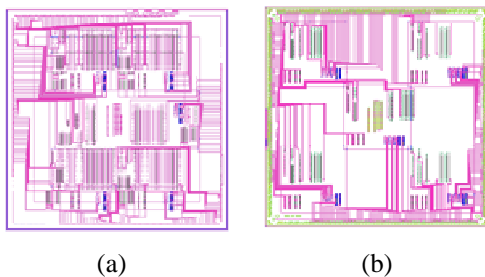
For micro-electromechanical systems (MEMS) device SiP, the stress analysis software ADVENTURE Cluster are added to STEERSIP, and finally MEMS/SiP tool named STEERMEMS are developed. Figure 1 shows the stress analysis of 3D acceleration device with STEERMEMS.



**Figure 1.** Stress analysis of 3D acceleration device

### TEG CHIPS

In order to evaluate the assembling process such as dicing, bonding, and molding, TEG chips are used commonly. Figure 2 shows the TEG chips with low-k insulating layer. Since the low-k materials are fragile against the mechanical stress, defects are introduced sometimes during assembling processes such as dicing and bonding, and molding. The assembling process is evaluated from the change in capacitance and resistance. There are several capacitors near the dicing street, for example. If the low-k layer is damaged by the dicing, the change in capacitance must be measured. TEG wafers are 300 mm in diameter, and fabricated by 90 nm and 130 nm process.



**Figure 2.** Low-k TEG chips with 90nm node (a) and 130 nm node (b) for evaluating the assembling process

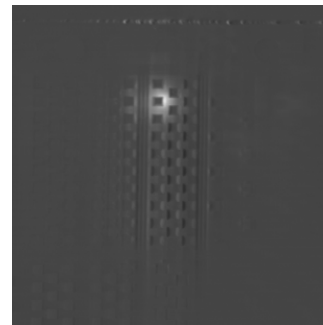
### EVALUATION EQUIPMENT

Figure 3 shows the scanning electron and laser beams induced current (SELBIC) measurement system[6]. Both of electron and infrared laser beams irradiate the sample at the same time from both sides of the sample, and can be scanned. The cold cathode field emission gun and laser sources with two wavelengths of 1064 nm (YAG laser) and 1400 nm (laser diode) are installed coaxially, and the vacuum chamber is sandwiched between an electron microscope positioned above and an inverted-type laser microscope positioned below. It is possible to fix an electron beam and to scan the optical beam. It is effective to supply electrons to an electrode in

order to obtain the image induced by the optical beam.



**Figure 3.** Scanning electron and laser beams induced current (SELBIC) measurement system



**Figure 4.** Current image of TSV obtained by scanning 1.064  $\mu\text{m}$  laser

Figure 4 shows the current image of TSV obtained by scanning 1.064  $\mu\text{m}$  laser. It is seen that the right hand side of one TSV showed the high current. It suggests that the leakage point in the insulating layer exists inside the via wall. Since nondestructive and electrical measurements are available, this method is effective for the failure analysis of TSV.

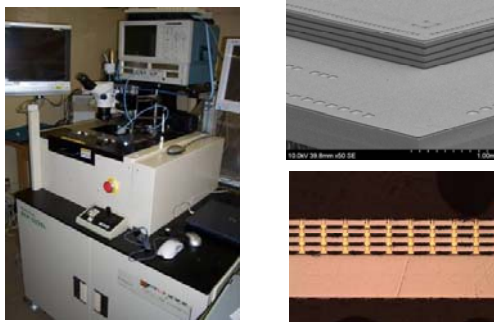
Usually the usage of electron beam requires the vacuum chamber, and the size of chamber must be big if 300mm wafer is tested. The scanning laser beam induced current (SLBIC) system was also developed, as shown in Fig.5. Two laser beams without electron beam can irradiate 300 mm wafer from the bottom, and the current image can be obtained by moving the wafer stage after scanning the laser.

Figure 6(a) shows the time domain reflectometry (TDR) measurement system developed for detecting failure points inside a device embedded substrate. It consists of TDR oscilloscope and semi-automatic prober. The step voltage with a rise time of 15ps is applied to the substrate, and reflection signal is measured. Figure 6(b) is the stacked TEG chips with TSV on the silicon interposer. Intentionally solder bump between TEG chips

was removed in order to make disconnections, and TDR signal was measured in order to detect the failure points. The reflection signal was differentiated with respect to time, and the peak position was obtained in order to calculate the electrical length from the input terminal. Figure 7 is the plot of electrical length vs. distance. The distance between the input terminal and disconnection point was measured by observing the cross-sectional view. It is seen that electrical length is proportional to distance. It means that from the TDR signal it is possible to evaluate the failure point for stacked chips.

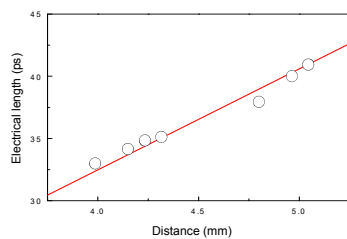


**Figure 5.** Scanning laser beam induced current (SLBIC) measurement system



(a) (b)

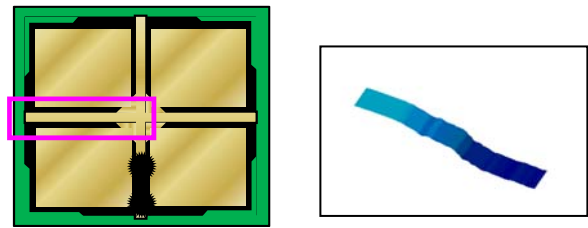
**Figure 6.** Time domain reflectometry (TDR) system (a) with 15ps rise time was applied to stacked TEG chips (b) with TSV in order to detect the failure point of TSV interconnection



**Figure 7.** Electrical length vs. distance obtained from TDR measurements



**Figure 8.** MEMS wafer test system with multimode infrared laser of 1.55  $\mu\text{m}$  in wavelength



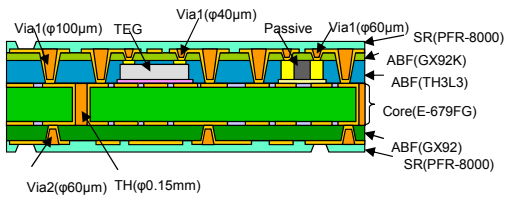
(a) (b)

**Figure 9.** 3D acceleration device (a) and the vibration with time (b) measured at the red square region of (a)

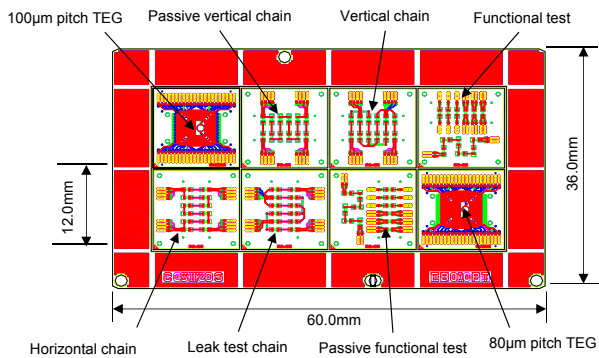
Figure 8 shows the MEMS wafer test system. The multimode infrared laser with central wavelength of 1.55  $\mu\text{m}$  has about 60 different wavelengths. After passing the spectrometer, 60 laser points irradiate the sample at the same time. Figure 9(a) shows the 3D acceleration device, and laser beams irradiate the red square region at the same time, for example. Doppler effect enables to measure the motion, as shown in Fig.9(b). Fast measurements in  $\mu\text{s}$  range are possible. Since it can measure the motion very fast, the failure due to deep reactive etching can be eliminated by the scanning the laser on the wafer.

## EVALUATION KITS OF DEVICE EMBEDDED SUBSTRATE

In March, 2011, a new research center was constructed in Fukuoka, Japan. Starting from design, analysis, prototyping and test of device embedded substrates are possible in the volume production level. Also 8" silicon wafer process to make TEG chips with TSV structure is available in the center. According to JPCA standard on device embedded substrate EB01 (Edition 5), electrical test boards have been developed. Figure 10 shows structure of device embedded substrate for evaluation. TEG chips and discrete devices 1005 and 0603 are embedded, and connected through vias.



**Figure 10.** Cross section of device embedded substrate



**Figure 11.** Evaluation kit of device embedded substrate SIPOS\_EB01

Figure 11 shows the evaluation kit SIPOS\_EB01 for device embedded substrates. This kit has been used in order for device companies to perform the functional test of discrete devices embedded inside the substrate with common substrate structure.

## ACKNOWLEDGEMENTS

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