SUSTAINED HIGH-TEMPERATURE VIBRATION RELIABILITY OF THERMALLY AGED LEADFREE ASSEMBLIES IN AUTOMOTIVE ENVIRONMENTS

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ABSTRACT
Applications in downhole drilling, automotive industry and avionics industry require exposure of electronics to sustained high temperatures electronics combined with vibration loads. In these conditions, maximum temperature can exceed 200 ℃ and vibration G-level up to 10g. Combined effect of elevated temperature and vibration can cause faster failure in electronics components. In this study, reliability for SAC105 and SAC305 electronics operation at elevated test temperature and vibration has been studied. Pristine and aged test board with lead-free SAC daisy chain CABGA packages have been subjected to harmonic vibration at their 1st natural frequency at three test temperatures (25°C, 55°C and 155°C) and vibration with amplitude of 5g, 10g and 14g. Test boards were exposed to isothermal aging conditions at 150°C for 60 days. Hysteresis loop and plastic work density of critical solder joint extracted using FEA based global and local method. S-N curves were obtained for test vehicle. Failure mode analysis has been done for test board. Anand Viscoplasticity material data from the prior studies by the authors have been used to capture the high-strain rate temperature dependent aging behavior of the solder joints. A new model has been proposed to predict the high frequency fatigue life under simultaneous temperature-vibration.

Key words: High Temperature Vibration, Reliability, Solder Joints, Automotive Electronics, Downhole Electronics, Hysteresis Loops, Life Prediction.

INTRODUCTION

Electronics applications have emerged in downhole drilling, automotive industry and avionics industry may be subjected to combined temperature and vibration loads in addition to extended term high-temperature storage. Electronics products in downhole drilling applications exhibit degradation or failures at operating temperatures of 150 to 175℃ [Johnson 2004; Watson 2012]. Automotive underhood electronics located on-engine or on-transmission, can subjected to combined mechanical vibration and sustained high temperature operation. Maximum sustained operating temperature can reach 200℃ in presence of simultaneous vibration G-level of up to 10g. Prior work has shown that electronics subjected to simultaneous temperature-vibration exhibit different degradation signatures and failure modes in comparison with exposure to single stresses [Basaran 2002; Barker 1990; Qi 2004]. There is scarcity of life-prediction models and experimental data for assessing the effect of simultaneous stresses on the expected life of the electronics assembly. Further, electronics subjected to vibration may experience high-strain rate deformation super-imposed on thermally activated creep and stress relaxation. Prior work focuses on the assessment of reliability of electronics under single stresses of temperature and vibration [Steinberg 1988; Henderson 1995; Hu 1995; Lau 1991; Upadhyayula 1997; Li 2001]. Life prediction models have been proposed for solder joints subjected to the single stresses of thermal cycling [Tavernelli 1962]. Occurrence of multiple failure mode including solder fatigue, copper trace or lead fracture due to high cycle fatigue have been reported under vibration loads [Wong 1997]. However, very few researchers have investigated the reliability of solder joint under high temperature and vibration at same time.

A number of methods have been previously used to assess the solder joint reliability under single stresses. Finite element method has been used to quantify deformation of solder joint [Pitarresi 1991, 1993, Park 2007, Lall 2007, 2008, 2009, 2010, 2012, 2013, 2014, 2015, 2016, 2017, 2018]. FE models have also been developed to predict fatigue life in conjunction with damage relationships for electronic components under single stress of mechanical-vibration [Chen 2008, Zhao 1999]. Global-local modeling methods with smeared properties have been used to assess the vibration reliability in a computationally efficient manner [Wong 2007, Lall 2013, 2017, Limaye 2013]. Sub-modeling technique has been used to investigate the deformation of solder joints in both shock and vibration [Syed 2007, Lall

2013, 2017]. It is fairly well established that package reliability behavior is hugely impacted by the PCB deformation and stiffness. Material properties of the printed circuit board change with operating temperature during transition through the glass transition region. The changes are significant enough to change the natural frequencies of the printed circuit assembly under vibration [Lall 2013, 2017]. Digital image correlation has been used to capture the deformation of the printed circuit assemblies under drop-shock and vibration [Lall 2007, Park 2007, 2008, Miller 2007]. S-N curves for solder joints have been plotted using a combination of fatigue life data and stress amplitude from simulation under single stress of vibration [Al-Yafawi 2010, 2011, Lall 2013]. A comparison of failure modes of various SAC alloys compositions has been studied by the authors at elevated operating temperatures (25, 55 and 155°C) and vibration (5g and 14g) [Lall 2017 and Lall 2018].

In this study, the reliability of thermally aged assemblies which have been stored in non-climate controlled enclosures prior to operation has been studied under combined stresses of temperature and vibration. Pristine and aged test board with lead-free SAC daisy chain CABGA packages have been subjected to harmonic vibration at their 1st natural frequency at three test temperatures (25°C, 55°C and 155°C) and vibration with amplitude of 5g, 10g and 14g. Test boards were exposed to isothermal aging conditions at 150°C for 60 days. Resistance data were measured at each test conditions using high speed data acquisition. The experimental system characteristics such as mode shapes and natural frequencies and displacement amplitudes for each test condition compared with global-local FE models. A comparison of strain data from the center of test board has been done using strain gauge and DIC. Hysteresis loop and plastic work density of critical solder joint extracted using FEA based global and local method. Failure mode analysis has been done for test board. Anand Viscoplasticity material data from the prior studies by the authors have been used to capture the high-strain rate temperature dependent aging behavior of the solder joints. A comparison between simulation and experimental results is conducted. In this paper, a new model has been proposed to predict the high frequency fatigue life under simultaneous temperature-vibration.

TEST VEHICLES AND TEST MATRIX

In this paper, the reliability of lead-free SAC (SAC105 and SAC305) solder alloys at high temperature and vibration for pristine and thermally aged assemblies. Test vehicle design with lead free SAC solder alloy components is shown in Figure 1. The test vehicle is intended to assess the stresses encountered by engine mounted control units subjected to harmonic vibration due to the engine RPM or due to road shock. Test vehicle used in this study has 12 daisy-chained CABGA288 packages arranged in a 4x3 configuration with lead-free solder daisy-chained packages as shown in Figure 1. The 8-layer board is 132mm in length, and 77mm in width. Board thickness is 1.6mm. Internal layers of the board has copper loading to simulate the power and ground planes of functional printed circuit assemblies. Pads on the board have immersion-silver finish. The detailed test board and package attributes are listed in Table 1. X-ray image of CABGA288 package is shown in Figure 2. The board assemblies have been tested in Mode-1 deformation, which involves the deformation of the board assembly in a half-sine waveform at their first natural frequency.

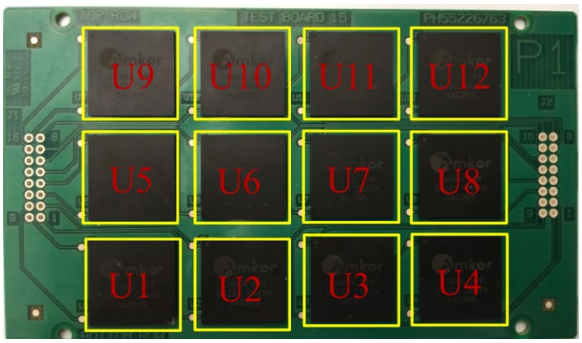


Figure 1: Test Vehicle used in this study

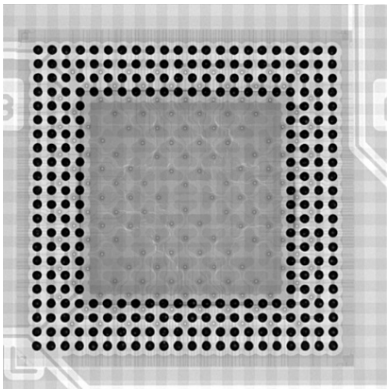


Figure 2: X-ray Image of CABGA288 package.

Table 1: Test Board & Package Attributes

Test Board				
Dimension			132mmx77mmx1.6mm	
Layers			8 Layered (FR4)	
Finish			Immersion Silver	
Packages per Board			12	
Package	Pitch (mm)	Ball Dia.	Solder Alloy	I/O Count
CABGA	0.8	0.46	SAC105 SAC305	288

Table 2: Detailed Test Matrix.

Test Temp (C)	Stress Level: 5G, 10G, 14G.			
	SAC105		SAC305	
	No aging	60 Days	No Aging	60 Days
25 °C	X	X	X	X
55 °C	X	X	X	X
155 °C	X	X	X	X

Since the first-natural frequency of the board assemblies vary in the test population, the test has been conducted through use of a narrow window time-sweep centered around the first natural frequency. Vibration acceleration levels of 5, 10 and

14 G at elevated temperatures have been used for the test. The results of pristine assemblies has been compared with assemblies which have been subjected to aging for 60-days. The detailed test matrix is shown in Table 2.

EXPERIMENT SETUP

High-temperature vibration has been conducted using a LDS 722 series electro-dynamic shaker with an isothermal oven. The out-of-plane vibration has been measured through a glass window of the chamber providing direct view of the printed circuit assembly during vibration.

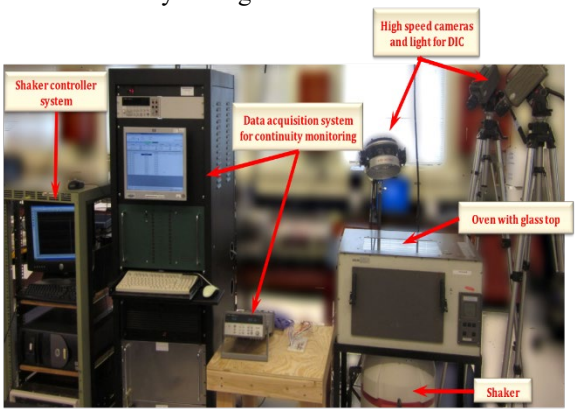


Figure 3: Experimental set up for High-TempVibration.

Digital image correlation in conjunction with a speckle pattern on the board assembly has been used to track the deformation during vibration. Resistance data from 12 packages has been simultaneously monitored using a high-speed data acquisition system as shown in Figure 3. The test was run until all packages on the board assemblies failed. Failure was defined as a 20-percent high-resistance event for 20-consecutive cycles. The cycles-to-failure has been recorded for each of the packages in the assembly. The experimental set up is shown in Figure 3. The full experimental set up described in earlier publication by authors [Lall 2017 and 2018].

EXPERIMENTAL MODAL ANALYSIS

Natural frequency (NF) of printed circuit board assembly is computed using Experimental modal analysis (EMA) at elevated temperatures of 25, 55, and 155°C using configuration shown in Figure 4. Two-accelerometers have been used to compute receptance of the board assembly and measure the mode-shapes. The first accelerometer is attached at the center of PCB to measure the board acceleration and second-accelerometer is attached to shaker table to capture the excitation signal.

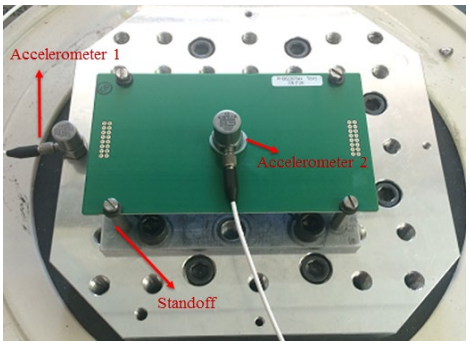


Figure 4: Experimental Modal Analysis (EMA) set up to acquire Natural Frequency.

A sine-sweep profile from 5 Hz to 2000 Hz with constant amplitude of 10 G is used to obtain natural frequencies of the board assembly. Figure 5 shows the transmissibility plot obtained from EMA at 25°C. Figure 5 shows obtained 1st NF from EMA at 25°C which is 360Hz. Higher peaks indicate the frequency-location of the higher mode-shapes and natural frequencies. Since, the board assembly is only subjected to high-temperature vibration in mode-1 in the scope of the present study, only the first natural frequency is relevant for the test data presented.

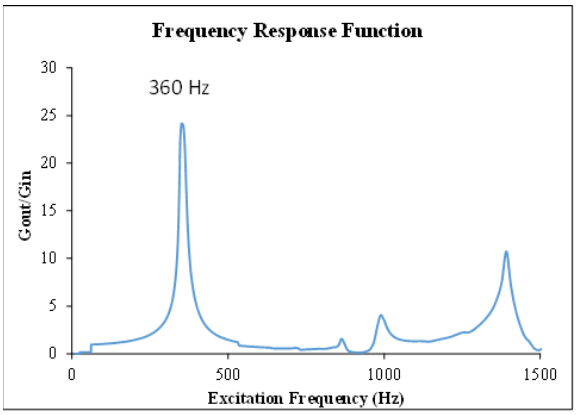


Figure 5: Transmissibility Plot from EMA.

FEA BASED MODAL ANALYSIS

FEA based Modal Analysis has been conducted to predict the NF's and compared to EMA based NF's. A global-model has been created to simulate the vibration events for test-vehicle with implicit finite-element method as shown in Figure 6. The global model with 12 packages is shown in Figure 6. The solder joints have been modeled using Timoshenko beam elements. The cut-section view of meshed package of test board is shown in Figure 7.

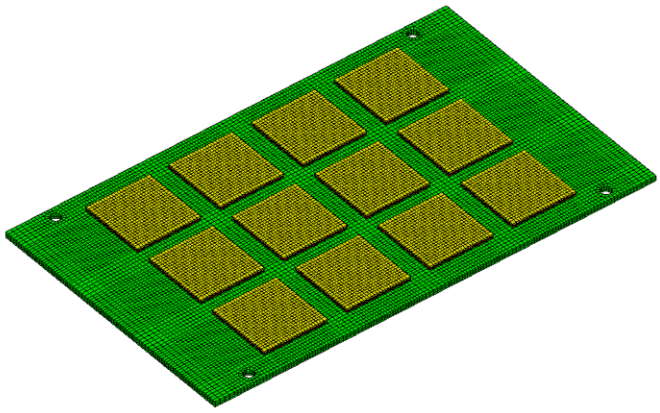


Figure 6: Global Model of Test Vehicle with 12 CABGA packages.

Internal details of the package elements have been modeled including the substrate, mold compound, silicon die, adhesive. Details of the element types used to build the model are shown in Table 3. Four mass elements are also created at screw holes of PCB to apply the boundary conditions with Input-G method. All materials are modeled with linear elastic materials. Materials properties used in FEA based models shown in Table 4. Results from the EMA have been compared with FEA modal analysis predictions.

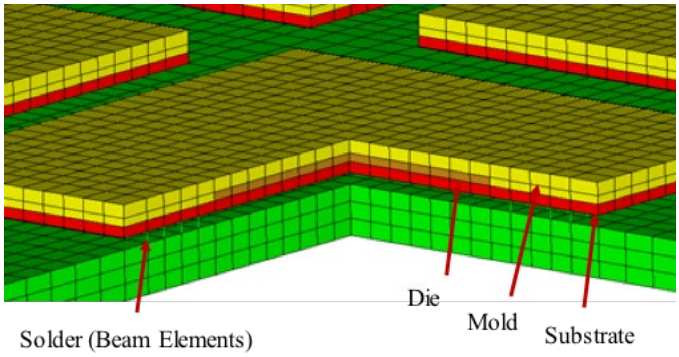


Figure 7: Cut-Section View of CABGA288.

Table 3: Elements Type for Global Model

Board Assembly	Element Type
PCB	SOLID 45
Copper Pad	SOLID 45
Mold Compound	SOLID 45
Silicon Die	SOLID 45
Die Attach	SOLID 45
BT Substrate	SOLID 45
Corner Joints	VISCO 107
Center Joints	BEAM 188
Mass Element	MASS 21

Table 4: Material Properties

Package Assembly	E (MPa)	Poisson's Ratio	Density (tonne/mm^3)
Solder Joints	42000	0.34	8.40E-09
EMC	23500	0.25	1.65E-09
Silicon Die	162000	0.28	2.33E-09
Die Attach	2760	0.35	7.80E-09
BT Substrate	17400	0.28	1.80E-09
Copper Pad	129000	0.34	8.82E-09
PCB	23.8	0.39	1.80E-09

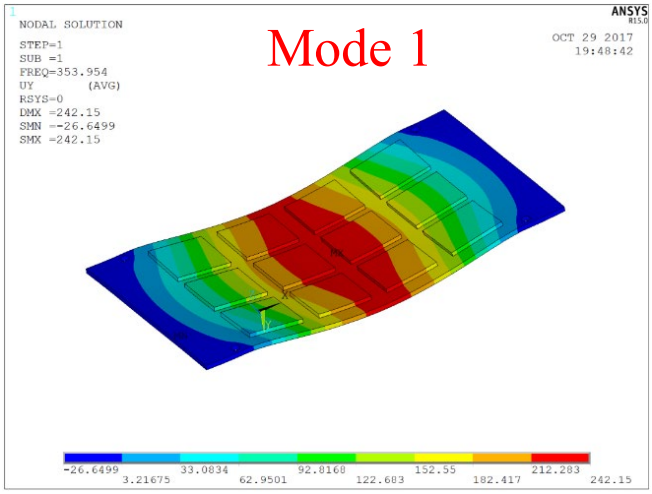


Figure 8: Mode-1 of Test Vehicle

Comparison of the modeled weight with the experimental weight shows the modeled weight of 50.5gm correlates well to the actual weight of 50.9gm measured using a weighing scale. Comparison of the 1st natural-frequency obtained from EMA with the FEA model predictions indicates less than 2-percent deviation in the predicted results as shown in Table 5 and Figure 8-to-Figure 11 show four mode shapes and NF's obtained from Modal Analysis for the board assembly. Deformed shape in mode-1 indicates that not all the components mounted on the board assembly experience identical board strains or solder joint stress histories.

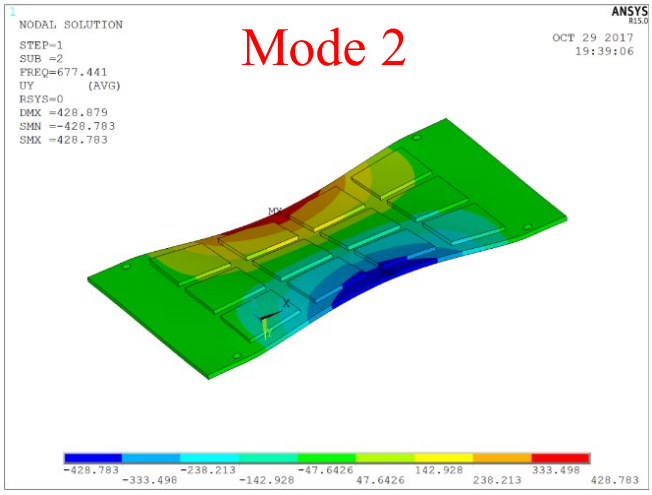


Figure 9: Mode-2 of Test Vehicle

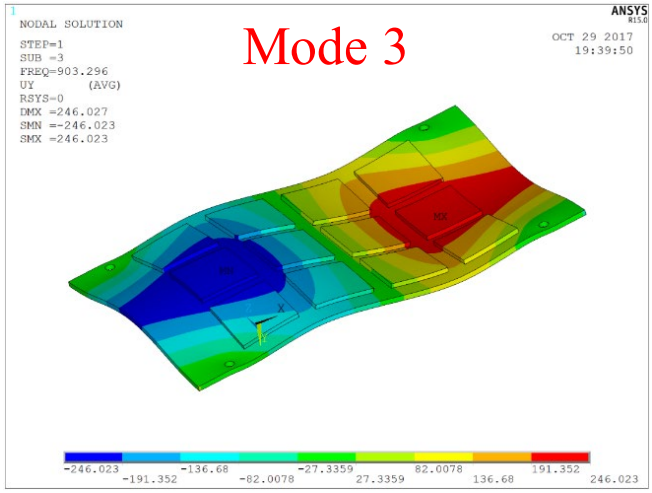


Figure 10: Mode-3 of Test Vehicle

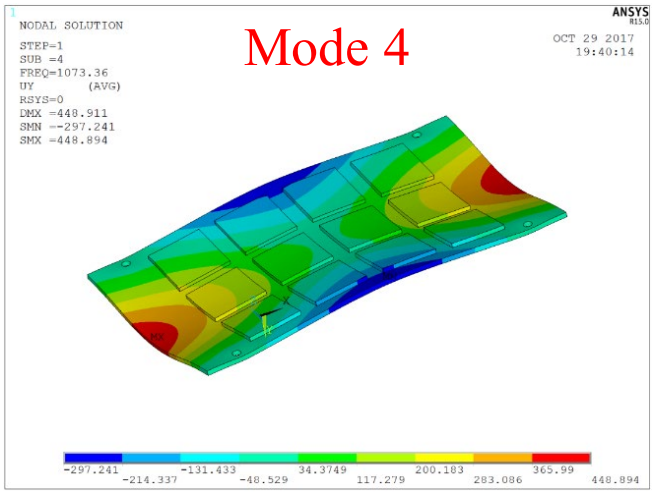


Figure 11: Mode-4 of Test Vehicle

EFFECT OF OPERATING TEMPERATURE ON 1ST NATURAL FREQUENCY

Effect of elevated operating temperature on natural frequency of the board assembly has been studied in the temperature range of 25-155°C. Board temperature has been measured using a thermocouple attached on the surface of the board assembly. The measured natural frequencies at elevated temperatures are shown in Table 5 and Figure 12. The natural frequencies for mode-1 indicate a linear variation with temperature. The rate of change in the natural frequency is found to be about 0.53 Hz/°C. The temperature dependence of natural frequency is attributed to the temperature dependence of the elastic modulus for the printed circuit board and that of the electronic mold compound in the ball-grid arrays mounted on the board. Mode-shape 1 of board assembly at 55°C and 155 °C are shown in Figure 13 and Figure 14 respectively.

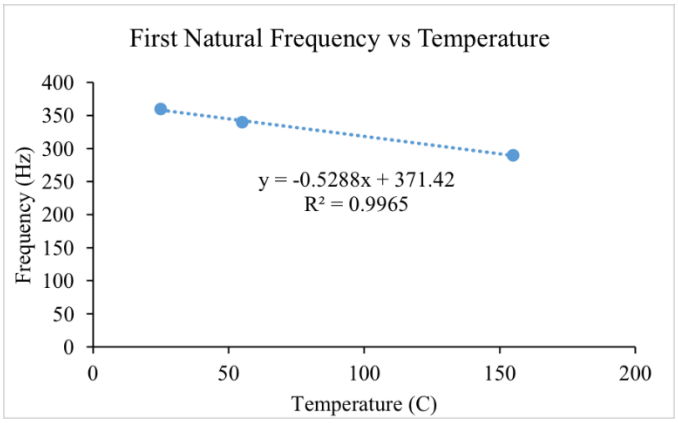


Figure 12: Variation in 1st NF due to operating Temperature.

Table 5: EMA and FEA based 1st NF Comparison

Temperature (°C)	Experiment (Hz)	Simulation (Hz)	error (%)
25	360	353	-1.94
55	342	337	-1.46
155	291	289	-0.69

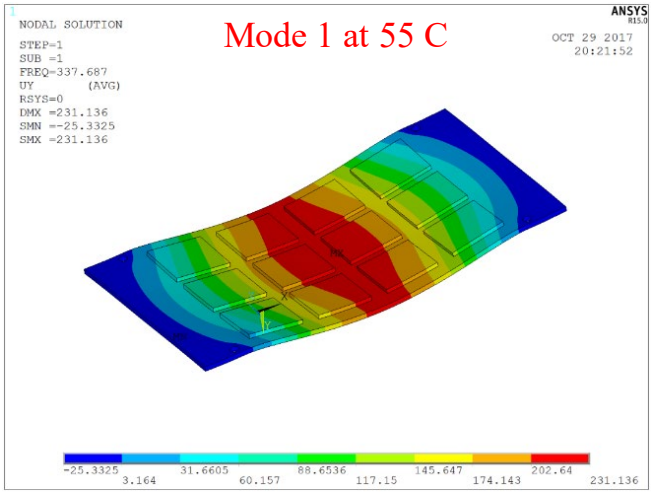


Figure 13: Mode Shape-1 at 55°C.

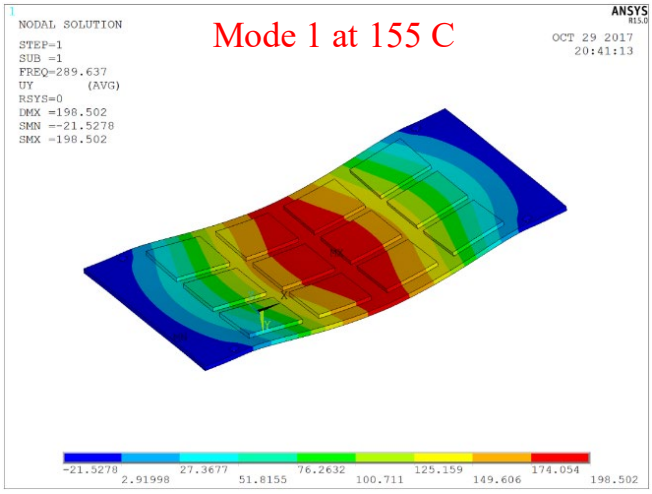


Figure 14: Mode Shape-1 at 155 °C.

RESISTANCE DATA

Resistance data were measured using high-speed data acquisition from each of the twelve daisy-chained packages while subjected to vibration at elevated temperatures. Resistance vs cycles plots are shown in Figure 15 to **Error! Reference source not found.** for test vehicle. Effect of package location also has been studied. Packages at different board-locations exhibit different cycles-to-failure owing to different PCB strain levels.

SAC105 at 5G

Predominant failure locations on the SAC105 assembly are at U1, U3 and U6 at operating temperature of 25°C and 5G acceleration (Figure 15). Thus, the locations closer to the support points and center of the board assembly are the most prone to failure. Once failure initiates, the resistance increases rapidly with the increase in the cycles to failure.

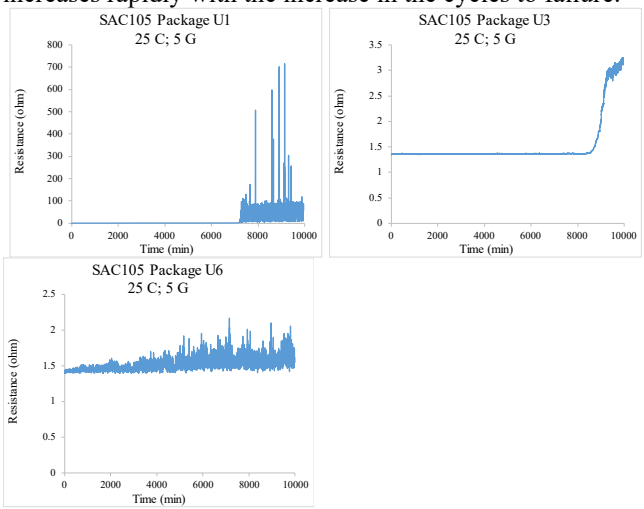
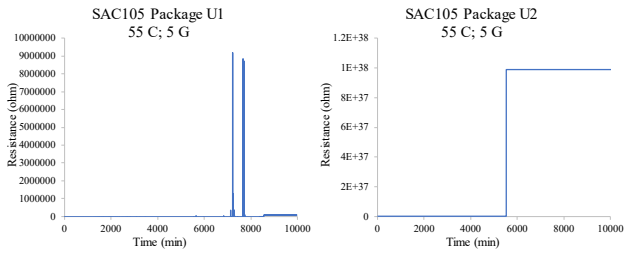


Figure 15: SAC105 Resistance vs time at 25°C at 5G.

For operating temperature of 55°C and 5G acceleration, predominant failure locations on the SAC105 assembly are at U1, U2, U5 and U6 (Figure 16). Thus, additional failure locations of U2 and U5 surface with the increase in test temperature to 55°C. Thus, the locations closer to the support points and center of the board assembly continue to be most prone to failure even at the higher test temperature. Once failure initiates, the resistance increases rapidly with the increase in the cycles to failure.



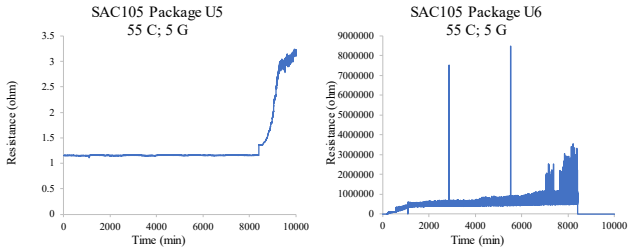


Figure 16: SAC105 Resistance vs time at 55°C at 5G.

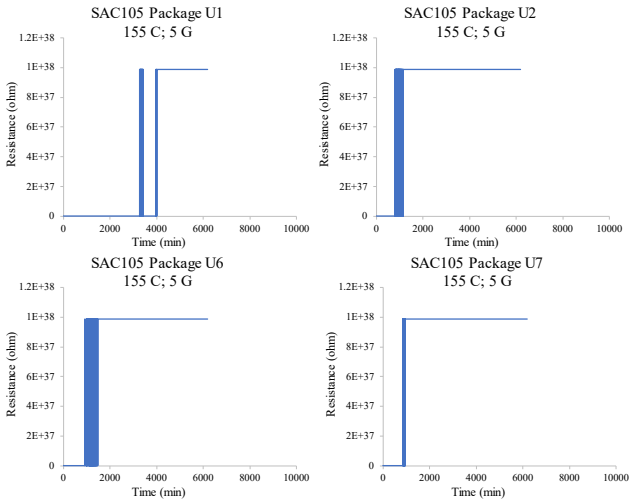
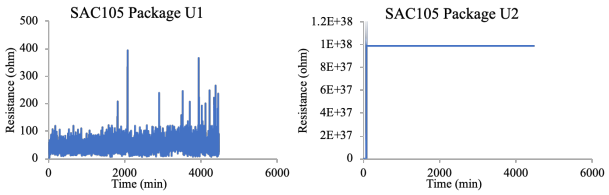


Figure 17: SAC105 Resistance vs time at 155°C at 5G.

For operating temperature of 155°C and 5G acceleration, predominant failure locations on the SAC105 assembly are at U1, U2, U6 and U7 (Figure 17). Thus, additional failure locations of U6 and U7 surface with the increase in test temperature to 155°C. Thus, the locations closer to the center of the board assembly have a higher incidence of failure at the higher test temperature. Once failure initiates, the resistance increases rapidly with the increase in the cycles to failure.

SAC105 at 10 G

Predominant failure locations on the SAC105 assembly are at U1, U2, U6, and U7 at operating temperature of 25°C and 10G acceleration (Figure 18). Thus, similar to the test acceleration of 5G @25°C, the locations closer to the support points and center of the board assembly are the most prone to failure. The transition to failure is much more abrupt, and once failure initiates, the resistance increases rapidly with the increase in the cycles-to-failure in most locations closer to the center of the board assembly.



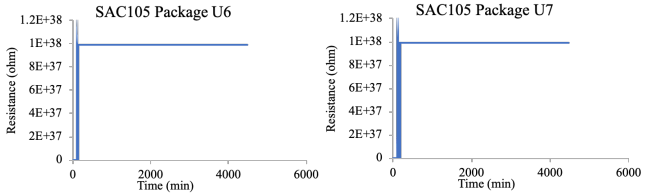


Figure 18: SAC105 Resistance vs time at 25 °C at 10G.

For operating temperature of 55°C and 10G acceleration, predominant failure locations on the SAC105 assembly are at U1, U2, U5 and U6 (Figure 19). Thus, the failure locations are identical to those at test acceleration of 5G at 55°C. Thus at 10G @55°C, the locations closer to the support points and center of the board assembly continue to be most prone to failure even at the higher test temperature. Once failure initiates, the resistance increases rapidly with the increase in the cycles to failure.

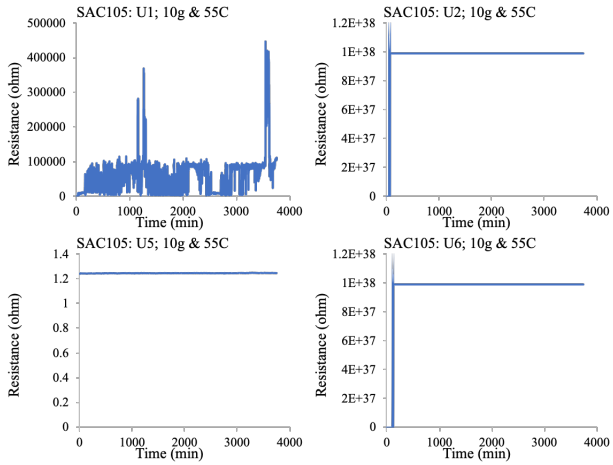
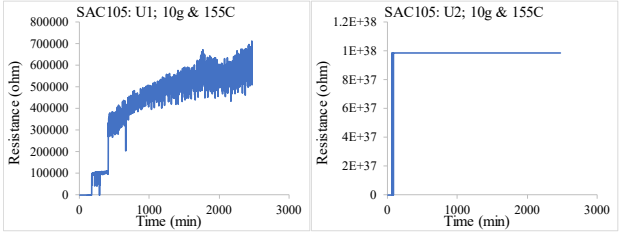


Figure 19: SAC105 Resistance vs time at 55 °C at 10G.

For operating temperature of 155°C and 10G acceleration, predominant failure locations on the SAC105 assembly are at U1, U2, U5 and U6 (Figure 20). Thus, in comparison with the 5G @155°C test condition, the U5 failure location replaces U7. However, U7 is a mirror image of the U5 failure location – thus the failure location map is similar to that of 5G @155°C test condition. For the 10G @155°C test condition, locations closer to the center of the board assembly have a higher incidence of failure at the higher test temperature. Once failure initiates, the resistance increases rapidly with the increase in the cycles to failure.



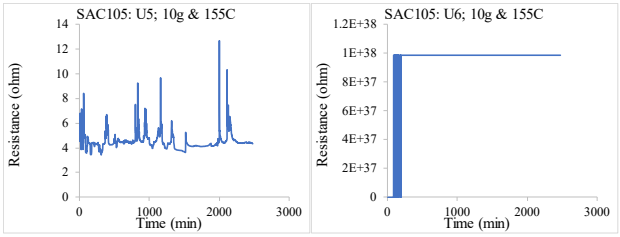


Figure 20: SAC105 Resistance vs time at 155 °C at 10G.

SAC305 at 5G

Predominant failure locations on the SAC305 assembly are at U1, U2, U3 and U6 at operating temperature of 25°C and 5G acceleration (Figure 21). Thus, similar to 5G @25°C test condition for SAC105, the locations closer to the support points and center of the board assembly are the most prone-to-failure. Once failure initiates, the resistance increases rapidly with the increase in the cycles to failure.

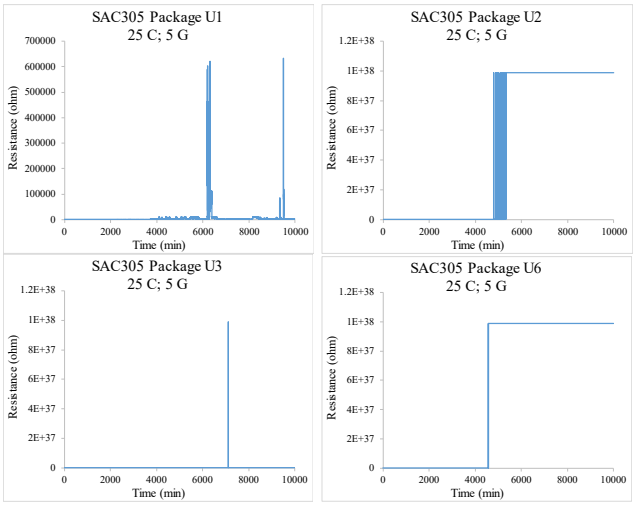
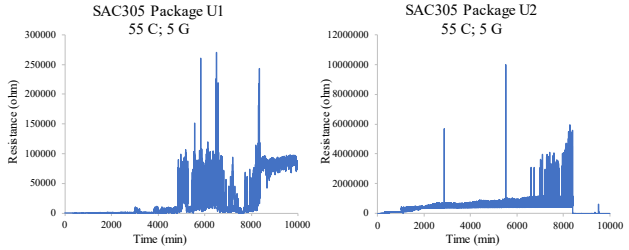


Figure 21: SAC305 Resistance vs time at 25°C at 5G.

For operating temperature of 55°C and 5G acceleration, predominant failure locations on the SAC305 assembly are at U1, U2, U6 and U7 (Figure 22). Thus, the failure locations are not identical to those at test acceleration of 5G at 55°C for SAC105. Thus at 5G @55°C for SAC305, the U7 failure location replaces U5 in comparison with 5G @55°C for SAC105. However, U7 is a mirror image of the U5 failure location – thus the failure location map is similar to that of 5G @55°C test condition for SAC105. However, the locations closer to the support points and center of the board assembly continue to be most prone to failure even at the higher test temperature. Once failure initiates, the resistance increases rapidly with the increase in the cycles to failure.



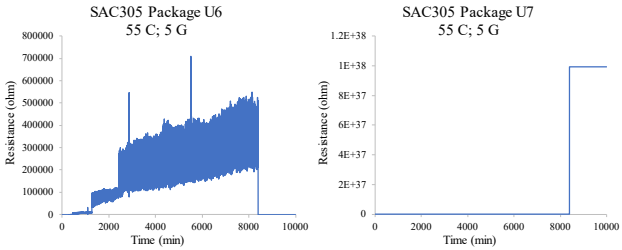


Figure 22: SAC305 Resistance vs time at 55°C at 5G.

For operating temperature of 155°C and 5G acceleration, predominant failure locations on the SAC305 assembly are at U1, U2, U6 and U7 (Figure 23). Thus, in comparison with the 5G @155°C test condition for SAC105, the failure locations are identical. For the 5G @155°C test condition, locations closer to the center of the board assembly have a higher incidence of failure at the higher test temperature. Once failure initiates, the resistance increases rapidly with the increase in the cycles to failure.

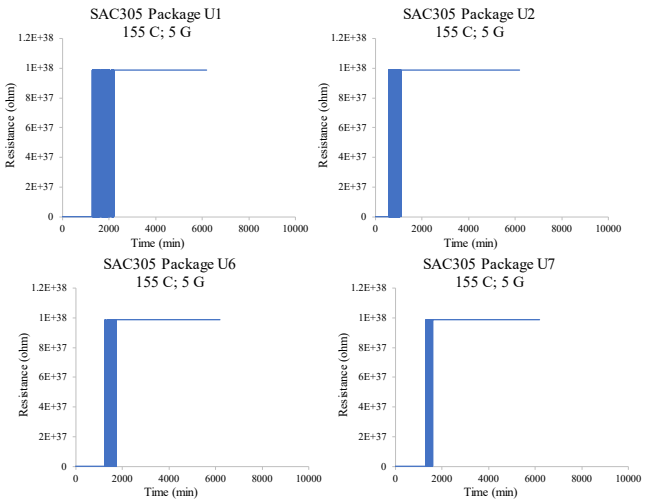
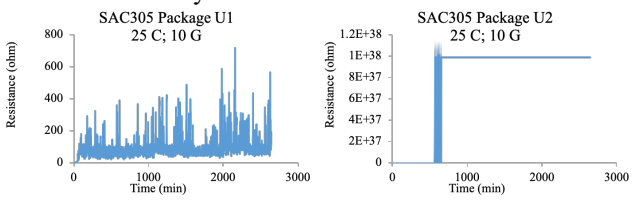


Figure 23: SAC305 Resistance vs time at 155°C at 5G.

SAC305 at 10G

Predominant failure locations on the SAC305 assembly are at U1, U2, U6, and U7 at operating temperature of 25°C and 10G acceleration (Figure 24). Thus, in comparison with the 10G @25°C condition for SAC105 the failure locations are identical. Similar to the test condition of 10G @25°C for SAC105, the locations closer to the support points and center of the board assembly are the most prone to failure. The transition to failure is much more abrupt, and once failure initiates, the resistance increases rapidly with the increase in the cycles-to-failure in most locations closer to the center of the board assembly.



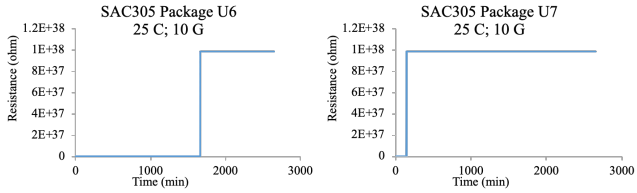


Figure 24: SAC305 Resistance vs time at 25 °C at 10G.

For operating temperature of 55°C and 10G acceleration, predominant failure locations on the SAC305 assembly are at U1, U2, U5 and U6 (Figure 25). Thus, the failure locations are identical to those at test acceleration of 10G at 55°C for SAC105. Thus at 10G @55°C, the locations closer to the support points and center of the board assembly continue to be most prone to failure even at the higher test temperature. Once failure initiates, the resistance increases rapidly with the increase in the cycles to failure.

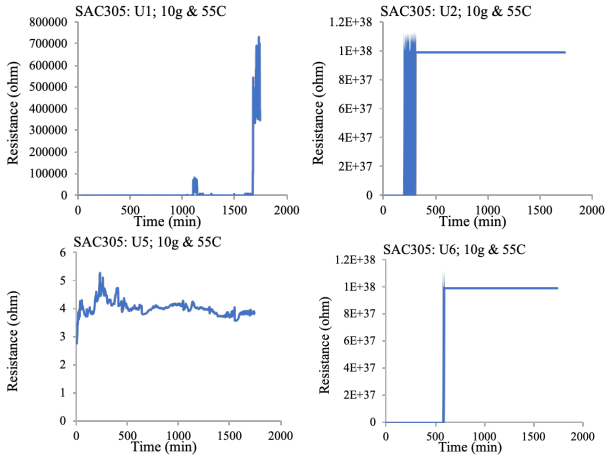


Figure 25: SAC305 Resistance vs time at 55 °C at 10G.

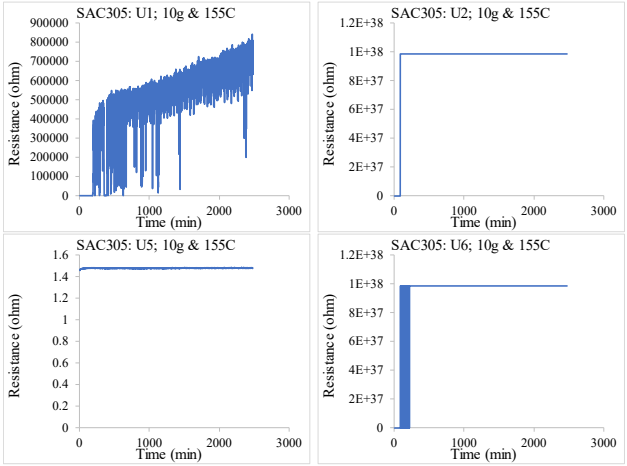


Figure 26: SAC305 Resistance vs time at 155 °C at 10G.

For operating temperature of 155°C and 10G acceleration, predominant failure locations on the SAC305 assembly are at U1, U2, U5 and U6 (Figure 26). Thus, in comparison with the 5G @155°C test condition for SAC105, the failure locations are identical. For the 10G @155°C test condition, locations closer to the center of the board assembly have a higher incidence of failure at the higher test temperature.

Once failure initiates, the resistance increases rapidly with the increase in the cycles to failure.

3D DIGITAL IMAGE CORRELATION (DIC)

PCB deformation history of test vehicle has been measured using 3D-DIC during the vibration events at 1st natural frequency. The experiment setup for DIC measurement has been shown in Figure 27.

Figure 27: 3D DIC Set up.

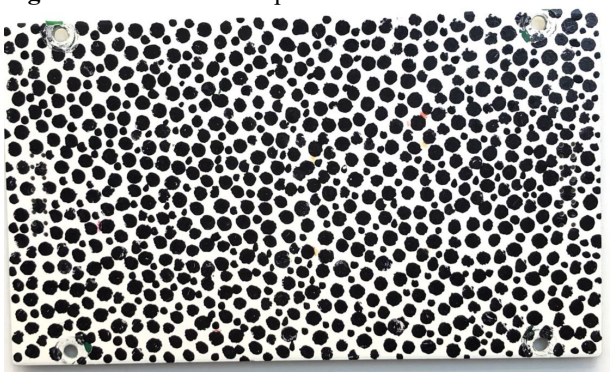


Figure 28: Test Vehicle with speckles pattern.

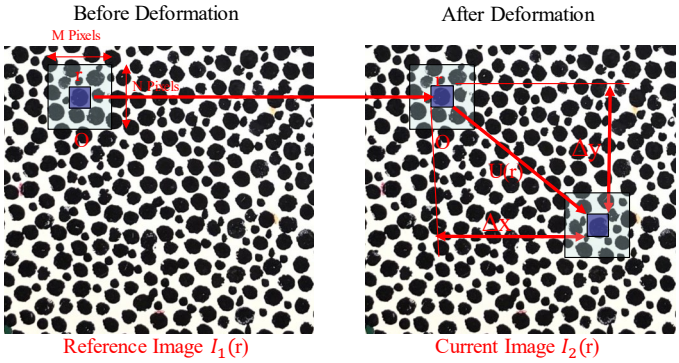
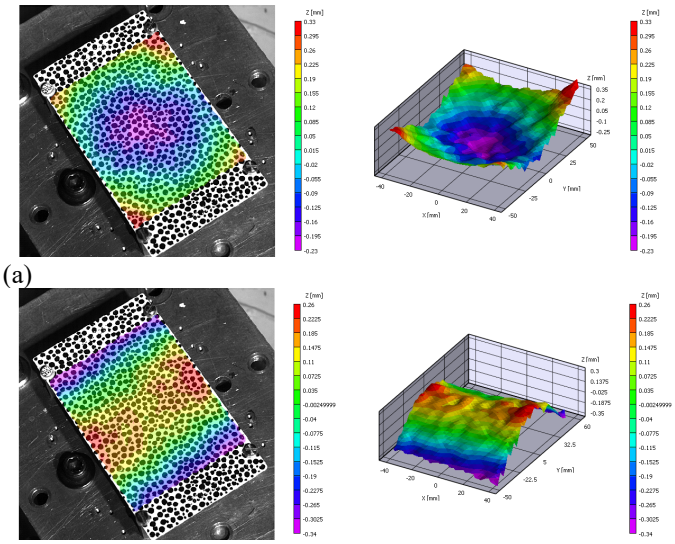


Figure 29: Digital Image Correlation.

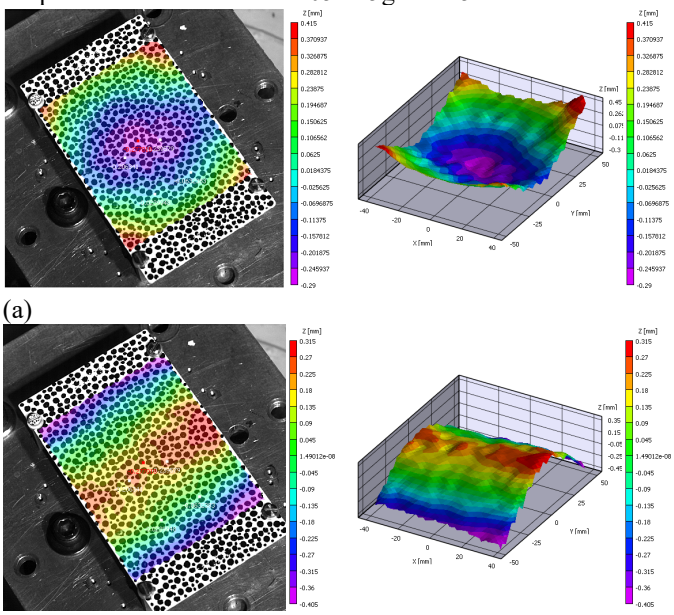
The out-of-plane displacement and strain history of test vehicle are computed in this study. Figure 28 shows the test vehicle with speckles pattern. A high-speed video has been captured to track the motion of the speckles during vibration event. The two high-speed cameras mounted on rigid tripod mounts to prevent movement of the cameras have been used to measure both the in-plane and out-of-plane deformation during vibration as shown in Figure. Previously, 3D-DIC measurement of out-of-plane displacements during the transient shock and vibration events has been demonstrated by [Lall 2007, 2008, 2012, 2014].



(a)

(b)

Figure 30: a) Maximum Downward and b) Upward Displacement Plot for SAC105 at 5g and 25°C.



(a)

(b)

Figure 31: a) Maximum Downward and b) Upward Displacement Plot for SAC105 at 10g and 25°C.

The method of measuring deformation using 3D-DIC is shown in Figure 29. Before deformation and after deformation images have been captured using high-speed cameras. Since a single pixel is not a unique signature of a point hence correlation of neighboring pixels called subset are used. Deformation history for PCB has been measured using 3D-DIC at vibration levels of 5g and 10g at their first natural frequency during vibration events. Figure 30 and Figure 31 shows maximum downward and maximum upward

displacement of PCB at 5g and 10 g respectively. Displacement history have been extracted from PCB deformation history at 5-locations includes center of PCB, U1, U2, U5 and U6 as shown in Figure 32. Effect of Vibration G-level (5G and 10G) dwelling at its first natural frequency (360Hz) at room temperature has been measured.

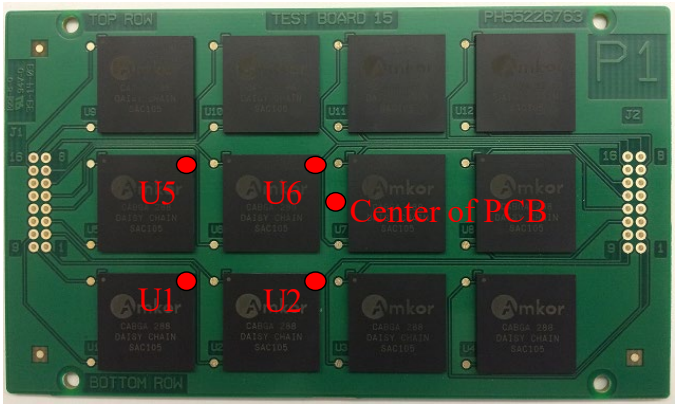


Figure 32: Deformation History Locations on PCB.

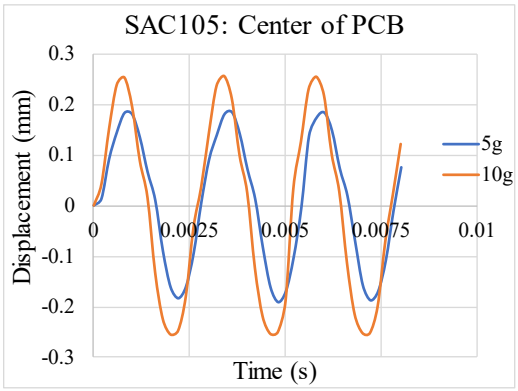


Figure 33: Effect of G-level on Displacement History at center of PCB.

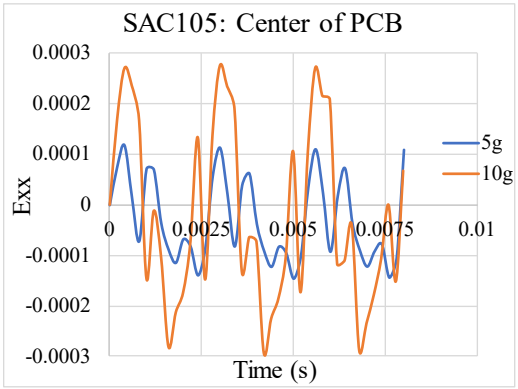


Figure 34: Effect of G-level on Strain History (Exx) at center of PCB.

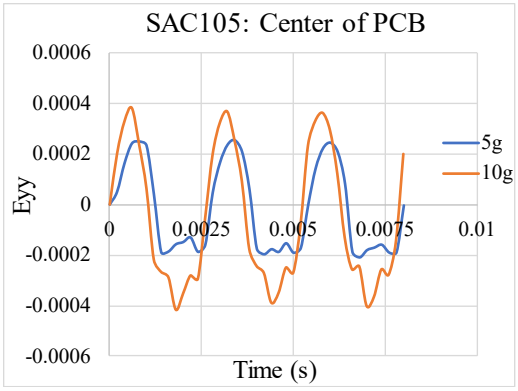


Figure 35: Effect of G-level on Strain History (Eyy) at center of PCB.

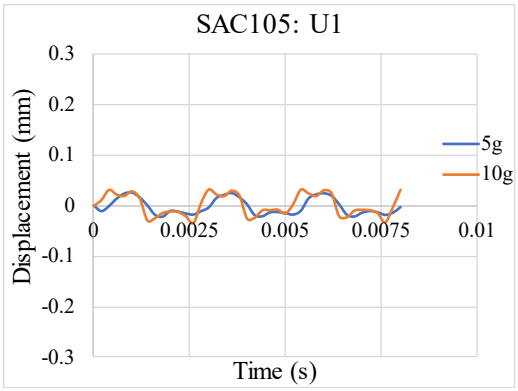


Figure 36: Effect of G-level on Displacement History at U1.

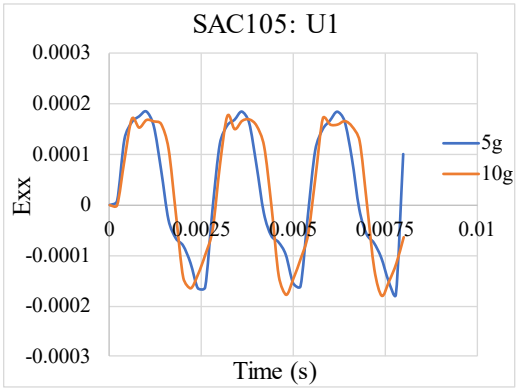


Figure 37: Effect of G-level on Strain History (Exx) at U1.

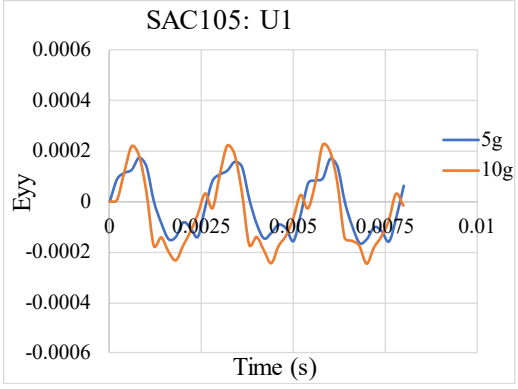


Figure 38: Effect of G-level on Strain History (Eyy) at U1.

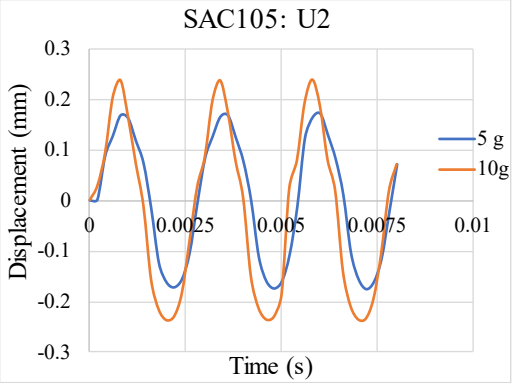


Figure 39: Effect of G-level on Displacement History at U2.

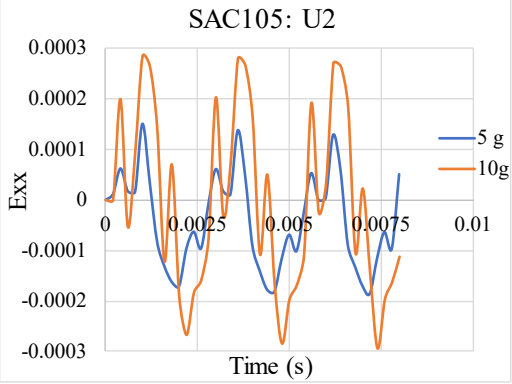


Figure 40: Effect of G-level on Strain History (Exx) at U2.

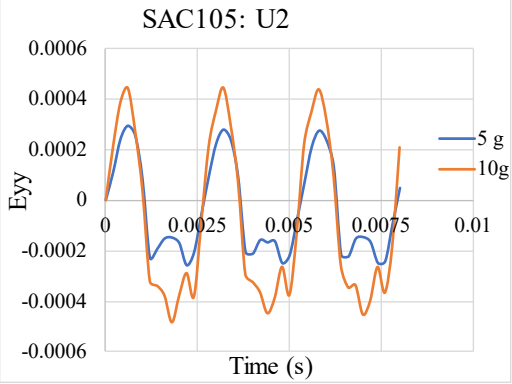


Figure 41: Effect of G-level on Strain History (Eyy) at U2.

The displacement and strain history of Test board at 5-different locations (Figure 32) at different G-level are shown in Figure 33-to-Figure 41. It is easily observed with increase in input G-level, the displacement amplitude and strain level are also increased for all the packages (U1, U2, U5, U6).

FEA BASED INPUT-G METHOD

Vibration at first natural frequency with different G-levels and at elevated temperatures has been simulated using Input-G method. Four mass elements have been created at the center of screw holes of PCB (Figure 42). Desired input acceleration data can be converted to force-data by applying acceleration with the mass of the elements. The mass of this element is five orders magnitude larger than the actual weight of test board. The rigid elements were created to connect mass element to PCB. Figure 43 and Figure 44 indicates the desired input excitation and input force data at different G-level. The tabular force data is applied at the mass node along the normal direction of PCB. A nonlinear transient analysis is used to analyze this vibration event. **Error! Reference source not found.** shows the acceleration history output at the mass node vibrating at 360 Hz and at 14G.

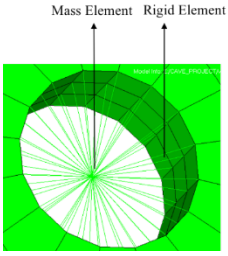


Figure 42: Mass and Rigid Element created at Screw holes of PCB.

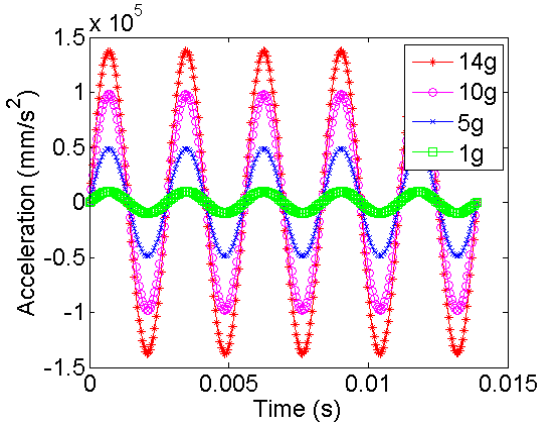


Figure 43: Desired Input Excitation

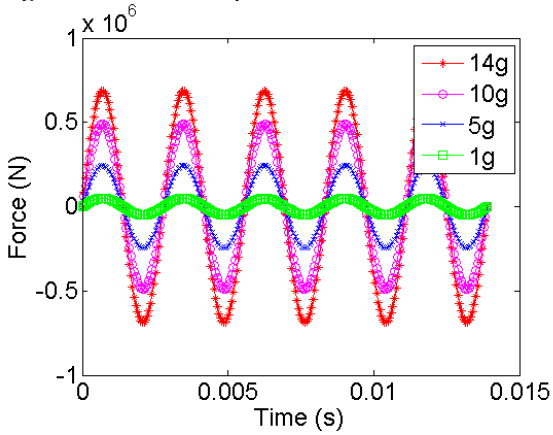


Figure 44: Input Tabular Force Data

NONLINEAR SUB-MODELING

A sub-model has been created at same coordinate system from Global model. Figure 45 to Figure 47 show different views of the sub-model for CABGA288, with four-corner solder ball meshed with VISCO107. Figure 47 shows the meshed solder joint of package. Figure 49 shows the meshed geometry with tabular cutting boundary displacement history applied in ANSYS APDL. The detail procedure to implement non-linear sub-modeling in ANSYS is shown in Figure 48.

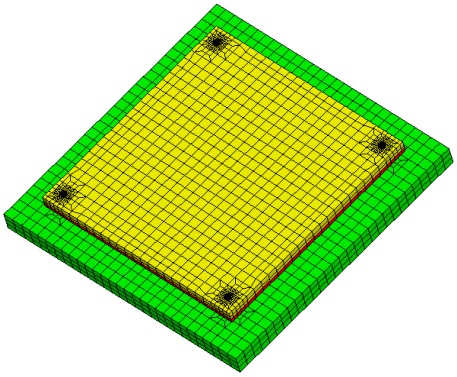


Figure 45: General View of CABGA288.

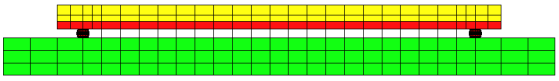


Figure 46: Front View of CABGA288

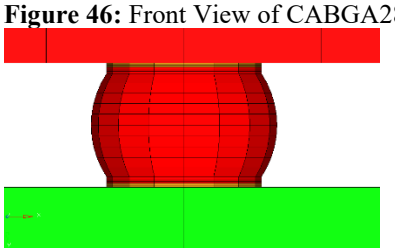


Figure 47: Solder Ball Details of CABGA288.

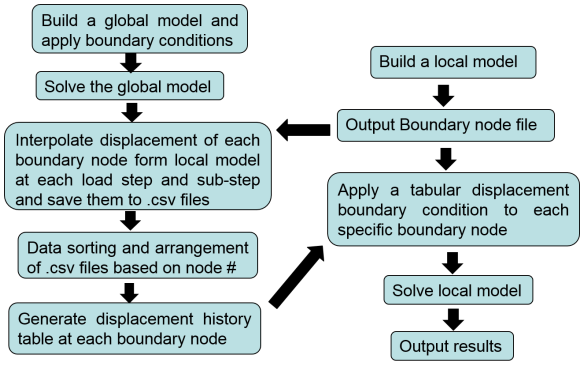


Figure 48: Flow Chart of Nonlinear Sub-modeling Technique.

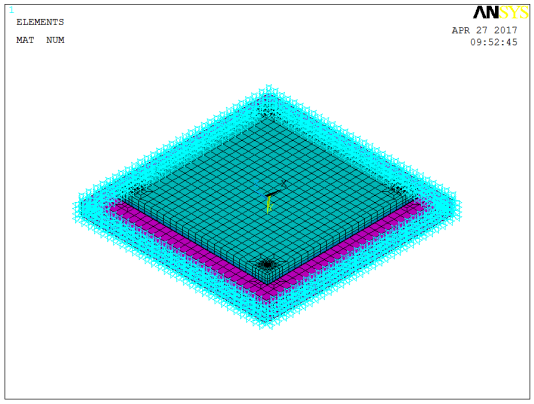


Figure 49: Boundary Condition of CABGA288 in ANSYS.

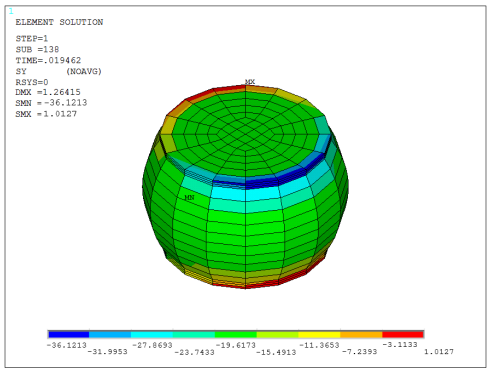


Figure 50: Critical SJ Stress U6 at Max Upward Deformation of PCB (5g, 25°C)

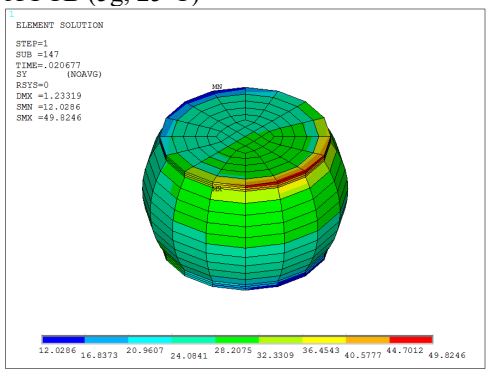


Figure 51: Critical SJ Stress U6 at Max Downward Deformation of PCB (5g, 25°C)

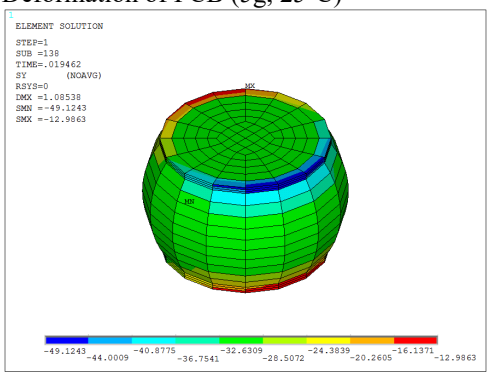


Figure 52: Critical SJ Stress U6 at Max Upward Deformation of PCB (10g, 25°C)

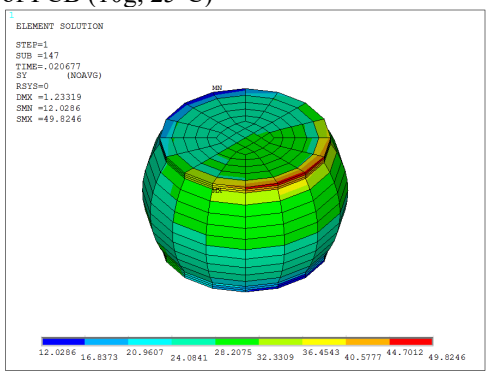


Figure 53: Critical SJ Stress U6 at Max Downward Deformation of PCB (10g, 25°C)

Critical solder joint, i.e. the one with the maximum plastic work is observed at the corner of the package from the

simulation results. Figure 50 to Figure 53 show stress contour plot of critical solder joint of U6 at 25°C for different vibration G-Level. It is observed the maximum stress happened between the solder joint and the copper pad. Hysteresis loop of solder joint has been extracted using stress-strain data. Stress and strain data from top layer of critical solder joint is computed using volume average technique as shown in Equation (1) and Equation (2). Figure 54 to Figure 57 shows the hysteresis loops at different G-level and elevated temperature. The area of hysteresis plot shows plastic work density stored in solder ball per bending cycle.

$$\sigma_{ave} = \frac{\sum_{i=1}^{n} \sigma_i V_i}{\sum_{i=1}^{n} V_i} \quad (1)$$

$$\varepsilon_{ave} = \frac{\sum_{i=1}^{n} \varepsilon_i V_i}{\sum_{i=1}^{n} V_i} \quad (2)$$

Hysteresis loops are extracted from 4-locations (U1, U2, U5, U6) and 2G-levels (5G and 10G) at 25°C. Figure 57 show the effect of G-level on the area of hysteresis loop for package U6. As the G-level increases, the area for hysteresis loop also increased. Figure 54 to Figure 57 show the similar trend at different locations of packages. Furthermore, the packages located at the center of PCB have maximum area of hysteresis loop than other locations, which is because the center packages are subjected to larger deformation.

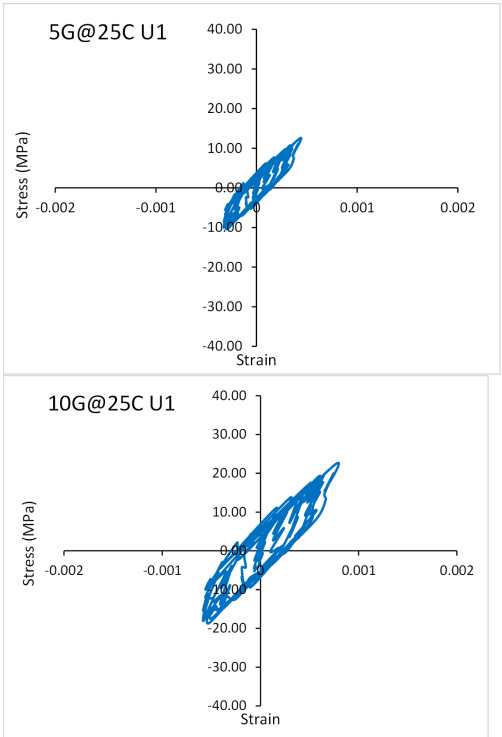


Figure 54: Extracted Hysteresis Loop of Critical Solder Joint (U1 @ 25°C @ 5g and 10g).

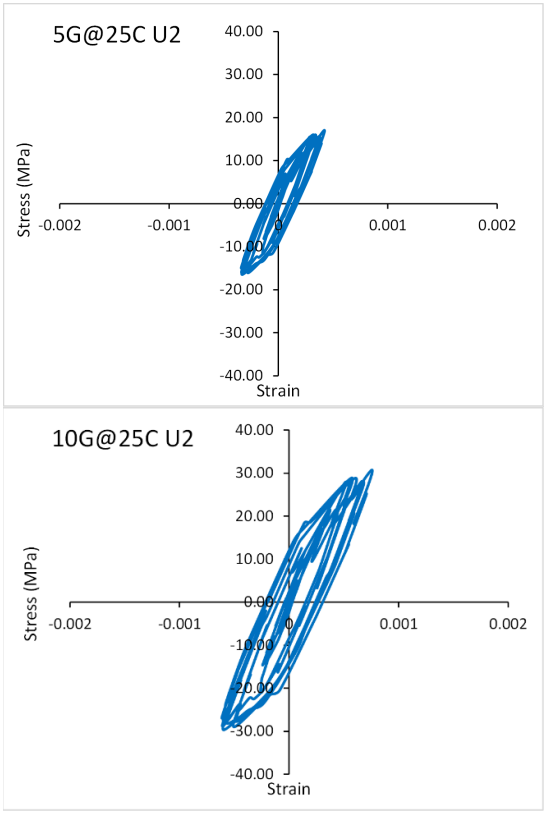


Figure 55: Extracted Hysteresis Loop of Critical Solder Joint (U2 @ 25°C @ 5g and 10g).

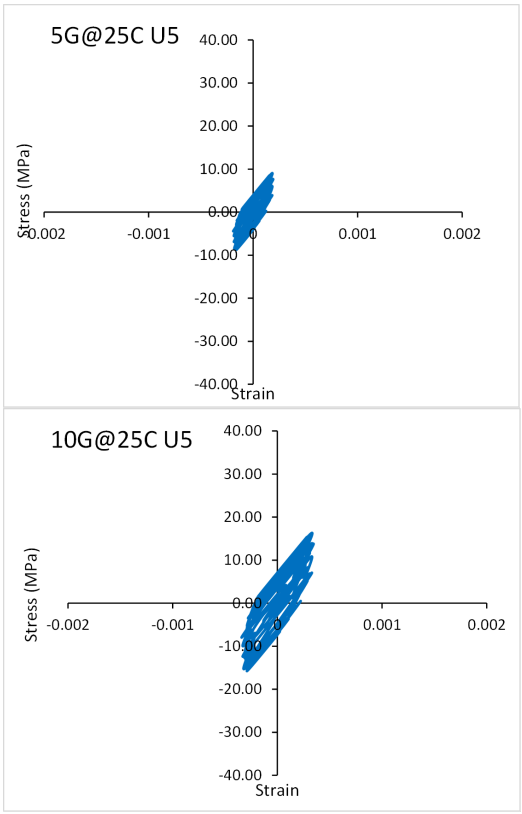


Figure 56: Extracted Hysteresis Loop of Critical Solder Joint (U5 @ 25°C @ 5g and 10g).

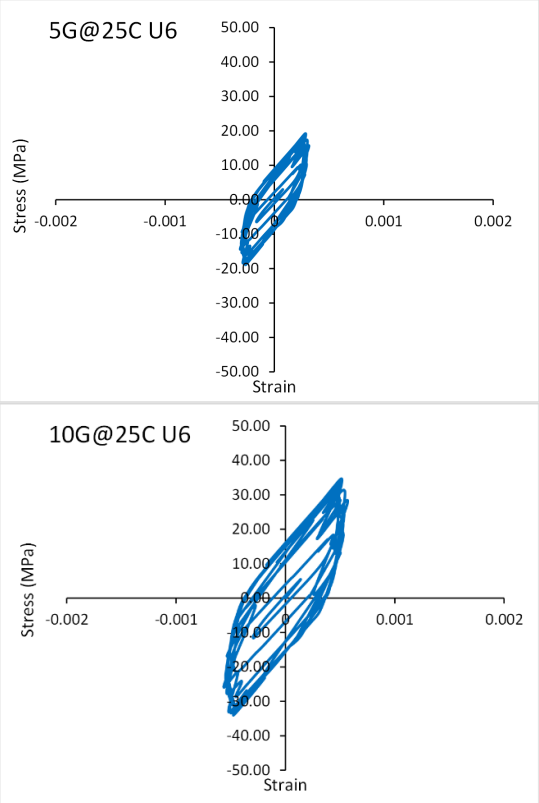


Figure 57: Extracted Hysteresis Loop of Critical Solder Joint (U6 @ 25°C @ 5g and 10g).

LIFE DATA ANALYSIS

All the packages on test board are daisy-chained before testing. A high-speed data acquisition is used to continue to monitor the resistance change in packages. The 20-percent increase for continuously 20-cycles in resistance is considered as a failure of package. The cycles to failure have been calculated by multiplying the time-to-failure by frequency of base excitation, which is constant throughout the test. Two-parameter Weibull analysis has been used to analyze failure data. Equation (3) is cumulative distribution function, which is used to compute characteristic life of packages. Cycles to failure are different for each package due to different strain amplitude at different locations. Due to symmetry of test board, four different locations have been analyzed (U1, U2, U5, U6).

$$F(t) = 1 - e^{-\left(\frac{t}{\eta}\right)^{\beta}} \quad (3)$$

where t is time, is η characteristic life, β is the shape parameter. Figure 60 show the Weibull plots of packages at three locations (U1, U2, U6) and three temperatures (25, 55, 155 °C) at 5G for SAC305.

Table 6: Characteristic Life

SAC305 at 5G			
Component	**25°C**	**55°C**	**155°C**
U1	8933149	4698845	3680046
U2	3224010	1883862	1404801
U6	2197947	989739	568038

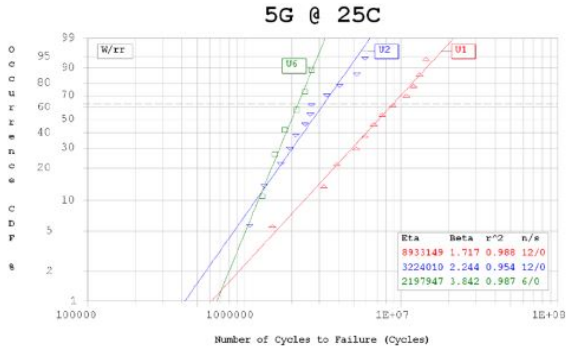


Figure 58: Weibull Plot at 5g for SAC305 at 25°C.

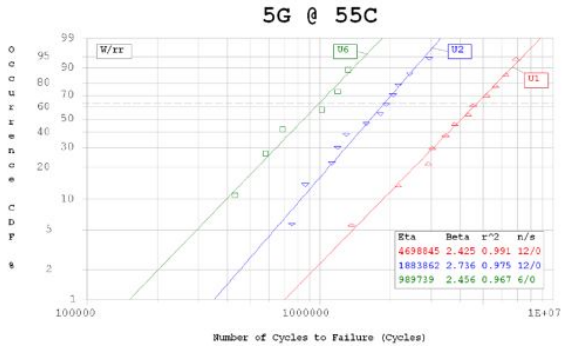


Figure 59: Weibull Plot at 5g for SAC305 at 55°C.

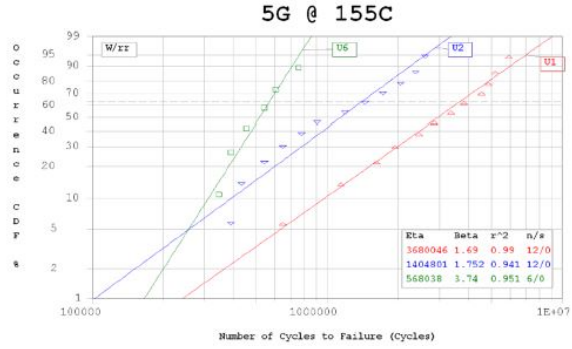


Figure 60: Weibull Plot at 5g for SAC305 at 155 °C.

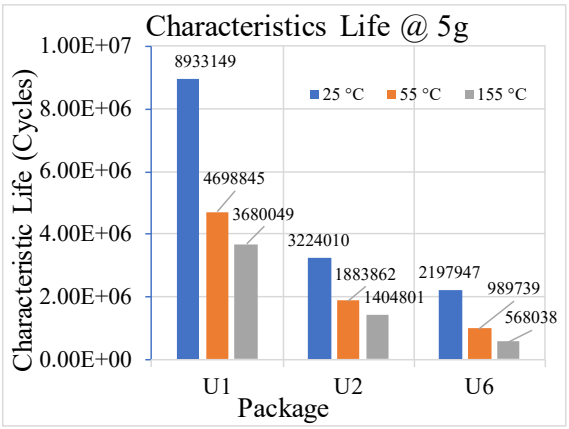


Figure 61: Characteristic Life for SAC305 at 5g.

Figure 61 and Table 6 shows the extracted characteristics life for CABGA288 packages from Weibull plots. Experimental data indicates that with the temperature increase, the characteristic life decreases. The characteristic life dropped

approximate 50-percent at various locations with the increase in temperature. The packages (U6 and U2) close to center of PCB have lower characteristic life compare to package (U1) far from center of PCB as shown in Figure 61. Package close to center of PCB fail faster due to more strain experienced by the package.

ENERGY BASED LIFE PREDICTION MODEL

Fatigue life has been computed using the energy-based method. The plastic work density has been used to estimate the damage to critical solder joint per bending cycle. When the accumulative plastic work density is larger than the threshold value of solder joint, it leads to failure in second-level interconnect. Power law equation has been used to predict fatigue life of solder joints as shown in Equation (4).

$$N_f = a.\left(\Delta W_{ave}\right)^{-b} \quad (4)$$

Where N_f is characteristic life, ΔW_{ave} is the plastic work density accumulated per bending cycles, a is fatigue coefficient and b is fatigue exponents. Table 7 shows the plastic work density values at 5G for SAC305 test board. All those values are extracted from simulation.

Table 7: Plastic Work Density at 5g.

SAC305 at 5G			
ΔW_{ave}	**25°C**	**55°C**	**155°C**
U1	0.21	0.29	0.42
U2	0.38	0.41	0.67
U5	0.16	0.19	0.27
U6	0.42	0.53	0.84

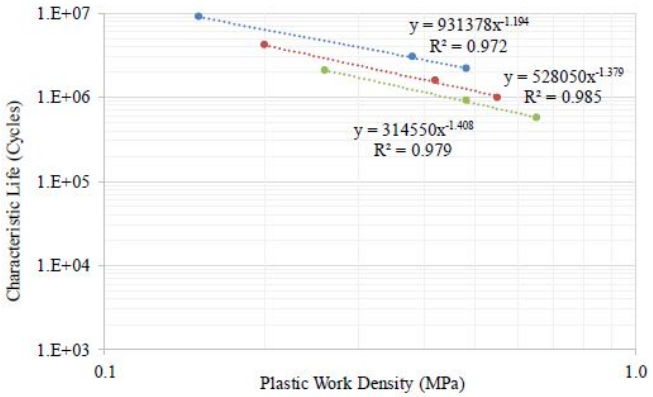


Figure 62: Characteristic Life vs Plastic Work Density.

Table 8: Fatigue Constants

Constants	**25°C**	**55°C**	**155°C**
a	931378	528050	314550
b	1.194	1.379	1.408

Characteristic life (N_f) vs. Plastic Work density (ΔW_{ave}) plot shown in Figure 59. Three curves have been generated at different temperature 25, 55, 155 °C. Equation (4) has been used to compute fatigue coefficient and fatigue exponent. Table 8 shows computed fatigue constant values from Figure 59 at various temperature. The fatigue constants and fatigue exponents have been extracted and plotted against operating temperature. Figure 60 shows fatigue coefficient and fatigue exponents vs operating temperature. Arrhenius equation has been used to investigate the temperatures effect on fatigue constants.

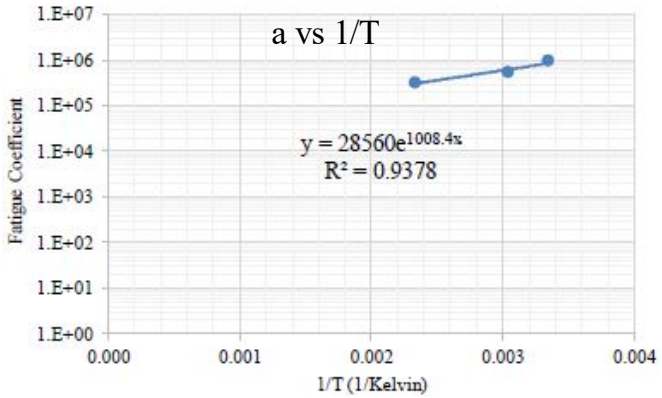
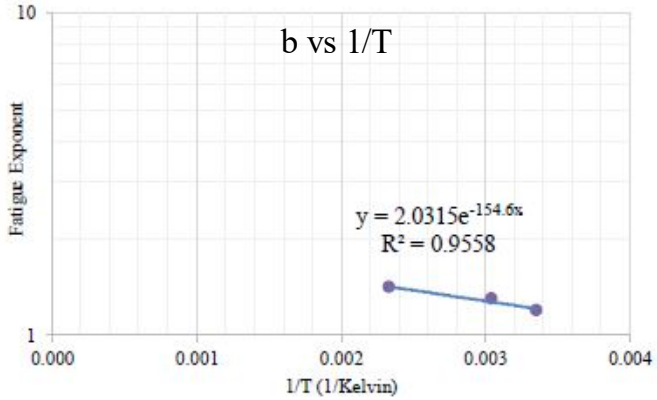


Figure 623: Fatigue Constants "a".



(b)

Figure 634: Fatigue Constants "b".

Equation (5) and Equation (6) show fatigue coefficients and fatigue exponents in terms of temperature. Fatigue coefficient decreased with increase in temperature, while fatigue exponents increased with increase in temperature as shown in Table 8. Fatigue life prediction model can be described as Equation (7).

$$a\left(T\right) = 28560.e^{\frac{1008.4}{T}} \quad (5)$$

$$b\left(T\right) = 2.0315.e^{-\left(\frac{154.6}{T}\right)} \quad (6)$$

$$N_f = \left(28560.e^{\frac{1008.4}{T}}\right).\left(\Delta W_{ave}\right)^{2.0315.e^{-\left(\frac{154.6}{T}\right)}} \quad (7)$$

Equation (7) can be used to predict the fatigue life of solder joint subjected to combined high operating temperature and vibration.

FAILURE MODE ANALYSIS

Failure analysis has been performed on CABGA288 after reliability test. Figure 61 shows the cross-sectioned image of critical corner solder joint after failure. Multiple failure modes have been observed. We observed that crack occurred at solder-copper interface on package-side and PCB-side as shown in Figure 61. Furthermore, it is observed that corner solder joints have a higher propensity of failure.

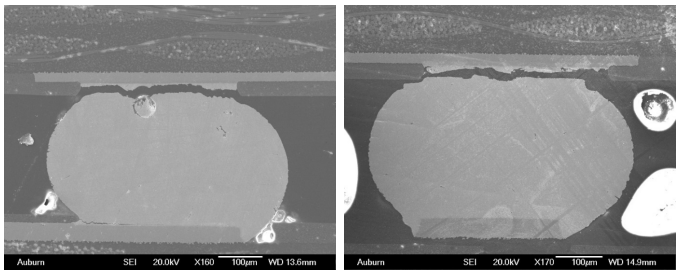


Figure 64: Corner solder ball from Package U6 and U7.

SUMMARY AND CONCLUSIONS

The reliability of test boards with SAC solder interconnects (SAC105 and SAC305) have been studied at different vibration G-Level and at elevated temperatures. The FEA based modal analysis and Experimental modal analysis have been conducted to determine the PCB characteristics such as natural frequencies, mode shapes. A good correlation was achieved between the experimental and FE based natural frequencies. Effect of operating temperatures have been studied and it was found that natural frequencies decreased with increase in the temperatures. Resistance data have been monitored using high speed data acquisition system till failure. Effect of Location of packages also has been studied and we found that packages at center location failed quicker compare to other locations due to higher strain at center of board. Anand Model has been used to describe the deformation behavior of critical solder joint. It was observed the maximum stress happened between the solder joint and copper pad. FEA based global and local method has been used to extract hysteresis loop and plastic work density of critical solder joint at different G-level and elevated temperatures. Effect of temperatures, locations of package and G-level have been studied on hysteresis loop. The area of hysteresis loop increased with larger input G-level and higher operating temperatures and package located at center of PCB has maximum area compare to other location due to larger displacement at center. Plastic work per cycle shows an increase with increase in G-level and operating temperatures leading to faster failure rate. Energy based Fatigue life prediction model has been developed for SAC solder materials during combined high operating temperature and vibration loads.

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