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Solder Paste Stencil Design for Optimal QFN Yield and Reliability

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Abstract
The use of bottom terminated components (BTC) has become widespread, specifically the use of Quad Flat No-lead (QFN) packages. The small outline and low height of this package type, improved electrical and thermal performance relative to older packaging technology, and low cost make the QFN/BTC attractive for many applications.

Over the past 15 years, the implementation of the QFN/BTC package has garnered a great amount of attention due to the assembly and inspection process challenges associated with the package. The difference in solder application parameters between the center pad and the perimeter pads complicates stencil design, and must be given special attention to balance the dissimilar requirements.

The lack of leads on the QFN/BTC package and the low standoff height result in significantly less compliance relative to other package types, making the QFN/BTC package more susceptible to CTE mismatch issues. Careful assembly of QFNs and proper printed circuit board (PCB) design can result in acceptable reliability depending on the overall design. One area that has not been well addressed, however, is the impact of die to package size ratio, and how this factor should be considered in circuit card assembly. IPC-7093 mentions the inverse relationship between relative die size and reliability, and Syed and Kang found the relationship to be non-linear, yet die size is seldom noted in component datasheets, and vendor recommendations do not include this ratio as a factor in assembly.

In this study, the volume of solder used in assembly of two QFN/BTC packages will be varied to investigate the relationship between standoff height and thermal cycle life, and to determine acceptable process limits with respect to first-pass yields. The QFNs selected have dissimilar die to package size ratios to assess the impact of this factor on the process window. Solder joint defect levels and thermal cycle results will indicate the ability to adjust manufacturing parameters to achieve a balance between the two objectives of process yield and reliability. The results will define a process window that provides the optimal installation of these packages.

Introduction
A wealth of information is available for optimizing PCB design and assembly for QFN packages, and this industry knowledge has been well cataloged in IPC-7093 [1]. This guideline reflects the recommendations found in many of the major component vendor application notes [2-8]. These documents all agree with respect to the typical target conditions for the solder joint; a standoff height of 2-3 mils, which is generally achieved by printing 1:1 on the perimeter lands and with a 20%-50% reduction of solder paste coverage on the center pad (although some vendors give more specific recommendations within this range of solder reduction on the center pad). These parameters will generally provide a high first-pass yield while providing for a relatively robust joint. The trade-offs for adjusting solder paste are also often mentioned; decreasing the volume of solder paste can reduce solder defects such as bridging but can negatively impact reliability, while increasing solder volume can do the opposite. Significant increases to the solder volume, however, can cause the component to float, potentially creating opens or misalignment.

One QFN/BTC property that is briefly mentioned in IPC-7093 and which been demonstrated to have a significant impact on QFN reliability is die size, or die to package ratio [9-11]. Component datasheets do not typically include information on the size of the die, but a sample of QFNs from several component vendors exhibited die to body ratios ranging from 0.27 to 0.58.

For the circuit card assembler, most of the decisions related to ensuring the best potential reliability of the QFN package have already been determined through design of the component package itself and of the PCB footprint. Once the design makes it to the point of assembly, the assembler has limited options to impact reliability, and these

are dominated by stencil design (to affect standoff height and solder joint configuration). Standoff height can be controlled in several ways (bumping, use of preforms, stencil modification). Although standoff height is one of the standard recommendations from IPC-7093 and component vendors (2-3 mil), fillet formation is also recommended [10-13]. Kim et al. [12] concluded that a large fillet was preferred when increasing stand-off height of the component which was achieved at the expense of the fillet size.

Given the number of characteristics related to QFNs and their implementation that can impact reliability, it is unclear whether an assembler can apply a standard set of rules for installing QFNs onto a PCB, or if they must be evaluated on a case by case basis. Should the assembler adjust stencil apertures based on other design criteria, or should the standard 20-50% reduction of solder on the center pad be followed regardless, and if so, what value in that range is most desirable? Or should a greater reduction of solder paste be applied such that stand-off height is sacrificed to ensure large, convex fillets?

In this study, two QFN/BTC packages were evaluated for robustness of solder joints relative to changes to solder joint height controlled by center pad solder paste reduction. Extreme levels of solder variation (outside of the typical 20-50% reduction) were employed to demonstrate the amount of influence this factor may have and the points at which assembly defects may become important.

Experimental Procedure

The PWB selected for this study is a commercially available QFN/BTC style package test board. The board is constructed of FR-4 epoxy laminate, is two-sided (although only one side will be used in this study), is 0.062 inch thick, and has a HASL finish over copper. Approximate X-Y CTE is 11-13 ppm/°C. Two QFN style component packages will be used. These components have daisy chain circuitry to match the PWB, and have the parameters shown in Table 1.

Table 1 - QFN Package Parameters (dimensions are mm)

Package	# of Contacts	Size	Thickness	Die Size	Die Thickness	Die / Body Ratio	Flag Size	Flag Thickness	Pitch
QFN44	44	7 x 7	0.85	2.5	.2	.35	3.4	.2	.5
QFN68	68	10 x 10	0.85	7.0	.2	.7	7.8	.2	.5

These two components were selected based on results of previous testing. The QFN68 package has a very high die to body size ratio, and has performed relatively poorly in other thermal cycle tests. The QFN44 package, however, has a low die to body size ratio, and in a previous test, there were no failures after 2520 thermal cycles. This testing will investigate the ability to improve results on a 'poorly' performing part, as well as the potential for reducing performance on a 'robust' part.

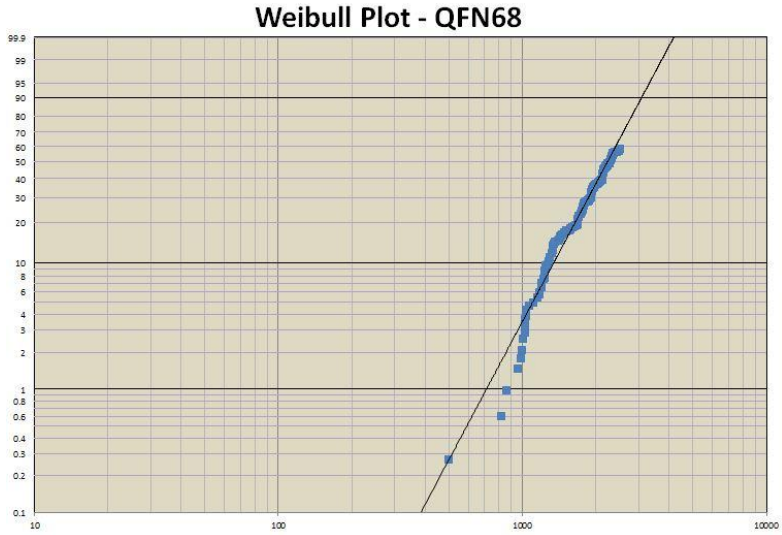

Figure 1 – Thermal cycling test results from a previous study on QFN68 package

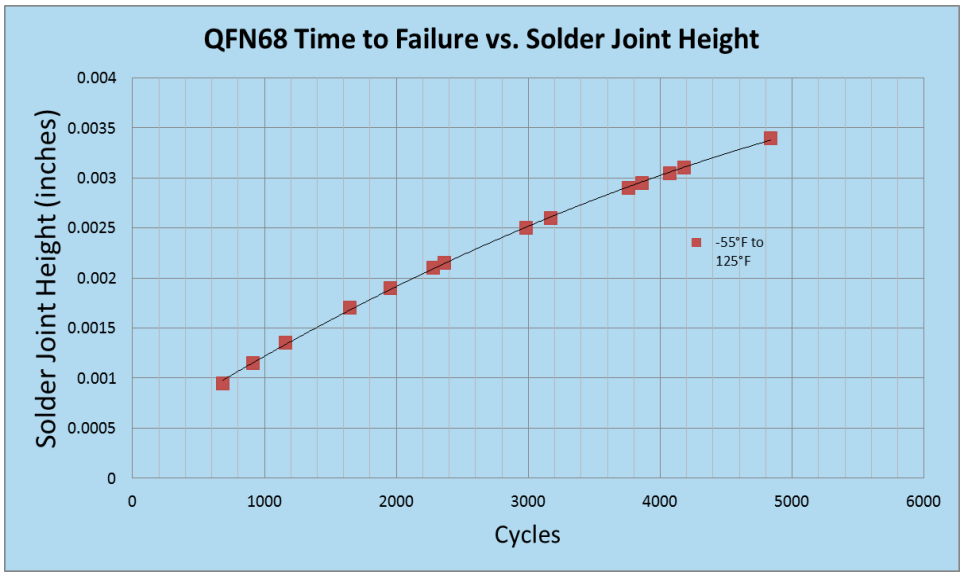

Figure 2 – Simulation prediction for QFN 68 installed at various solder joint heights. Previous testing calibration point indicated at 2.1 mil solder joint height and 2279 thermal cycles.

To develop an idea about how the chosen experimental parameters and variation would affect test results, a simulation software package was used to predict the outcomes of the testing. Figure 2 shows the results of that simulation and the prediction of the average thermal cycle survival period for the QFN68 package at the solder joint heights to be used in this test. Results of previous testing were used as a baseline to fit the prediction results to the test vehicle used.

A 5 mil stencil was used for solder paste application with apertures similar to those shown in Figure 3, but which varied by location on the board to control the volume of solder deposited at different sites across the assembly. The volume of solder was controlled by the number and size of apertures on the center pad of the QFN/BTC footprint. The volume of solder applied to the perimeter pins was also adjusted, with the objective of creating similar solder joints on all component locations (i.e. solder joint with the same amount of toe wetting and with similar fillet shape), although the height of these joints was different from location to location. Ten different aperture patterns were used for the QFN44 package, and 14 different aperture patterns were used for the QFN68 package. Reduction of solder on the center pad ranged from 10% to 90%. These values are outside of both the minimum and maximum recommendations, but are being evaluated to observe potential trends.

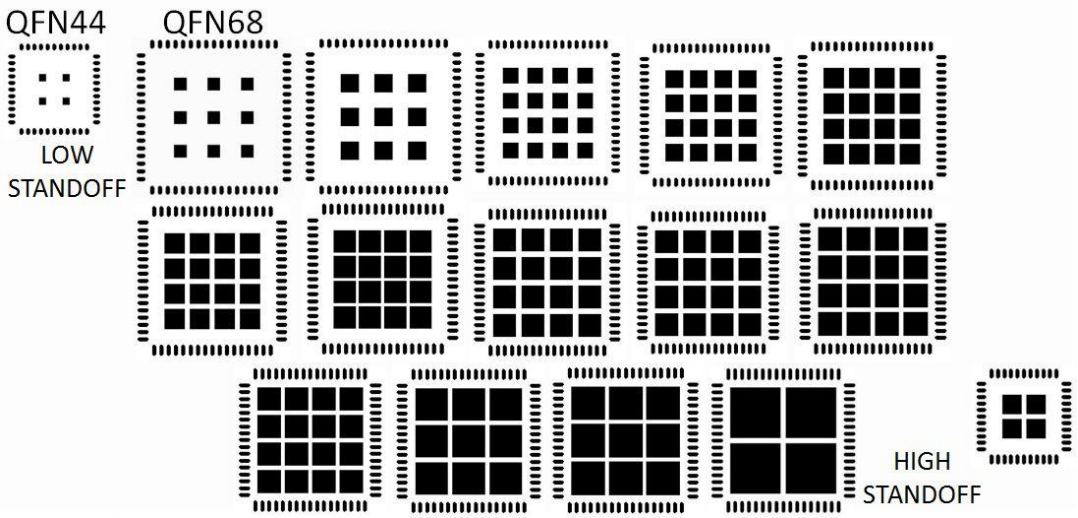

Figure 3 – Representative solder paste stencil apertures

Following automated stencil printing of the solder paste (Sn63Pb37), the QFN/BTC packages were machine placed on the solder paste deposits, the test vehicles were run through an in-line convection reflow oven, and then washed in an aqueous in-line cleaner. A typical ramp-soak-spike (RSS) reflow profile was used. Completed assemblies were inspected using X-Ray for bridging and the level of voiding was evaluated, and then continuity tests were performed to check for opens.

One assembly was cross-sectioned to evaluate solder joint heights, and the rest were subjected to thermal cycling. The assemblies were continuously electrically monitored during testing to identify when component failures occur. An air-circulating environmental chamber and a thermal cycle of -55°C to 125°C were used. The chamber includes a continuous recording unit for temperature. The ramp rate was set to 4.5°C/min and the dwell time set to 15 minutes.

An electrical continuity monitor was used determine time of failure for individual components. Testing was performed in accordance with IPC-SM-785 standard, with failures identified as short duration, high resistance spikes as described in section 4.3.1 of that guideline. Variations in channel current-loop resistance which exceed the selected threshold resistance were flagged as events, subject to the minimum event duration limit.

Results

Thirteen cards were built with a total of 20 QFN44 and 28 QFN68 packages on each card. Table 2 shows results from cross-section measurements, x-ray inspection, and continuity check. Several points are evident from these results. The first is that 'open' defects were present in the QFN68 locations where the least amount of solder reduction was applied. The QFN44 package did not exhibit any of these open defects. Bridging was not a common problem, but seems to have occurred randomly.

Table 2 – Solder joint results

Package	Site Name	Solder Reduction	Solder Joint Hgt. (mil)	Average Void %	Solder Opens	Solder Bridges
QFN44	A1	90%	1.0	5.3	0	0
QFN44	A2	85%	1.1	4.9	0	0
QFN44	A3	80%	1.2	4.7	0	0
QFN44	A4	75%	1.4	4.7	0	0
QFN44	A5	70%	1.7	5.7	0	0
QFN44	A6	60%	2.1	7.7	0	0
QFN44	A7	50%	2.6	10.8	0	1
QFN44	A8	40%	2.6	9.0	0	0
QFN44	A9	30%	3.2	9.9	0	0
QFN44	A10	20%	3.3	6.5	0	1
QFN68	B1	90%	1.0	10.2	0	0
QFN68	B2	80%	1.**2**	4.0	0	0
QFN68	B3	70%	1.4	3.8	0	1
QFN68	B4	60%	1.9	4.1	0	0
QFN68	B5	50%	2.1	4.0	0	0
QFN68	B6	50%	1.7	4.5	0	0
QFN68	B7	40%	2.2	3.9	0	0
QFN68	B8	35%	2.5	6.9	0	0
QFN68	B9	30%	2.6	5.8	1	0
QFN68	B10	25%	3.1	6.3	1	0
QFN68	B11	25%	2.9	6.2	1	0
QFN68	B12	20%	3.1	6.0	4	0
QFN68	B13	15%	3.0	6.0	8	0
QFN68	B14	10%	3.4	6.8	8	0

Voiding levels were fairly low. Only three locations had total voiding above 25%, and some of these were attributed to 'bottoming-out' of the component on the solder mask at B1 sites. It was determined that the solder volume at these sites was low enough such that some parts were resting on the solder mask, which enabled voids to remain in the solder joint instead of making their way out.

One test board was selected for cross-sectioning to evaluate solder joint heights and geometry. Figures 4 and 5 are representative images of the solder joints formed. On components with a larger stand-off height (i.e. taller solder joints), the solder at the toe is slightly concave in shape, while it is convex on the parts with a lower stand-off. This demonstrates that the sizing of the stencil apertures at the perimeter pin locations was not quite compensated enough to achieve consistent fillets at all locations. Solder joint open defects were reworked by hand and were tied in for thermal cycle testing, although the locations were noted for future reference to determine the impact that rework may have on reliability.

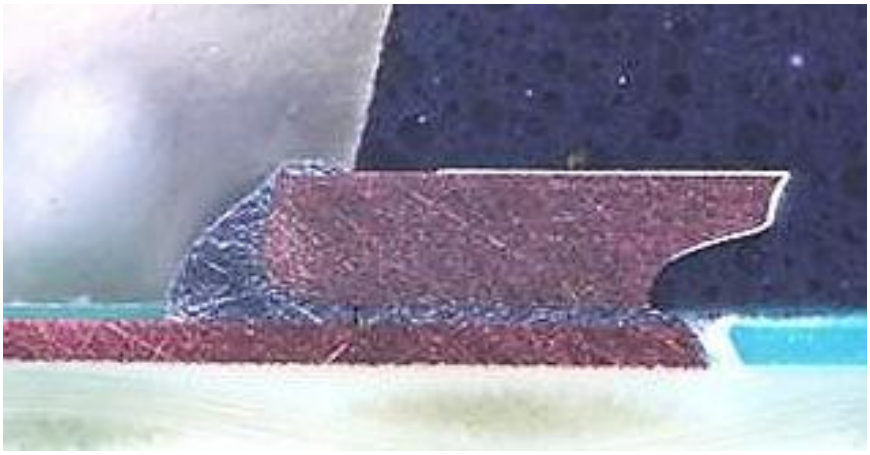

Figure 4 – QFN68 with 1.0 mil standoff height (Site B2)

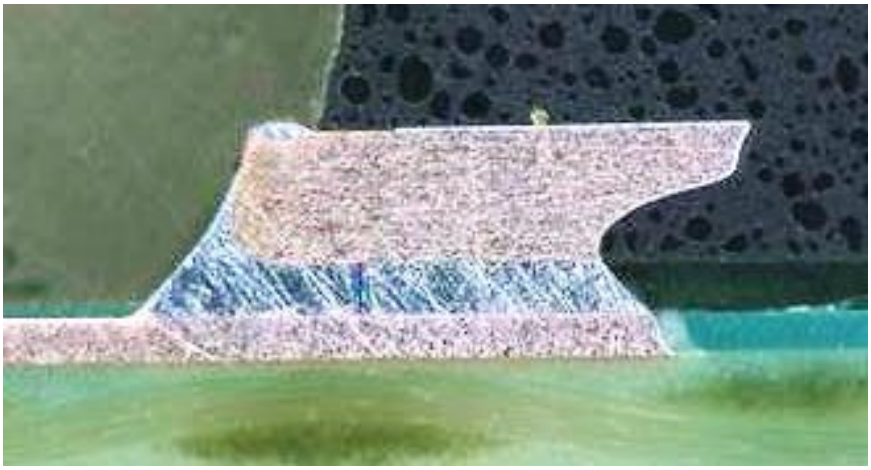

Figure 5 - QFN68 with 2.8 mil standoff height (Site B13)

Solder joint height for the QFN package is generally defined by the amount of solder applied to the center pad. In this study, the PCBs used had a HASL finish, so they have some volume of solder already present on the center pad. Cross section measurements of the solder joint height (actual height) were compared to the expected values at each location, as seen in Figure 6. This data demonstrates a good trend, and variation seen is attributed to three main variables; pre-existing solder volume from HASL, solder volume applied in-process, and variation of the QFN position in the cross-section (i.e. potential tilt of the package).

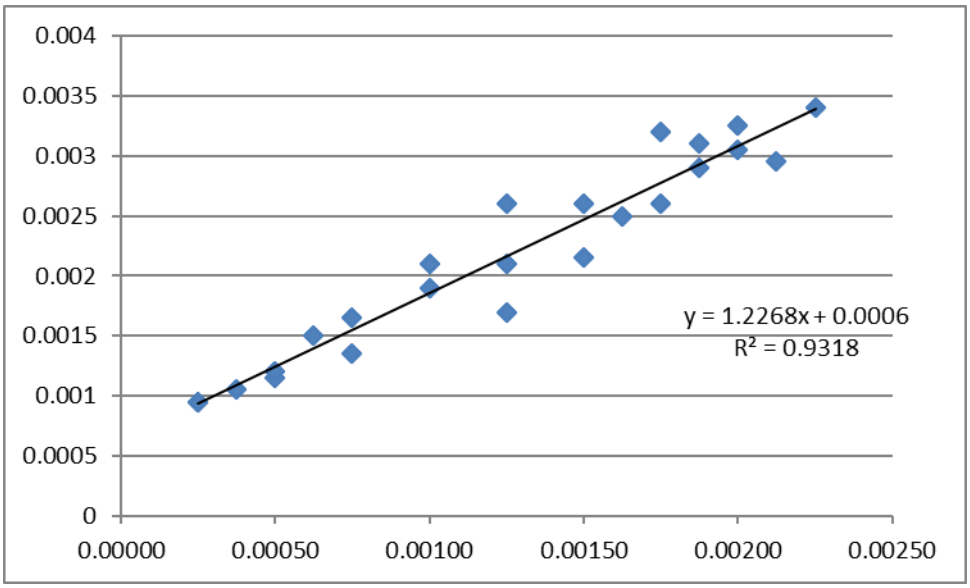

Figure 6 – Solder joint height; expected vs. actual (inches)

To date, the test vehicles have been exposed to 1100+ thermal cycles (-55°C to 125°C), with the profile as shown in Figure 7. There have been only four failures out of the 576 locations thus far. These failures have each been from a QFN68 package of a unique site, but none of these sites were those with greater than 50% solder reduction (the standard lower limit for paste application.)

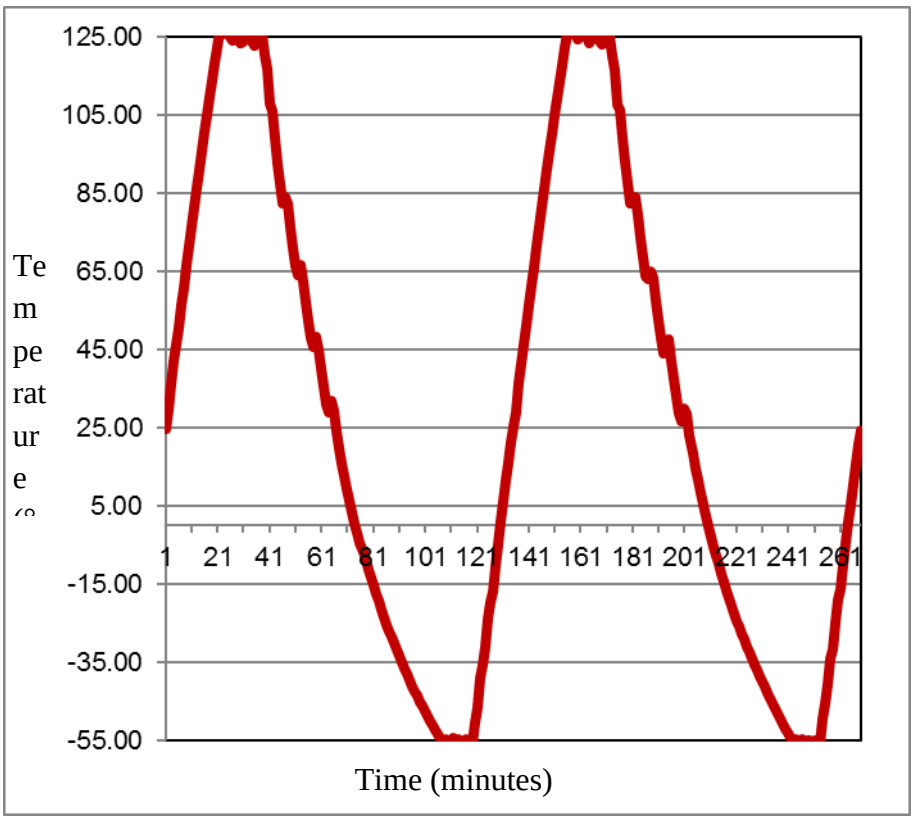

Figure 7 – Thermal cycle profile of test vehicles

Review of the component x-rays resulted in the observation of a property that was not originally of concern, and which was only partially observed in the process yield results; solder joint consistency. When the solder paste

volume is increased on the center pad, the increased standoff height results in less consistency in the perimeter pin solder joints. Figure 8 shows a typical x-ray image of a QFN68 from site B12, where the variation in solder joint volume is clearly seen, although this location passed continuity testing. A similar image from a B5 location shows much more consistent solder joints around the perimeter of the part. By comparison, the solder joints for the QFN44 (see Figure 9) are fairly consistent regardless of component standoff.

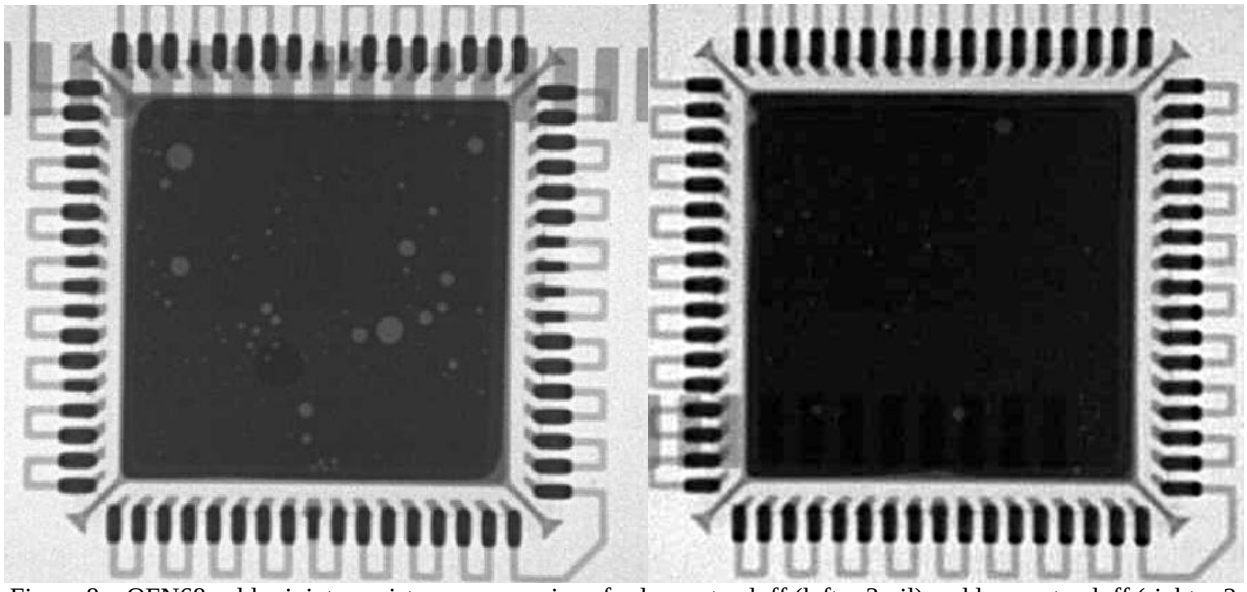

Figure 8 – QFN68 solder joint consistency comparison for large standoff (left, ~3mil) and lower standoff (right, ~2 mil)

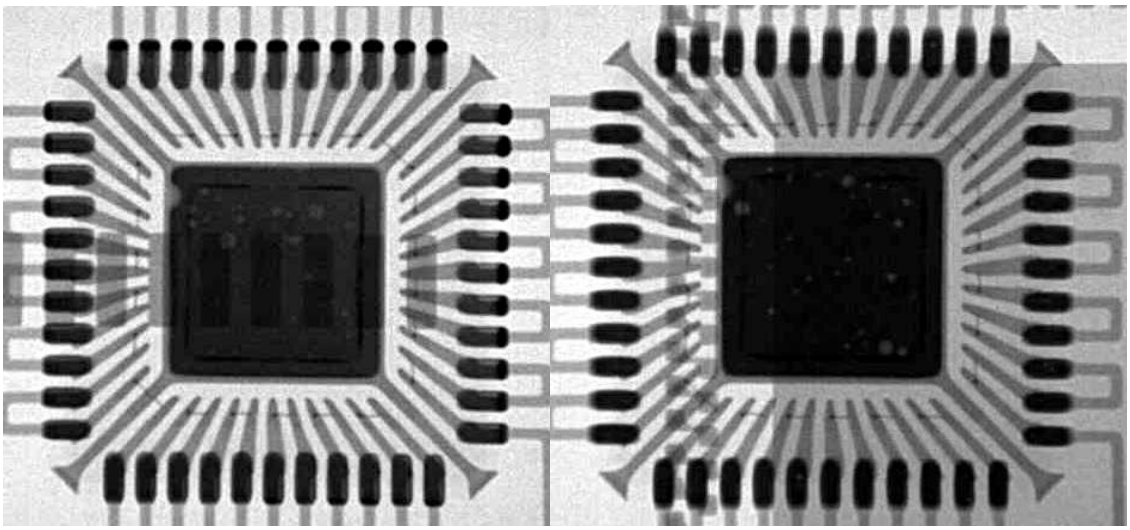

Figure 9 – QFN44 solder joint consistency comparison for large standoff (left, ~3mil) and lower standoff (right, ~2 mil)

Conclusions

Two QFN/BTC packages were installed onto representative circuit cards using a variety of solder paste applications. Many of the standard guidelines for QFN/BTC application and soldering were followed, with only the solder paste volume adjusted to control the resulting solder joint height and geometry. Actual solder joint height for this assembly was shown to correlate well to expected solder joint height according to the stencil design.

In general, an increase in the amount of solder paste used resulted in an increase in the amount of voiding. This is expected, as the pathways for volatiles to escape are reduced and the overall amount of volatiles is increased as the total solder volume increases. Voiding was low in general, with few instances of voiding exceeding 25% of the soldered area.

Thus far, the failure rates for the various solder joint configurations (height) are not as predicted by the simulation software. Of particular note is the inconsistency of the solder joints on the QFN68 packages at increased solder joint heights. The joints seen in the Figure 8 above make electrical connection, but may represent weak joints that are likely to fail relatively early. This joint variation in the previous testing could have skewed the simulation baseline, and therefore the current prediction, which likely assumes that every joint is exactly the same within the programmed parameters. Another potential impact that could be impacting thermal cycle survivability is the slight change in the solder joint shape at the toe fillet. The solder stencil was adjusted to vary the amount of solder paste applied at the perimeter pins, resulting in solder joints that had very similar geometry, but which were not exactly the same. The slightly larger solder joints on the locations with a shorter solder joint height could improve the thermal cycle survivability. The simulation software did not allow the size or shape of the toe fillet to be adjusted.

Until more failure data is collected, specific conclusions cannot be substantiated, but the observations and results so far indicate that center pad size (and presumably die to package ratio) should not be ignored when implementing QFNs. There were clear differences in the results between the two packages used in this study. Components with a small center pad are relatively robust not only in thermal cycling, but also with respect to yield and consistency in the manufacturing process. Components with a large center pad require more attention, as they have a smaller process window for optimal solder joints, and have reduced reliability. Initial results indicate that such a component is best installed with 50% or more in solder paste reduction on the center pad, but more failure data is required to determine the ideal stencil design.

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