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# SILICON V-GROOVE ALIGNMENT BENCH FOR OPTICAL COMPONENT ASSEMBLY

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## ABSTRACT

One of the primary technical challenges associated with the manufacture of optical assemblies, especially systems with higher levels of integration, is component to component optical alignment. Components must be brought into precise spatial relationship and the precision of this alignment must be captured and maintained throughout the useful lifetime of the assembly. The alignment step can be done actively or passively. The active approach is more complicated involving powering up devices and measuring optical coupling results while moving the components into the aligned position. The passive approach relies on building precision into the parts so that they can be directly assembled into the aligned position without activating the components. This paper describes the use of a large V-groove wet etched into a silicon wafer to form an alignment bench component, which can be used in combinations with silicon based interposer / photonic integrated circuit (PIC) die and either additional similar die, or optical fibers assembled with cylindrical ferrules such as the LC connector ferrule. The silicon interposer die / PIC die are constructed with wet etched v-grooves along the locations where the die will be diced. This allows the sidewalls of these edge locator grooves to be used in combination with the alignment bench to precisely position features on the die relative to other similarly constructed components or optical fibers. The accuracy achieved by the photolithographic processes employed allow passive alignment to be used for constructing these assemblies.

Key words: Active Alignment, Passive Alignment, Silicon Interposer (SI), Photonic Integrated Circuit (PIC), Wafer-Scale Processing, Wide Alignment Groove (wag), LC Connector Ferrule, lC Connector Assembly, Laser Fiber Endface Cutting, Through Silicon Via (TSV), Chip-to-world Interconnect, Bi-directional Optical Transceiver

## INTRODUCTION

Photolithographic methods provide extremely precise features on parts produced in foundries established for the processing of silicon wafers. Features such as solder pad arrays that are designed for flip-chip mounting can provide accurate positioning of electrical and optical die in addition to electrical and thermal interconnections to these die. Silicon Interposer (SI) die or Photonic Integrated Circuit (PIC) die incorporating such features can provide a number of sophisticated functions per die. In this paper, an approach will be prsented that uses wet etched v-grooves along the sides of Silicon Interposer / PIC die. These side locator alignment surfaces are used when assembling these die to a standard optical fiber connector front end. A precision alignment bench formed as a Wide Alignment Groove (WAG) that has been wet etched from a crystalline silcon wafer forms the base for the assembly. In this paper, a Silicon Interposer is described that provides electrical interconnects to an edge emitting laser die and a laser monitor detector die. The electrical interconnects for the SI described in this paper are formed using a process developed at MA/COM for their glass microwave integrated circuits (GMIC process). It involves etching pockets into the silicon wafer and then filling the pockets with glass frit material. Further processing of the wafer produces a surface with areas of glass and areas of silicon. The metallic electrical traces for this SI are run on the glass material areas in order to provide high frequency impedance control and dielectric isolation from the silicon substrate. Through Silicon Vias (TSVs) are used to interconnect the top surface pads of the SI to the bottom surface ground layer to provide top surface grounds where needed.

The electrical connections on the back end of the SI can be bonded to an electrical flex circuit for interconnection to a printed circuit board. The laser die on the front end of the SI is passively aligned to the solder pad array features when the solder is reflowed. The solder pad array features are accurately positioned relative to the SI wet etched sidewall alignment features. These sidewalls are aligned to a standard optical fiber connector sub-assembly by the WAG. In this case, the connector is an LC connector. The resulting assembly forms a chip-to-world interconnect that is small in size, offering a high speed packaging approach. The Silicon Interposer / PIC to standard LC connector receptacle sub-assembly alignment approach is shown in Figs. 1 & 2.

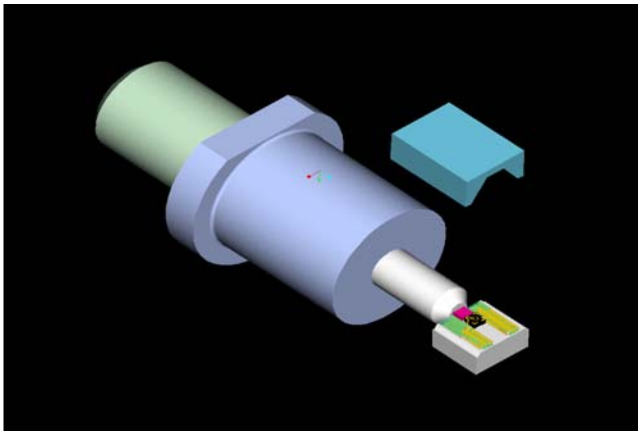


**Figure 1.** Silicon Interposer / PIC to standard LC connector receptacle sub-assembly alignment using Wide Alignment Groove (WAG).

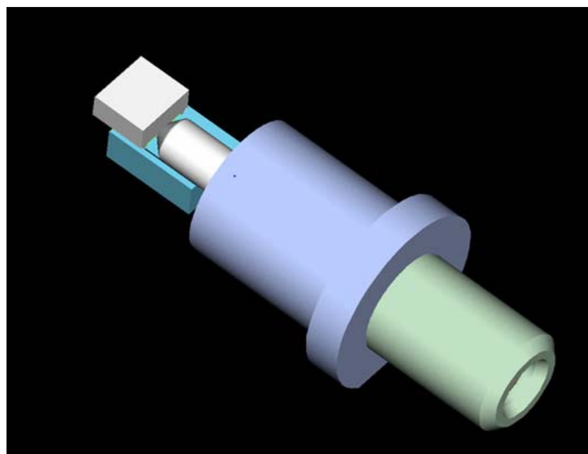
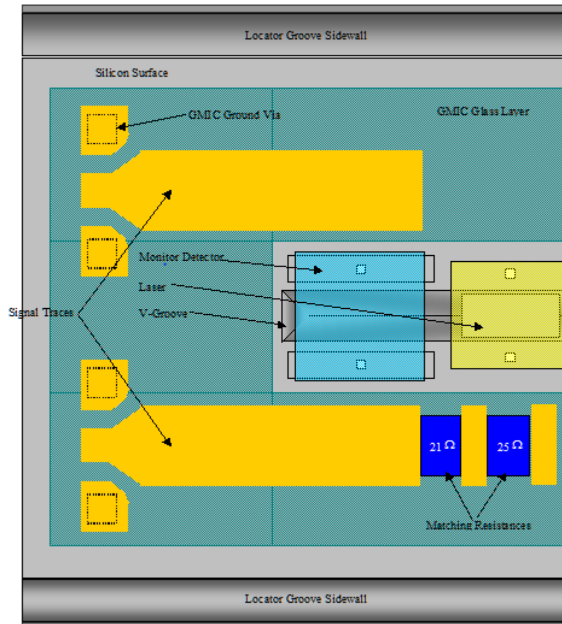


**Figure 2.** Wide Alignment Groove (WAG) is used to accurately position and provide stability to assembly.

## SILICON INTERPOSER (SI)

TE Connectivty, (formerly Tyco Electronics, a part of Tyco International) acquired AMP Inc. in Harrisburg, PA & Somerville, NJ and M/A-COM in Lowell & Burlington, MA) who developed a manufacturable process for mounting opto-electronic flip chip die onto GMIC silicon wafers. This work was presented at the Electronic Components and Technology Conference in 2001 [1]-[2]. US Patent 6,625,357 assigned to Tyco Electronics Corporation claims methods to fabricate devices having either mechanical seating or visually aligned fiducials. It also claimed the method of using matched solder metal pad arrays on the flip chip laser or detector die and on the silicon interposer for passive solder reflow alignment [3]. This invention was extended to include additional methods as well as other product configurations that use matching solder metal pad arrays on the flip chips and the silicon wafer as described in US Patent 6,933,536 assigned to Tyco Electronics Corporation [4]



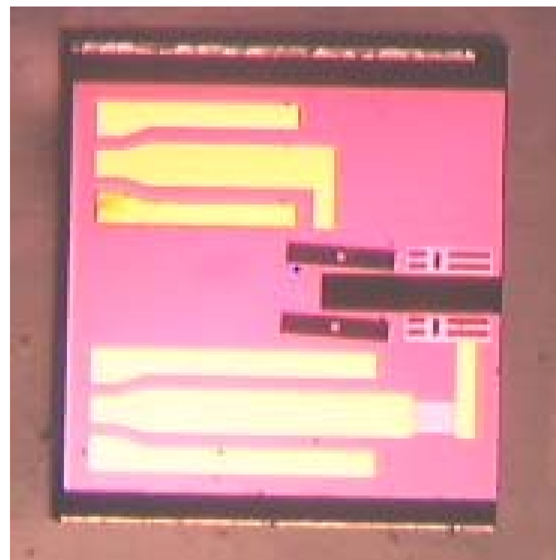



**Figure 3a and 3b.** Silicon Interposer for laser and monitor detector with locator groove sidewalls.

Passive die alignment using Gold / Tin solder reflow was presented at the 2003 M/A-COM Engineering Conference as an internal Tyco Electronics publication [5]. Figure 3 shows the metal pad array configuration for an edge emitting laser die and a laser monitor detector die. The signal traces for the high speed laser die include impedance matching resistors and are placed onto the glass sections of the GMIC wafer. The laser is flip chip mounted to the metal pad array in a silicon section of the GMIC wafer. Through silicon vias connect the top side ground pads to the ground plane back side of the SI. The LC connector sub-assembly as shown in Fig. 4 can be prepared with a fiber endface that has been polished or prepared by laser cutting as described in ref.[6].

**Figure 4.** LC Connector Sub-Assembly

The Wide Alignment Groove (WAG) is produced by wet etching arrays of grooves into a crystalline silicon wafer as shown in Fig 5 and dicing into individual parts as shown in Fig 6. It is very important to accurately align the etching mask to the crystal axis in the wafer in order to avoid the production of crystal plane steps on the large sidewalls of the WAG [7]. It is also important to control the etch process parameters in order to avoid the production of hillocks on the surface of the etched silicon for such large sidewalls.

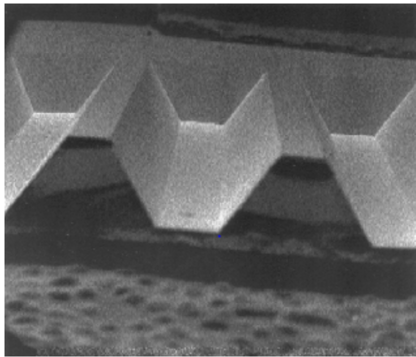


**Figure 5**. Wide Alignment Groove (WAG) array

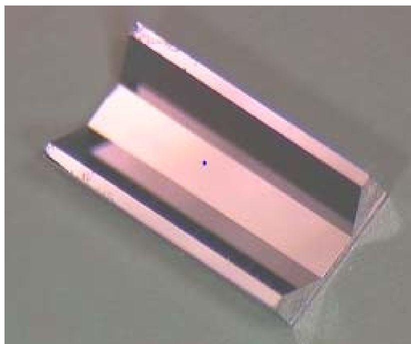


**Figure 6**. Diced Wide Alignment Groove (WAG)

**ALIGNMENT OF LC FERRULE TO SI USING WAG**

As shown in Fig 7, an LC connector sub-asembly is placed into the large WAG and the exposed LC ferrule contacts the WAG sidewall surfaces in 2 lines that accurately position the center axis of the LC ferrule in the WAG. The SI shown in Fig 8 is constructed with it's alignment sidewalls accurately placed about the metal pad array that positions the edge emitting laser die. When the spacing of the alignment sidewalls is chosen correctly, the centerline axis of the edge emitting laser die is positioned co-incident to the center axis of the LC ferrule. This alignment can be achieved to high precision using the crystal plane wet etching of the two silicon parts. This alignment mechanism is described in detail in US 7,511,258 assigned to Tyco Electronics Corporation [8]. This true position optical bench interconnection approach enables optical fibers to be interconnected to electro-optical chips that are flip chip mounted onto SI substrates with a high degree of precision. This type of interconnection has been termed Chip-to-World Interconnect since the distances of transmission enabled by the optical fiber can in fact span the world.

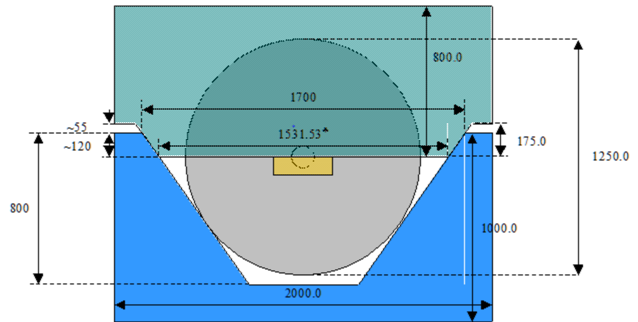



**Figure 7.** LC Ferrule to SI Locator Groove Sidewalls aligment using WAG

**Figure 8.** LC Ferrule Sub-Assembly aligned to SI using WAG

**THE LC CONNECTOR-TO-SI ASSEMBLY CAN REDUCE THE SIZE OF TRANSCEIVERS CURRENTLY BUILT WITH TOSA AND ROSA ASSEMBLIES**

The LC connector-to-SI assembly approach can bring a significant reduction in size to an optical transceiver when compared to optical transceivers built using conventional TOSA and ROSA assemblies that are based on hermetic TO-Can packaging. The electrical connections on the back end of the SI can be bonded to an electrical flex circuit for connection to a printed circuit board. The laser die on the front end of the SI is aligned to a standard optical fiber connector sub-assembly. In this case, the standard

connector is an LC connector interface. The result is a chip-to-world interconnect that is small in size and low in cost while offering a high speed package with improved optical coupling efficiency.

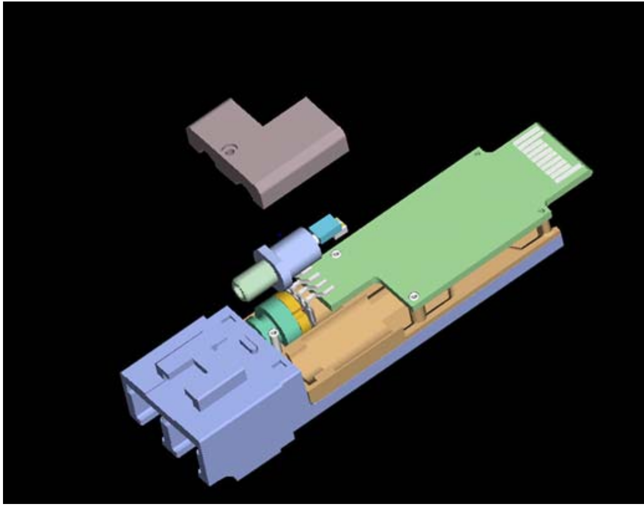


**Figure 9.** LC Connector-to-SI Assembly comparison to TOSA and ROSA based transceiver packaging

The exploded view of the LC receptacle assembly as shown in Fig. 10 uses a conventional split sleeve to align the LC ferrule component included in the receptacle assembly to the ferrule from the LC cable connector. The standard LC cable connector is shown in Fig 11. A typical optical transceiver will use 2 separate fibers for the send and receive directions, so there are 2 LC cable connector receptacles on the front end of the transceiver as shown in Fig 9. If the SI / PIC includes the capability to do wavelength division splitting and routing, a single Bi-Directional (Bi-Di) optical transceiver device can be formed. In this case, only a single LC connector front end receptacle is required per Bi-Di transceiver.

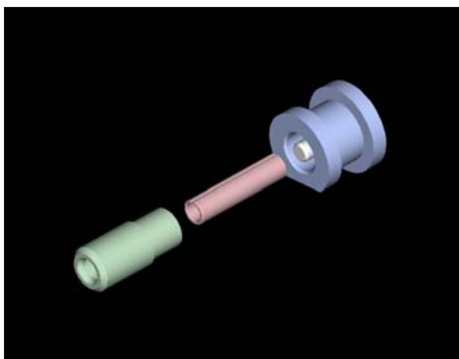


**Figure 10.** Exploded view of LC receptacle assembly

**Figure 11.** Standard LC cable connector

**SILICON INTERPOSER-TO-SILICON INTERPOSER SILICON INTERPOSER-TO-PIC INTERCONNECTS**

The WAG can also be used to align 2 or more SI components to each other to construct a complex device, or it can be used to align a SI component to an already complex PIC component. The only requirement is that the SI and PIC components must be produced with corresponding locator groove sidewall width and orientation to the coupled optical object positions. As an example of one of these additional SI configurations, arrays of optical waveguides on a first SI component can be aligned to a second array of optical waveguides or an array of optical fibers as shown in Fig 12. Such array Sis can greatly increase the interconnect density between components. When combined with dense wavelength division multiplexing on each optical waveguide, it is possible to envision 10's of Terabits of bandwidth interconnect between such components using this approach.

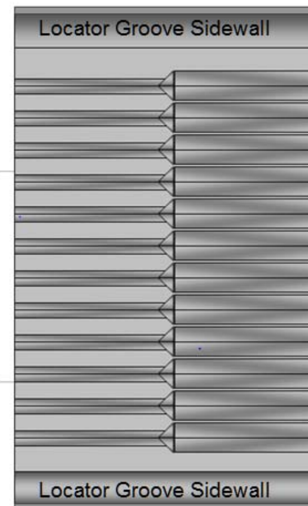



**Figure 12.** SI to position an array of optical fibers

## CONCLUSION

The use of a Wide Alignment Groove (WAG) that is wet etched from a silicon wafer to form an alignment bench component has been presented. The WAG, is used to align a combination of components such as a Silicon based Interposer (SI) / Photonic Integrated Circuit (PIC) die to either additional similar die, or to cylindrical ferrule connector receptacle sub-assemblies such as the LC connector ferrule receptacle sub-assembly described here. The silicon interposer die / PIC die are constructed with wet etched locator v-groove sidewalls along the locations where the die are diced. The sidewalls are used in combination with the WAG to precisely position features on the die relative to features on other similarly constructed die or to optical fibers. The accuracy achieved by the photolithographic processes employed enable passive alignment to be used for the construction of these assemblies.

The Silicon Interposer described provided electrical interconnects to an edge emitting laser die and a laser monitor detector die. The electrical interconnects were formed using an advanced electrical interconnect process developed at MA/COM for their glass microwave integrated circuits (GMIC process). It involved etching pockets into the silicon wafer and then filling the pockets with glass frit material and processing the wafer to produce a surface with areas of glass and areas of silicon. The metallic electrical traces for this SI were run on the glass material areas in order to provide impedance control and dielectric isolation from the silicon substrate. Through Silicon Vias (TSVs) were used to interconnect the top surface pads of the SI to the back surface ground layer in order to provide top surface grounding.

One of the primary technical challenges associated with the manufacture of optical assemblies, especially systems with higher levels of integration, is the component to component optical alignment. The alignment step can be done actively or passively. The active approach is more complicated involving powering up devices and measuring optical coupling results while robotically moving the components into the optimum aligned position. The passive approach as described in this paper, relies on building precision into the parts using wafer scale photolithography. This approach provides component parts that can be directly assembled into the aligned position without activating the components. Once the components are brought into precise spatial relationship the precision of this alignment is captured and maintained throughout the useful lifetime of the assembly.

The resulting assembly provides a chip-to-world interconnect that can be automated to produce high volumes.

## ACKNOWLEDGEMENTS

AMP, M/A-COM, Tyco Electronics, and TE Connectivity are trademarks of Tyco Electronics Corporation

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