As originally published in the IPC APEX EXPO Conference Proceedings.

"Why Signal Always Be Loss in a High Speed High Frequency Transmission Line"

Albert Chen
Elite Material Co., Ltd.
Taiwan, ROC

Abstract:

The high speed transmission applications in the electronic product become inevitable developing trend. The signal integrity becomes the most important issue in the electronic industry. The material suppliers, PCB manufactures, OEM designer commonly face the serious issue "how to keep signal integrity operated in the high speed transmission" for the modern electronic application nowadays.

The material suppliers dedicated into developing lower dielectric constant and dissipation factor material, PCB manufactures define the low loss material and copper foil selection guide and more delicate process handling. The OEM specify the signal integrity form the insertion loss and extracted material Dk / Df from signal loss result . All of these are for keeping signal could be transmitted completely at higher bandwidth. We discuss the following factors affect insertion loss result in this paper , such as material Dk / Df , copper foil type , skin effect, impedance variation , line width , line space, black / brown oxide treatment, dielectric thickness , via stub effect and so on through TDR and VNA measurement and simulation analysis result .

We hope we could more understand the mystery of signal loss issue through these discussions and meet the signal loss specification from the OEM designer.

Introduction

Nowadays, we could easily find there are many modern electronic products using high speed technology around us, such as USB (universal serial Bus) and SATA (serial advanced technology attachment) for higher data rate transmission, HDMI (high definition multimedia interface) and display port for higher resolution on the multimedia. Besides that the handling frequency of Intel CPU processer double every two years. It means that PCB with low loss characteristic would play a very important role for high speed transmission application.

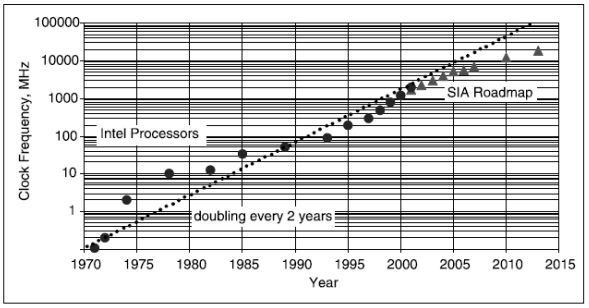


Figure 1 - Historical trend in the clock frequency of Intel processors based on years of introduction
(Source: Intel Corp and SIA (semiconductor Industry Association))

OEM signal integrity requirement review

For achieving more better signal integrity could be operated completely at higher frequency, OEMs specify their own methodology to identify the signal integrity in the form of insertion loss or extracted dielectric constant and dissipation factor from insertion loss.

Table 1 - Specific insertion loss evaluation by different OEMs

	IBM	Intel	Cisco
Methodology	SPP	SET2DIL	S3
Frequency concern	1GHz	4, 8GHz	10GHz
Impedance pattern	50 Ohms single end stripline	85 Ohms signal end to differential pair insertion loss	50 Ohms single end stripline
instrument	TDR	TDR	VNA
Purpose	Insertion loss and extracted Dk Df	Insertion loss	Insertion loss and extracted Dk Df

Others rely on VNA measurement for insertion loss/return loss by their own methodology.

Transmission line in PCB

It is known that ideal transmission line could be used following elements such as resistance, capacitance, inductance and conductance to stand for the transmission behavior at high frequency. The capacitance and inductance belong to energy storage elements; however, the serial resistance of copper resistance and shunt conductance from dielectric are energy loss elements in the transmission line. In the PCB, we use the microstrip and stripline structure to represent the transmission line with specified material property and geometry structure. In the signal attenuation discussion, the dielectric conductance and copper resistance are two main elements to cause signal loss at high frequency, since the dielectric conductance and copper resistance would varied with the frequency.

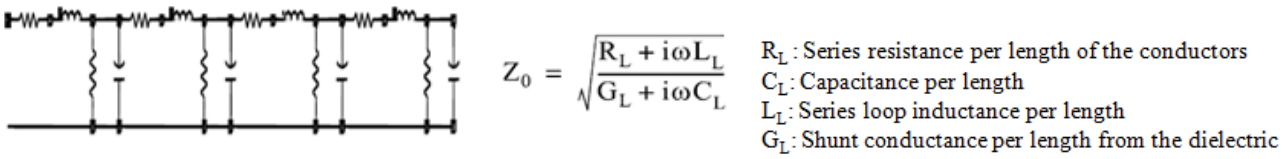


Figure 2 - RLGC model for an ideal lossy transmission line

Note:

1. In an ideal transmission line, R and G are energy dissipated element, L and G are energy stored element, R is the source of conductor loss, and G is the source of the dielectric loss.
2. The characteristic impedance of a lossy transmission line is shown as the above formula.
3. The RLGC value is related the material property and geometry.

The transmission line in a PCB stack up could be represented by following models; every model has specific formula for the

impedance calculation in a transmission line.

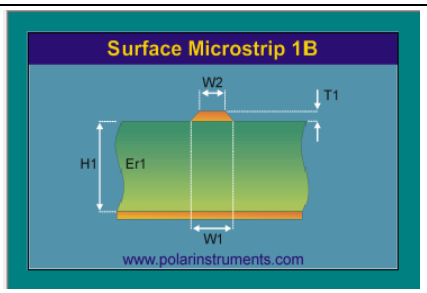
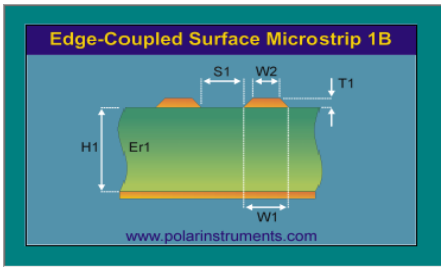
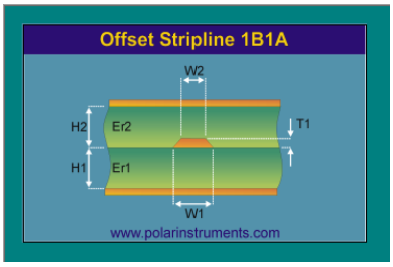
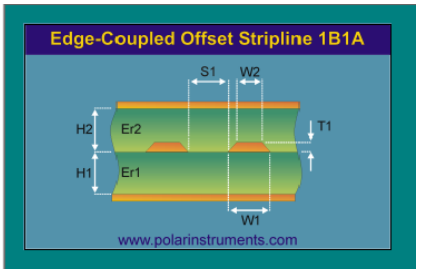
Microstrip single end	Microstripline differential pairs
	
Stripline single end	Stripline differential pairs
	

Figure 3 Typical Microstrip and Stripline structure for PCB (source: Polar Instruments Ltd)

In a multilayer board, a good transmission line should be well controlled that its characteristic impedance is constant everywhere down its length. If a controlled impedance board is that the characteristic impedance of all the traces meets a target spec value, typically 50 Ohms or 85 Ohms. Does it mean that it can always be having good quality all the time, especially for higher speed or higher frequency? The answer is depending on situation.

Why we get poor result of insertion loss sometimes?

Here is an example of 16L SI measurement, a PCB shop did a good controlled impedance board that the characteristic impedance of all the traces meets a target spec value of 85 Ohms. However the insertion loss value of every layer is exceeded -0.48db/in at 4GHz what they expect.

Layer	Coupon#1			Coupon#2			Coupon#3			Average		
	SDD21 (@4GHz)	SDD21 (@8GHz)	Impedance	SDD21 (@4GHz)	SDD21 (@8GHz)	Impedance	SDD21 (@4GHz)	SDD21 (@8GHz)	Impedance	SDD21 (@4GHz)	SDD21 (@8GHz)	Impedance
L1	0.506	0.914	90.3	0.532	0.927	86.8	0.506	0.904	89.3	0.515	0.915	88.8
L3	0.577	1.031	83.3	0.582	1.022	80.0	0.578	1.037	85.7	0.579	1.030	83.0
L5	0.550	0.963	83.4	0.546	0.961	83.1	0.547	0.969	86.3	0.548	0.964	84.3
L7	0.527	0.994	85.7	0.524	0.991	87.8	0.538	1.010	88.3	0.530	0.998	87.3
L10	0.524	1.001	88.0	0.533	0.978	88.5	0.524	0.989	86.8	0.527	0.989	87.8
L12	0.543	0.945	85.1	0.540	0.952	84.1	0.555	0.958	82.4	0.546	0.952	83.9
L14	0.569	1.023	85.0	0.570	1.014	89.9	0.579	1.025	83.5	0.573	1.021	86.1
L16	0.531	0.945	88.7	0.539	0.947	84.1	0.528	0.935	90.4	0.533	0.942	87.7

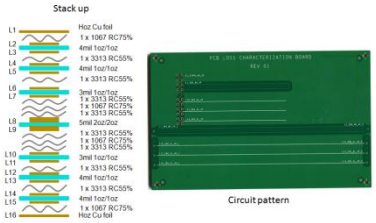


Figure 4 – 16L stackup, circuit pattern and measuring data

Elite Material Co., Ltd did following failure analysis in order to find out what's wrong in the measurement.

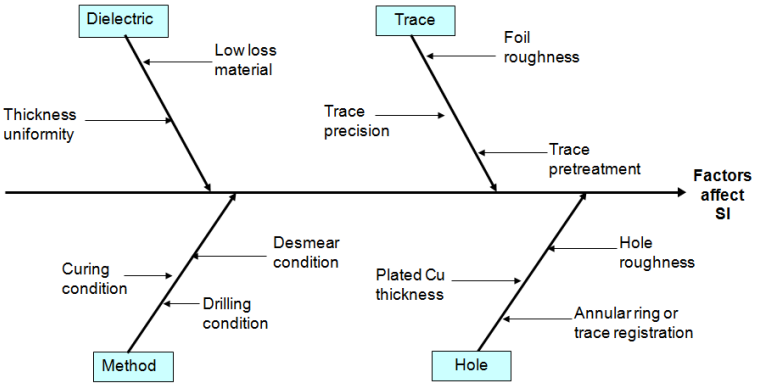


Figure 5 - Fishbone analysis of signal integrity

From Table 2 the physical property result, we can see the material is already fully cured with delta Tg less than 3 degree Celsius.

Table 2 - Material Property

Items		Unit	Result
T288		min	> 30
CTE	Alpha1	ppm/℃	51.12
	Alpha2	ppm/℃	184.4
	50~260℃	%	2.274
DSC Tg	Tg 1	℃	173.03
	Tg 2		175.56
	△Tg		2.53

Then we did cross-sectioning to check the registration, plated copper thickness and resin integrity of the coupons. However we don't see any obvious variation when referring to figure 6 & 7.

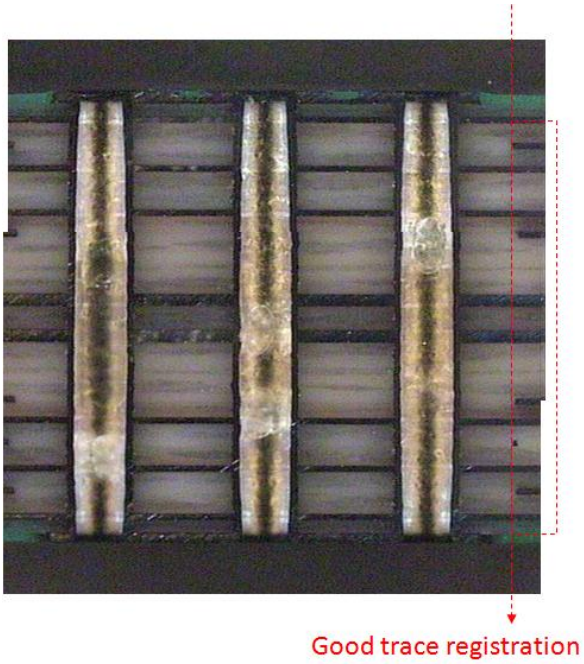
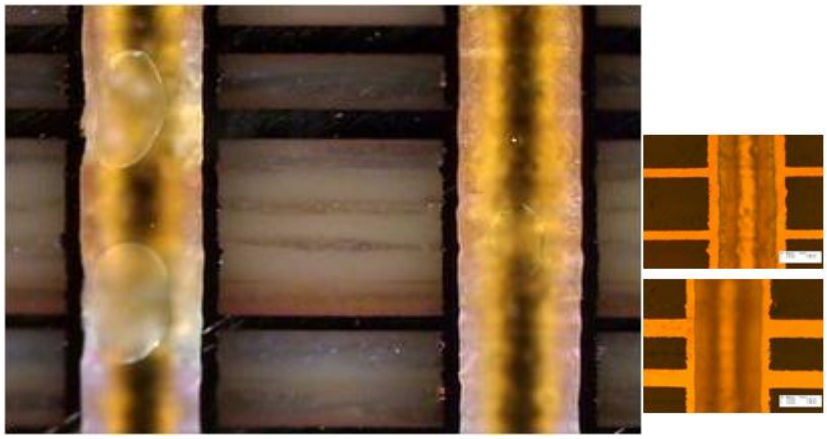


Figure 6 – Layer registration



Plated Cu thickness
1.288mils
1.255mils
1.272mils
1.190mils
1.109mils

Figure 7 – (left) No resin starvation defect found, (right) plated Cu thickness >0.8mil

We decided to do more cross-sectioning of trace according to below locations;

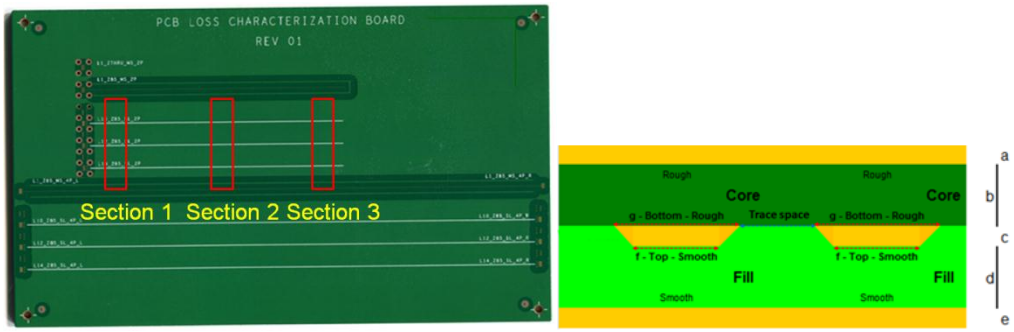


Figure 8 – Cross-sectioning location

It looks the prepreg dielectric (d) thinner than the designed value 3.7mils especially at layer 3, 5, 12 and 14.

L3

Parameter	units	Section 1	Section 2	Section 3	Avg.	Range	Spec.
a	mil	1.24	1.3	1.24	1.26	0.05	1.3
b	mil	3.84	3.78	3.78	3.80	0.05	4.0
c	mil	1.17	1.16	1.14	1.15	0.03	1.3
d	mil	2.86	2.70	2.81	2.79	0.16	3.7
e	mil	1.41	1.35	1.24	1.33	0.16	1.3
f	mil	3.42	3.4	3.46	3.42	0.06	
g	mil	3.88	3.94	3.9	3.91	0.05	4.1
h	mil	3.5	3.59	3.58	3.56	0.09	
space	mil	6.7	6.59	6.54	6.61	0.16	6.9
BO roughness	μm			1.18			
Matte side Roughness	μm			2.77			
Impedance	Ω			85.7			85

L5

Parameter	units	Section 1	Section 2	Section 3	Avg.	Range	Spec.
a	mil	1.24	1.41	1.35	1.33	0.16	1.3
b	mil	3.95	3.78	3.78	3.84	0.16	4.0
c	mil	1.18	1.15	1.2	1.18	0.05	1.3
d	mil	2.81	2.70	2.70	2.74	0.11	3.7
e	mil	1.3	1.35	1.3	1.32	0.06	1.3
f	mil	3.39	3.39	3.31	3.36	0.08	
g	mil	3.88	3.86	3.89	3.88	0.03	4.1
h	mil	3.57	3.55	3.55	3.55	0.02	
space	mil	6.7	6.7	6.75	6.72	0.05	7.0
BO roughness	μm			1.08			
Matte side roughness	μm			2.87			
Impedance	Ω			86.3			85

L7

Parameter	units	Section 1	Section 2	Section 3	Avg.	Range	Spec.
a	mil	1.3	1.3	1.24	1.28	0.05	1.3
b	mil	2.86	2.76	2.7	2.77	0.16	3.0
c	mil	1.14	1.15	1.16	1.15	0.02	1.3
d	mil	10.1	10	9.73	9.94	0.38	10.0
e	mil	2.81	2.76	2.59	2.72	0.22	2.6
f	mil	4.34	4.29	4.35	4.33	0.05	
g	mil	4.95	4.81	4.79	4.85	0.16	4.1
h	mil	4.60	4.50	4.52	4.54	0.1	
space	mil	7.67	7.83	7.73	7.74	0.16	8.25
BO roughness	μm			1.18			
Matte side roughness	μm			2.87			
Impedance	Ω			88.3			85

L10

Parameter	units	Section 1	Section 2	Section 3	Avg.	Range	Spec.
a	mil	1.41	1.24	1.35	1.33	0.16	1.3
b	mil	2.81	2.92	2.7	2.81	0.22	3.0
c	mil	1.26	1.18	1.13	1.19	0.13	1.3
d	mil	10.21	10.16	10.1	10.16	0.11	10.0
e	mil	2.7	2.54	2.76	2.67	0.22	2.6
f	mil	4.52	4.42	4.32	4.42	0.2	
g	mil	5.17	5.03	4.82	5.01	0.34	4.1
h	mil	4.84	4.67	4.5	4.67	0.34	
space	mil	7.13	7.19	7.57	7.3	0.43	8.25
BO roughness	μm			1.08			
Matte side roughness	μm			2.27			
Impedance	Ω			86.8			85

L12

Parameter	units	Section 1	Section 2	Section 3	Avg.	Range	Spec.
a	mil	1.3	1.3	1.24	1.28	0.05	1.3
b	mil	3.67	3.78	3.84	3.76	0.16	4.0
c	mil	1.2	1.23	1.18	1.2	0.05	1.3
d	mil	2.76	2.70	2.81	2.76	0.11	3.7
e	mil	1.41	1.48	1.24	1.37	0.22	1.3
f	mil	3.64	3.54	3.53	3.57	0.12	
g	mil	4.21	4.07	4.09	4.12	0.14	4.1
h	mil	3.85	3.68	3.71	3.75	0.17	
space	mil	6.21	6.27	6.16	6.21	0.11	7.0
BO roughness	µm			1.38			
Matte side roughness	µm			2.37			
Impedance	Ω			82.4			85

L14

Parameter	units	Section 1	Section 2	Section 3	Avg.	Range	Spec.
a	mil	1.24	1.24	1.3	1.26	0.05	1.3
b	mil	3.84	3.89	3.84	3.85	0.06	4.0
c	mil	1.2	1.16	1.16	1.17	0.04	1.3
d	mil	2.76	2.92	2.70	2.79	0.22	3.7
e	mil	1.24	1.35	1.3	1.3	0.11	1.3
f	mil	3.4	3.49	3.52	3.47	0.12	
g	mil	4.06	4.08	4.12	4.08	0.07	4.1
h	mil	3.6	3.74	3.75	3.7	0.15	
space	mil	6.48	6.32	6.7	6.5	0.38	7.0
BO roughness	µm			1.48			
Matte side roughness	µm			2.47			
Impedance	Ω			83.5			85

Figure 9 – Cross-sectioning result of dielectric thickness, copper trace width, trace space at layer 3, 5, 7, 10, 12 & 14

We also observe glass fiber touch onto the copper trace without sufficient resin coating at those thinner dielectric layers. As a result, the bulk resistivity of the dielectric would be dropped inevitably to cause signal loss increase.

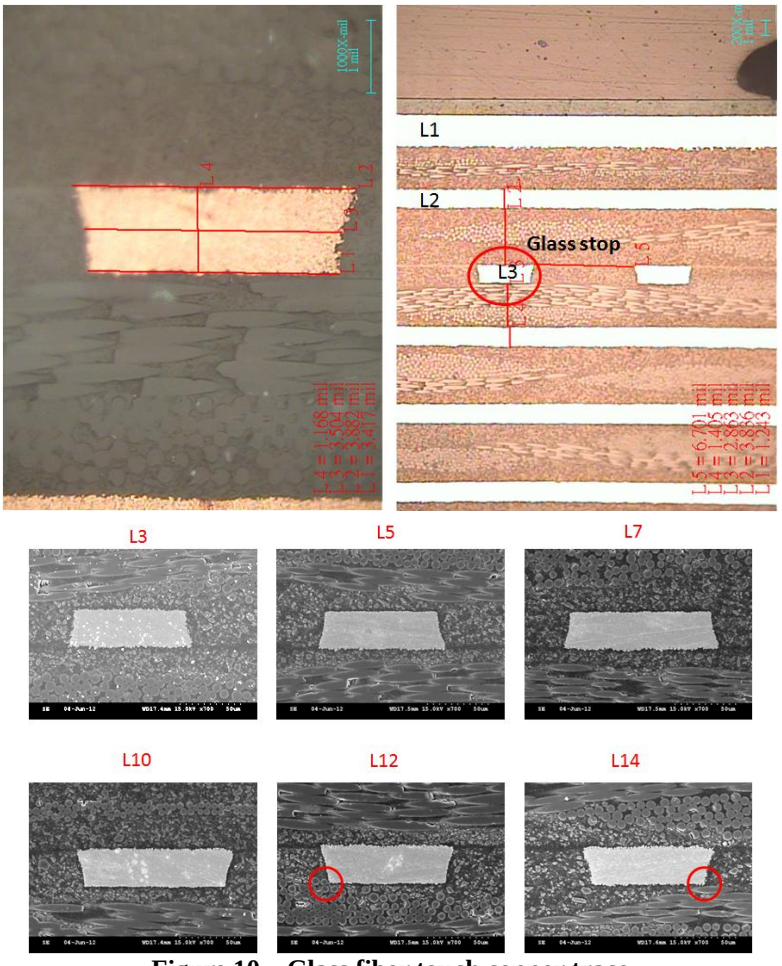
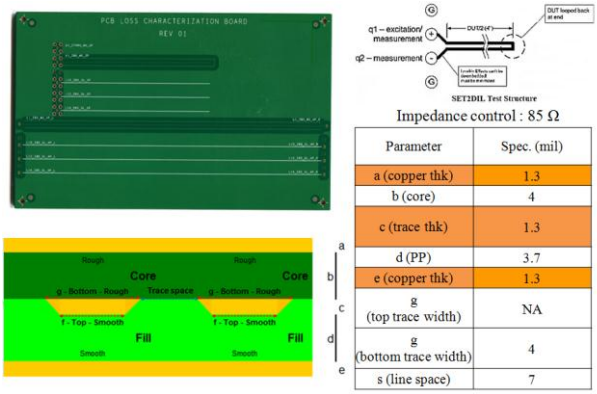


Figure 10 – Glass fiber touch copper trace

What is relationship between characteristic impedance and signal loss?

Someone may think about if we can achieve the nominal controlled impedance, we should have the best signal integrity result. The answer is not true for sometimes, but why?

Here is another example of 16L SI measurement from three different PCB shops. They used the same circuit pattern design and same low loss FR4 material to build the same 16 layers SI test vehicles. We measured them under the same environment condition. Unfortunately we don't see the best result at B shop even she get the best impedance controlled value of 85 Ohms.



Impedance control : 85 Ω

Parameter	Spec. (mil)
a (copper thk)	1.3
b (core)	4
c (trace thk)	1.3
d (PP)	3.7
e (copper thk)	1.3
g (top trace width)	NA
g (bottom trace width)	4
s (line space)	7

Figure 11 – Circuit pattern design

Table 3 - No guarantee for SI even good impedance control at B shop

Customer	Layer count	Coupon	Layer	SDD21 (@4GHz)	Impedance (Ω)
A	16L	parallel	L3	0.461	91.8
	16L	parallel	L5	0.469	92.3
	16L	parallel	L7	0.477	90.9
	16L	parallel	L10	0.472	91.2
	16L	parallel	L12	0.471	94.8
	16L	parallel	L14	0.460	94.5
B	16L	parallel	L3	0.578	85.7
	16L	parallel	L5	0.547	86.3
	16L	parallel	L7	0.538	88.3
	16L	parallel	L10	0.524	86.8
	16L	parallel	L12	0.555	82.4
	16L	parallel	L14	0.579	83.5
C	16L	parallel	L3	0.490	75.7
	16L	parallel	L5	0.501	75.6
	16L	parallel	L7	0.502	76.2
	16L	parallel	L10	0.499	76.9
	16L	parallel	L12	0.487	75.8
	16L	parallel	L14	0.478	74.4

Total loss

The signal total loss could be divided into two parts, dielectric loss and conductor loss. The total attenuation could be expressed as below formula

$$\alpha\ (dB) = \alpha(dielectric) + \alpha(conductor) \quad \text{for stripline}$$

How should we overcome the barrier to achieve better signal integrity?

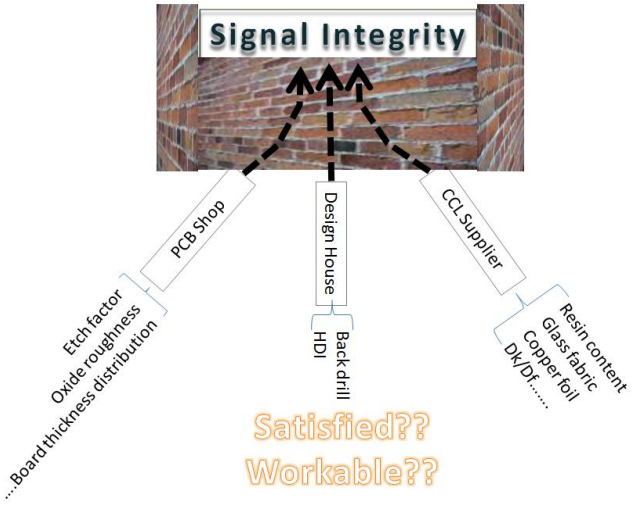


Figure 12 – Signal integrity barrier

Signal loss in transmission line

We select five different materials with their own dielectric constant and dissipation factor as shown below table and we do the insertion loss study by OEMs pattern (Table 5) and PCB stack up (Table 6).

Table 4 - Physical and electric properties of standard/middle/low loss materials

Property	Material A	Material B	Material C	Material D	Material E
Tg	210 (DMA)	170 (DSC)	175 (DSC)	150 (TMA)	175 (DSC)
Water absorption (wt%)	0.05	0.07	0.1	0.08	0.12
Dk (RC 50% @1GHz)	3.9	3.9	4.1	4.3	4.4
Df (RC 50% @1GHz)	0.007	0.009	0.01	0.011	0.018
Resin system	Halogen free low loss VLP	Halogen free low loss RTF	Halogen free middle loss RTF	Halogen free middle loss RTF	Brominated epoxy standard loss RTF

Table 5 - Test coupon pattern

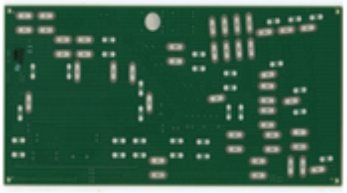
SPP coupon	S3 Coupon
	

Table 6 - Stackup

<table>
<tr><th>SPP Stack up</th><th>S3 Stack up</th></tr>
<tr><td>
<table>
<tr><th>Layer</th><th>Stack up</th></tr>
<tr><td>1</td><td>1/2 oz</td></tr>
<tr><td>PP</td><td>1080X1</td></tr>
<tr><td>2</td><td>1 oz</td></tr>
<tr><td>Core</td><td>106X2 RC 70-75%</td></tr>
<tr><td>3</td><td>1 oz RTF</td></tr>
<tr><td>PP</td><td>106X3 RC 70-75%</td></tr>
<tr><td>4</td><td>1 oz</td></tr>
<tr><td>Core</td><td>5mil (2116X1)</td></tr>
<tr><td>5</td><td>1 oz</td></tr>
<tr><td>PP</td><td>2116X1 RC 50-75%</td></tr>
<tr><td>6</td><td>1/2 oz</td></tr>
<tr><td>Core</td><td>4mil (2116X1)</td></tr>
<tr><td>7</td><td>1/2 oz</td></tr>
<tr><td>PP</td><td>2116*2 RC53 %</td></tr>
<tr><td>8</td><td>1/2 oz</td></tr>
</table>
</td><td>
<table>
<tr><th>Layer</th><th>Stack up</th></tr>
<tr><td>1</td><td>1 oz</td></tr>
<tr><td>PP</td><td>2116*2 RC53 %</td></tr>
<tr><td>2</td><td>1 oz</td></tr>
<tr><td>Core</td><td>10mil (2116*2)</td></tr>
<tr><td>3</td><td>1 oz</td></tr>
<tr><td>PP</td><td>7628 RC45 %</td></tr>
<tr><td></td><td>28mil core unclad</td></tr>
<tr><td>PP</td><td>7628 RC45 %</td></tr>
<tr><td>4</td><td>1 oz</td></tr>
<tr><td>Core</td><td>10mil core</td></tr>
<tr><td>5</td><td>1 oz</td></tr>
<tr><td>PP</td><td>2116*2 RC53 %</td></tr>
<tr><td>6</td><td>1 oz</td></tr>
</table>
</td></tr>
<tr><td>50 Ohms stripline/ trace length 3 & 10cm
trace width at L6 ~ 3.5mils (measured layer)</td><td>50 Ohms stripline/ trace length 16”
trace width at L2 ~ 8.8mils</td></tr>
</table>

No matters of SPP or S3 results, PWB base materials always are played a major role for insertion loss performance. The low dissipation factor of material the less loss we can observe in figure 13.

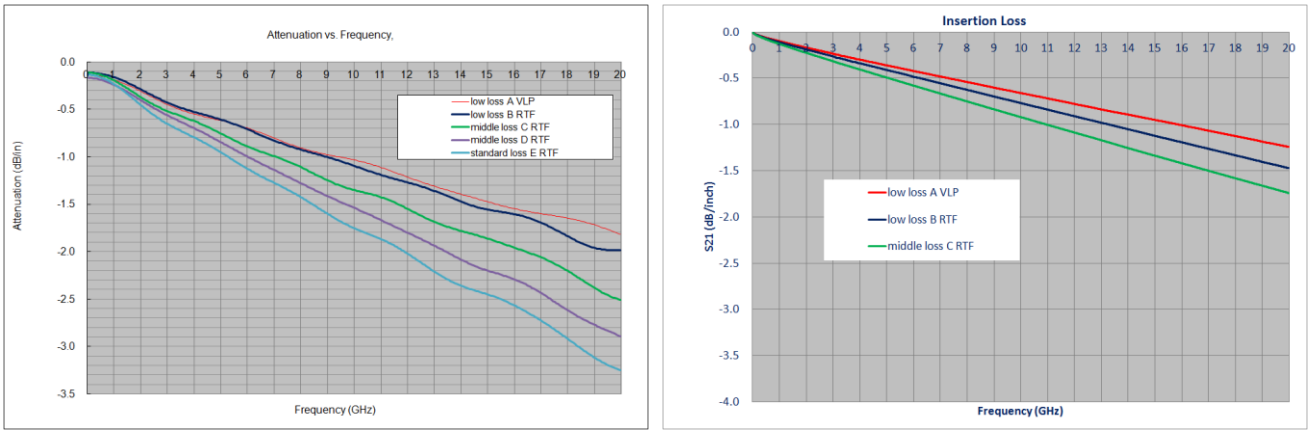


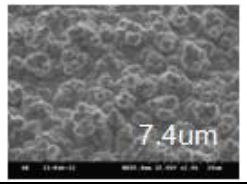
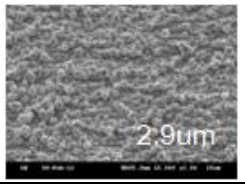
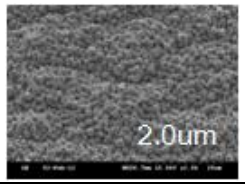
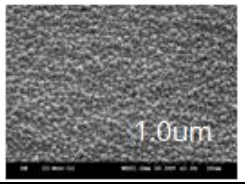
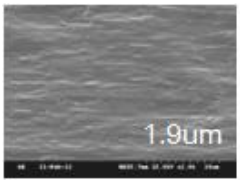
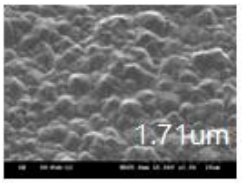
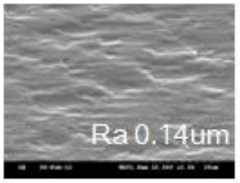
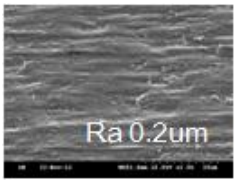
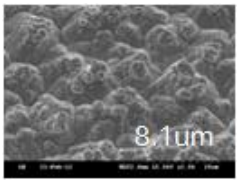
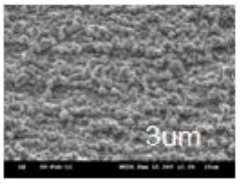
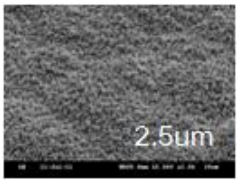
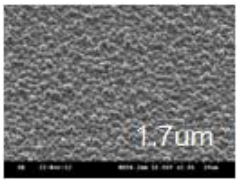
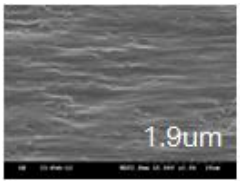
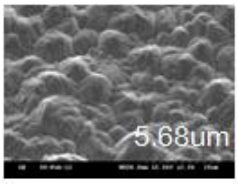
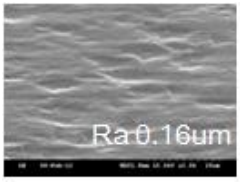
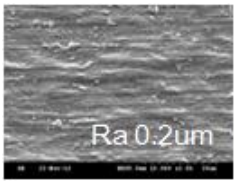
Figure 13 – (left) attenuation result convert by GammaZ from SPP measurement & (right) S21 result measures by VNA from S3 measurement

Copper roughness effect

At high frequency the skin depth shrinks to less than the RMS roughness of conductor, forcing current to traverse every hill and dale on the surface, it means that current will through the longer path than the smooth path and higher resistance that current face it, therefore the Rac with higher roughness will have higher resistance than smooth condition.

There are several types of copper foil in the market and their SEM photo is as shown below table

Table 7 - Copper foil roughness and SEM Photos

Copper type	HTE	RTF	VLP	HVLP
Hoz Core Side (matte side)				
Hoz Prepreg Side (shinny side)				
1oz Core Side (matte side)				
1oz Prepreg Side (shinny side)				

Recently, the copper foil manufacturers develop a new type of copper foil HVLP with very low roughness in order to solve the problem of signal loss caused by copper profile.

PCB manufacturing process and signal integrity

Oxide alternative and oxide replacement treatment

There are two main methods to treat the inner layer board for bonding, oxide alternative and oxide replacement; they use different principle and chemical to treat the surface of conductor. Does it cause the signal loss difference for different oxide treatment? We will discuss it in this paper later.

Lamination

The lamination is a key process for PCB manufacture, the material with higher cross link density under cured condition , means that moisture is not easy penetrate into the material and stabilize polymer structure. It is helpful to keep material with low dielectric constant and dissipation factor property.

Back drill and via stub effect

In order to reduce the return path in a transmission line, some PCB manufacturers develop back drill technique to reduce via stub effect. The via stub effect occurred at AC current the signal will travel longer return path than it should go. Back drill could eliminate the inductance on the extra path and should have better loss performance.

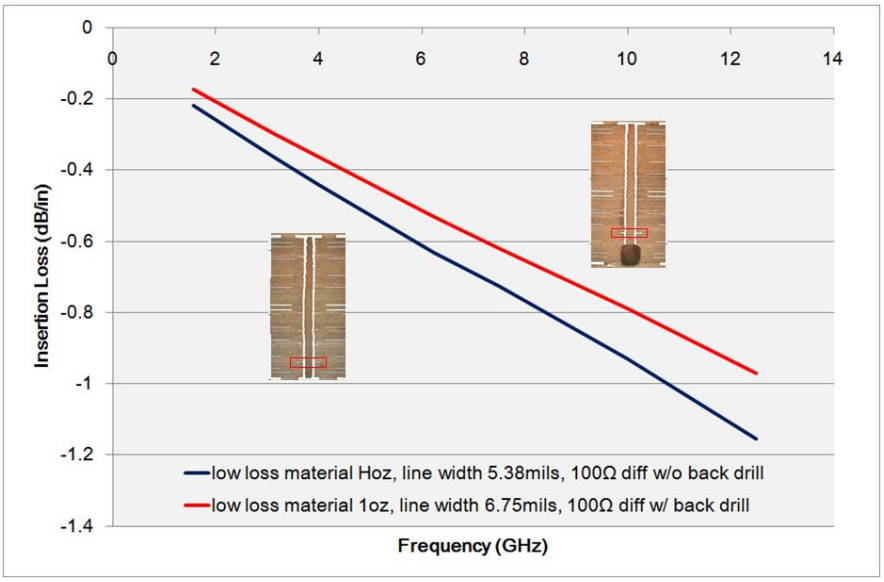


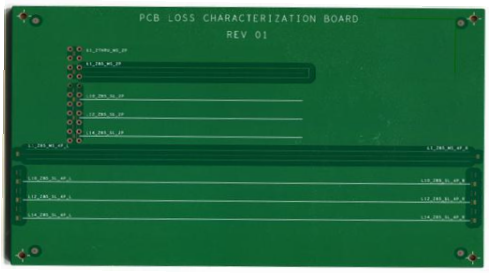
Figure 14 – Insertion loss of a 24 layer SI board

Proximity effect

It will have the proximity effect when pairs of two lines are too close together. We will discuss the line spacing effect for signal integrity under the same stack up, copper foil, and line width condition later.

Experiment Plan

In this experiment we want to find out which factors dominant to signal loss performance by doing SET2DIL measurement. We prepare a 16L SET2DIL stackup each for different set of factors and use low loss A material for the test vehicle.



Layer	Stack up
1	1/2 oz
PP	1080 RC 63%
2	1 oz
Core	4.5mil 2116 RC 50%
3	1 oz
PP	106X2 RC 75%
4	1 oz
Core	4.5mil 2116 RC 50%
5	1 oz
PP	106X2 RC 75%
6	1 oz
Core	3mil 1/1 1080X1 RC 63%
7	1 oz
PP	1080X2 RC 63%+2116 RC 55%
8	2 oz
Core	5mil 2116X1
9	2 oz
PP	1080X2 RC 63%+2116 RC 55%
10	1 oz
Core	3mil 1080X1
11	1 oz
PP	106X2 RC 75%
12	1 oz
Core	4.5mil 2116 RC 50%
13	1 oz
PP	106X2 RC 75%
14	1 oz
Core	4.5mil 2116 RC 50%
15	1 oz
PP	1080X2 RC 63%
16	Hoz

Figure 15 – Test pattern and stackup design of low loss material A

Factors to be consideration;

1. Change +/- 10% of the dielectric thickness
2. Change +/- 10% of the trace width
3. Change +/- 10% of the trace space
4. Change copper foil type/roughness
5. Change resin content of stack up
6. Change oxide treatment of inner layer (oxide replacement & reduced oxide)

Result and Discussion

1) Change dielectric thickness

Below table show the geometry variation between the control and test specimen;

Sample	item	L3	L5	L7	L10	L12	L14
"+10% dielectric"	core thk	13.39%	12.24%	16.79%	17.73%	12.50%	13.41%
	prepreg thk	11.05%	9.17%	11.15%	13.61%	5.73%	5.02%
	trace width	1.68%	2.21%	5.47%	-2.40%	2.98%	4.29%
	trace space	-2.02%	-2.36%	-5.80%	0.91%	0.21%	0.98%
"-10% dielectric"	core thk	-10.13%	-11.11%	-15.47%	-14.49%	-9.26%	-6.71%
	prepreg thk	-4.70%	-4.28%	-8.85%	-5.64%	-4.51%	-10.44%
	trace width	1.78%	1.34%	2.27%	-4.06%	2.58%	2.91%
	trace space	-2.53%	-0.41%	-3.35%	1.83%	2.08%	-1.78%

The dielectric thickness is an apparent influence factor for SDD21result. When it is increasing about 10%, it could reduce SDD21@4GHZ about 5%.

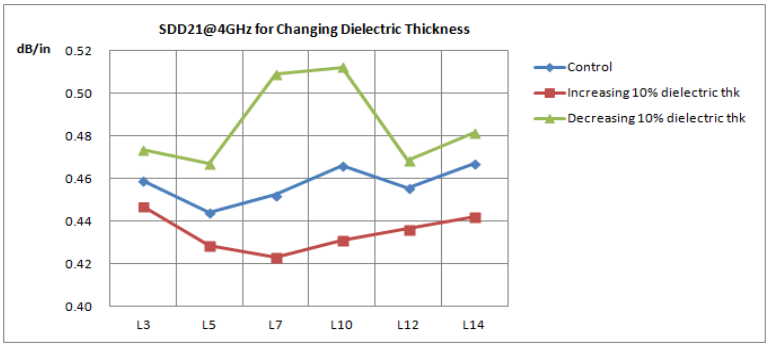


Figure 16 - The relationship between SDD21 and dielectric thickness

The insertion loss suddenly arise at layer 7 & 10 of the coupon with decreasing 10% dielectric thickness which is caused by resin starvation between glass fiber and copper trace shown as figure 17.

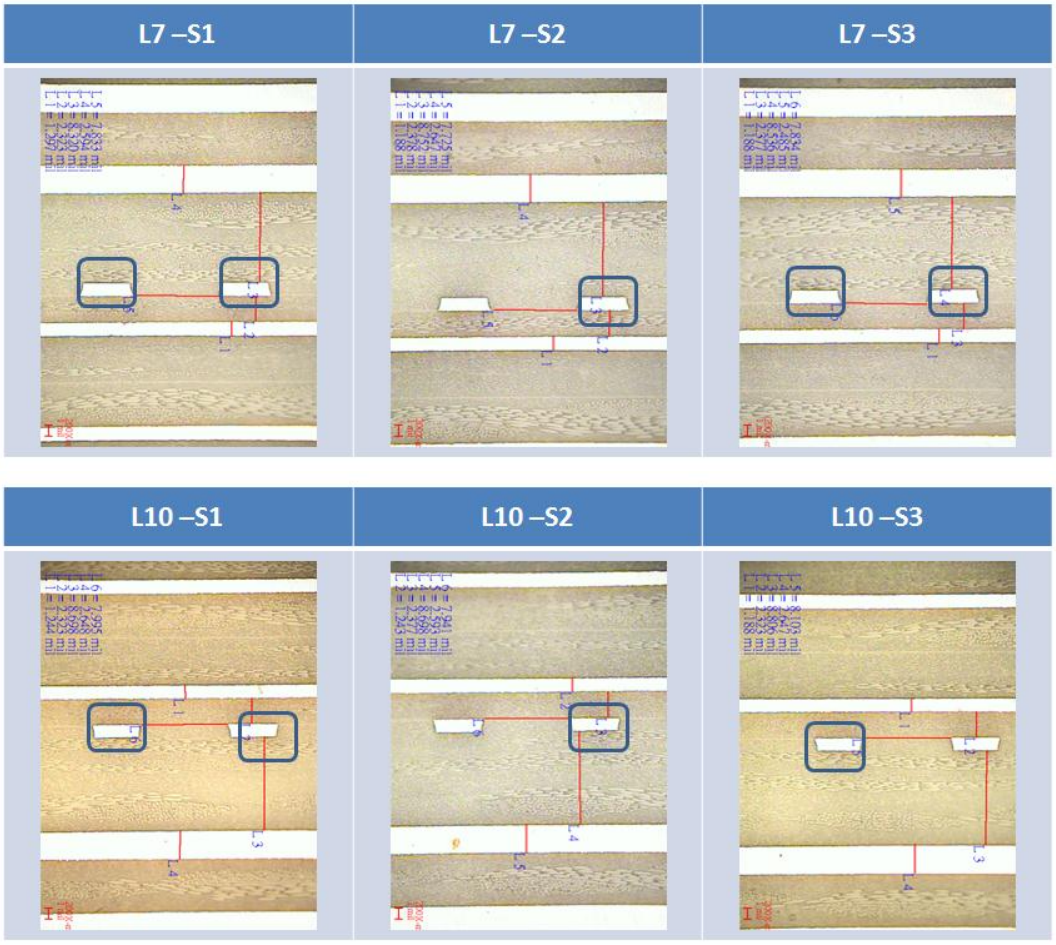


Figure 17 – Resin starvation found between glass fiber and copper trace of the "-10%" specimen

2) Change trace width

Below table show the geometry variation between the control and test specimen;

Sample	item	L3	L5	L7	L10	L12	L14
"+10% trace width"	core thk	1.14%	-1.13%	0.05%	1.95%	-0.82%	0.66%
	prepreg thk	-0.41%	0.39%	1.53%	3.30%	-0.83%	0.40%
	trace width	11.68%	9.80%	8.65%	7.83%	15.48%	19.22%
	trace space	-1.11%	-0.31%	-1.78%	0.23%	-0.11%	-1.58%
"-10% trace width"	core thk	0.00%	-1.61%	0.01%	0.63%	0.64%	-0.65%
	prepreg thk	-5.51%	1.83%	0.58%	2.33%	-0.82%	1.61%
	trace width	-4.69%	-7.58%	-9.88%	-11.22%	-8.89%	-5.37%
	trace space	-5.97%	-4.11%	-4.69%	2.75%	1.77%	-1.58%

The trace width varies within +/-10% doesn't affect the SDD21 performance.

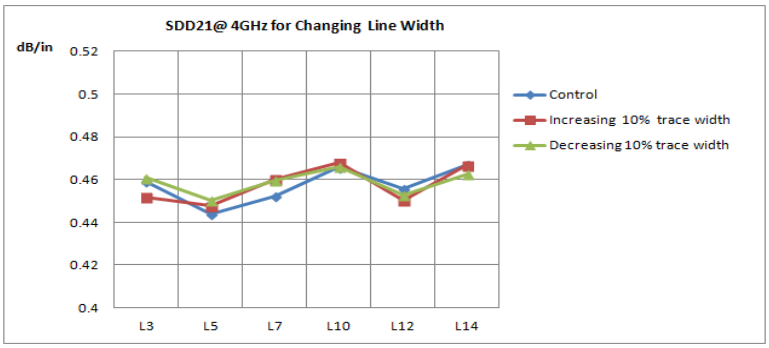


Figure 18 - The relationship between SDD21 and trace width

3) Change trace space

Below table show the geometry variation between the control and test specimen;

Sample	item	L3	L5	L7	L10	L12	L14
"+10% trace space"	core thk	0.48%	-1.61%	1.95%	2.64%	0.00%	1.15%
	prepreg thk	-0.20%	1.21%	-1.35%	1.17%	0.61%	-1.41%
	trace width	1.59%	-8.05%	-0.07%	-0.59%	3.77%	0.33%
	trace space	7.79%	13.96%	6.93%	11.22%	9.03%	10.27%
"-10% trace space"	core thk	1.46%	-1.61%	0.66%	0.01%	0.64%	0.66%
	prepreg thk	-3.27%	2.05%	1.73%	3.69%	2.45%	7.23%
	trace width	1.96%	2.11%	0.91%	-1.20%	2.88%	1.18%
	trace space	-13.24%	-11.40%	-13.61%	-10.52%	-9.97%	-8.30%

The trace space within +/-10% doesn't affect the SDD21 performance.

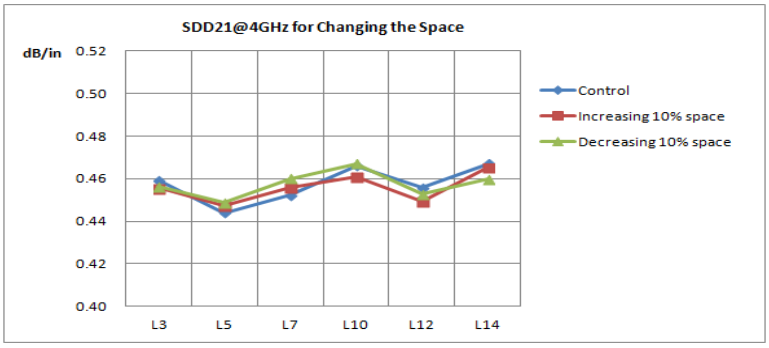


Figure 19 - The relationship between SDD21 and trace space

4) Change copper foil roughness

Below table show the geometry variation between the control and test specimen;

Sample	item	L3	L5	L7	L10	L12	L14
"HVLP"	core thk	1.96%	-0.49%	-2.57%	5.89%	-0.65%	0.66%
	prepreg thk	0.41%	-0.61%	1.73%	-0.39%	6.14%	-0.80%
	trace width	1.78%	-3.83%	1.38%	-0.52%	-0.31%	3.98%
	trace space	-0.20%	1.74%	-0.67%	-0.45%	0.93%	-0.89%

The copper foil roughness is an apparent influence factor for SDD21result. The lower copper roughness is beneficial for insertion loss. The HVLP copper foil could improve about 5.8% SDD21 compare with VLP copper foil.

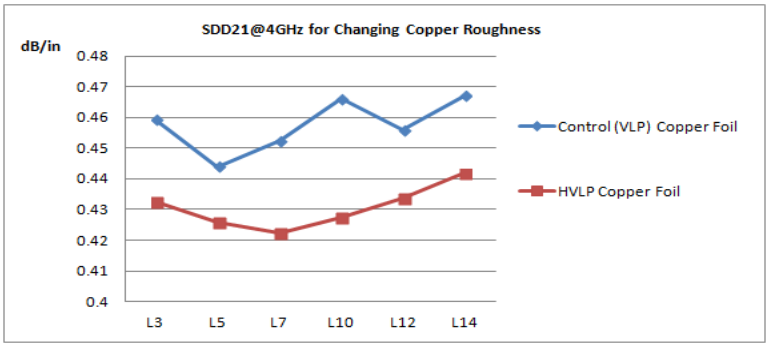
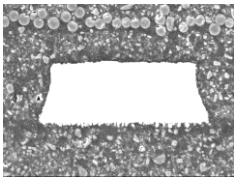
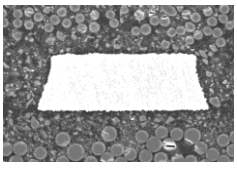
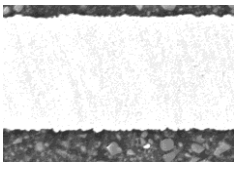


Figure 20 - The relationship between SDD21 and copper foil/roughness

HVLP copper profile is more uniform than VLP which is good for signal integrity.

Copper Foil type	500X	1000X
VLP Copper Foil (Rz : 1.7um)		
HVLP Copper Foil (Rz : 1.2 um)		

5) Change resin content of stack up

Below table show the geometry variation between the control and test specimen;

Sample	item	L3	L5	L7	L10	L12	L14
"low resin content 50~55%"	core thk	2.94%	-0.32%	0.00%	4.59%	2.43%	1.64%
	prepreg thk	6.95%	5.90%	2.50%	2.91%	5.12%	6.22%
	trace width	0.99%	-4.02%	1.68%	-1.35%	0.18%	3.12%
	trace space	-3.03%	0.41%	-4.24%	0.92%	0.83%	1.28%
"high resin content 70~75%"	core thk	-4.91%	-5.64%	-1.92%	4.60%	-4.07%	-3.12%
	prepreg thk	-2.66%	-3.47%	0.00%	-0.59%	-2.67%	-1.80%
	trace width	-1.17%	0.30%	2.28%	-5.19%	2.98%	-2.47%
	trace space	-1.82%	-0.72%	-5.58%	1.61%	1.45%	4.25%

Changing stack up resin content seems not improve the SDD21 result obviously.

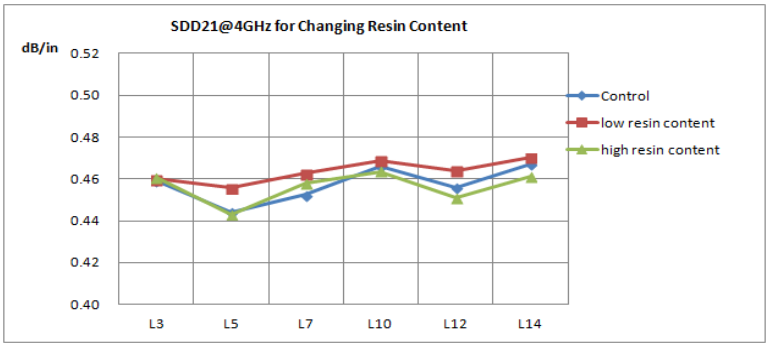


Figure 21 - The relationship between SDD21 and resin content

6) Change oxide treatment

Below table show the geometry variation between the control and test specimen;

Sample	item	L3	L5	L7	L10	L12	L14
"BO treatment"	core thk	1.14%	-0.33%	-1.93%	1.30%	-1.14%	1.79%
	prepreg thk	0.41%	-1.22%	0.77%	1.36%	-1.03%	-1.21%
	trace width	8.94%	-9.11%	1.75%	1.14%	6.56%	1.60%
	trace space	-5.15%	3.59%	-4.02%	-1.37%	1.55%	1.68%

From the below figure, we could see that black oxide replacement could improve SDD21 slightly compare to oxide alternative treatment about 3%.

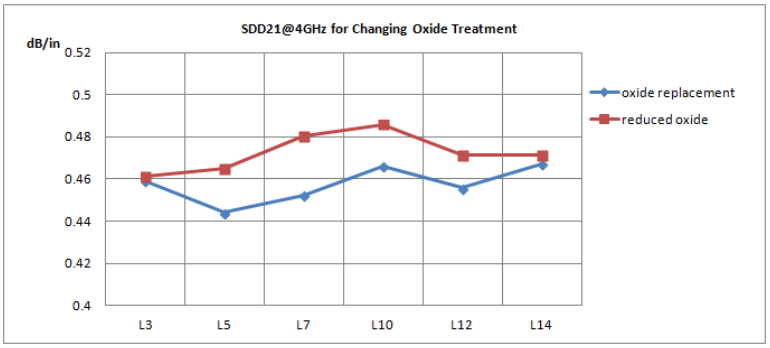


Figure 22 - The relationship between SDD21 and oxide treatment

The trace at layer 14 of the oxide replacement specimen looks high and close to the one of reduced oxide maybe cause by a glass fiber touch to the copper trace in figure 22. It should take more cross-sectioning for confirmation.

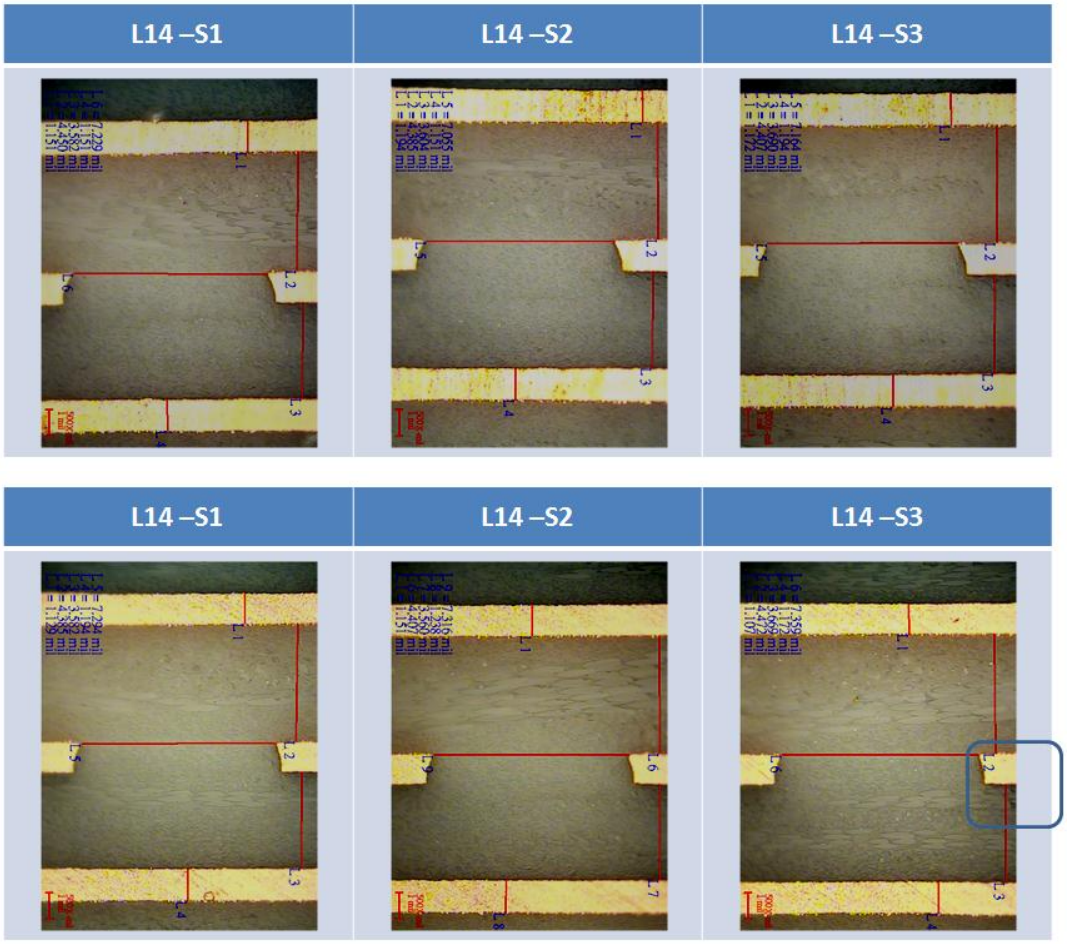


Figure 23 - The cross-section of layer 14 (upper) for reduced oxide specimen and (lower) for oxide replacement specimen which show a glass fiber touch the copper trace

Conclusion

1. No guarantee for signal integrity even there is good controlled impedance of the PCB board.
2. The lower Dk and Df property is an essential element for achieving better insertion loss performance in the high speed

and high frequency. It is necessary to use low loss base material to keep signal integrity especially under higher frequency requirement.

3. Considering skin effect of copper, low roughness profile foil should be used in priority for those high speed and high frequency application.
4. The back drill technique can eliminate via stub effect to improve signal integrity.
5. Regarding with experiment result of SET2DIL measurement,
    i. The dielectric thickness increase about 10% could reduce SDD21@4GHZ about 5%. This can explain why the multilayer board the insertion loss sometimes is increased even under same stackup and PCB manufacturing if there is insufficient dielectric.
    ii. The trace width and space within +/-10% doesn't affect the SDD21 performance.
    iii. The lower copper roughness is beneficial for SDD21performance. The HVLP copper foil (1oz / Rz 1.7um) could improve about 5.8% SDD21 compare to the one using VLP copper foil (1oz/ Rz 2.5um)
    iv. Changing resin content of stack up with keeping the same thickness (e.g. 2 ply of 106 instead 1 ply of 2116) doesn't affect SDD21 performance obviously.
    v. From the result it looks oxide replacement could improve SDD21 slightly compare to reduced oxide treatment about 3%. However we need to do further study for confirmation.

Reference

1. Signal Integrity : Simplified by Eric Bogatin