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Reliability Study of Bottom Terminated Components

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Abstract
Bottom terminated components (BTC) are leadless components where terminations are protectively plated on the underside of the package. They are all slightly different and have different names, such as QFN (quad flat no lead), DFN (dual flat no lead), LGA (land grid array) and MLF (micro lead-frame. BTC assembly has increased rapidly in recent years. This type of package is attractive due to its low cost and good performance like improved signal speeds and enhanced thermal performance.

However, bottom terminated components do not have any leads to absorb the stress and strain on the solder joints. It relies on the correct amount of solder deposited during the assembly process for having a good solder joint quality and reliable reliability. Voiding is typically seen on the BTC solder joint, especially on the thermal pad of the component. Voiding creates a major concern on BTC component's solder joint reliability. There is no current industry standard on the voiding criteria for bottom terminated component. The impact of voiding on solder joint reliability and the impact of voiding on the heat transfer characteristics at BTC component are not well understood. This paper will present some data to address these concerns. We will present our study on the thermal cycling reliability of bottom terminated components, including non-symmetrical LGA and QFN components. Two different solder process conditions and different voiding levels were included in the study, and the results will be discussed. The paper also covers our thermal modeling study of the heat transfer characteristic of BTC component.

Keywords: Bottom Terminated Component, BTC, LGA, QFN, BTC Reliability, Voiding and Reliability, Voiding and Heat Transfer of BTC Component.

Introduction

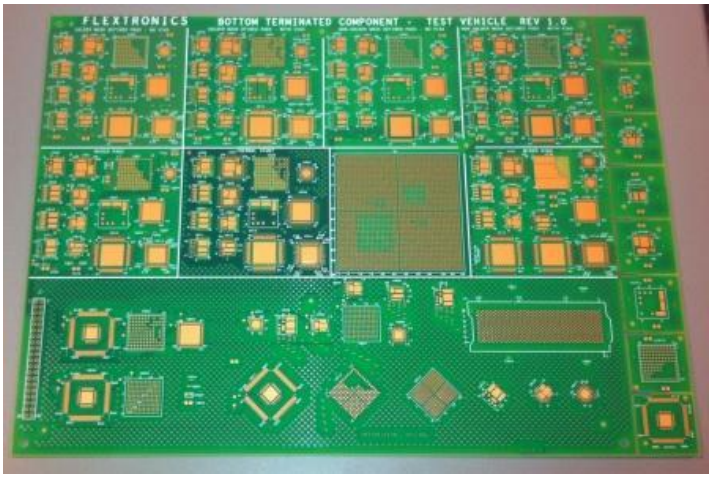
BTC is known as bottom terminated component or bottom termination component. It is a leadless component for which the termination is protectively plated and is on the underside of the package. Common BTC components include QFN (quad flat no lead), LGA (land grid array), MLF (micro lead-frame), DFN (dual flat no lead), etc. BTC components are available in different sizes, lead counts, and designs. Most parts are unique from supplier to supplier with various pad designs.

Most BTC components typically have a large ground or power termination along with smaller signal terminations. Voiding is commonly seen at the solder joint of BTC components, especially at the thermal pads. In many cases, large voids and many voids which can exceed 25% of the area can be seen at the thermal pads of BTC components. Voiding causes many concerns for the solder joint reliability of BTC components. The following questions are typical when dealing with BTC: Will the excessive voiding decrease the solder joint reliability? Will the voiding impact the heat transfer and thermal behavior of the BTC component? In this paper, we will present our study on the thermal cycling reliability of BTC components. Voiding and reliability data will be compared. We will discuss the heat transfer characteristic of BTC component using our thermal modeling study.

Experimental Details

Test Vehicle

The company Bottom Terminated Component Test Vehicle, Rev 1.0 was used in the study (Figure 1a). It is a double sided board with the dimension of 8" x 11" x 0.093" [203mmx279mmx2.4mm]. Thirteen different BTC component types from various suppliers were designed into the test vehicle (Figure 1b). It also had other components such as BGA, SMT connector, and chip components among others.



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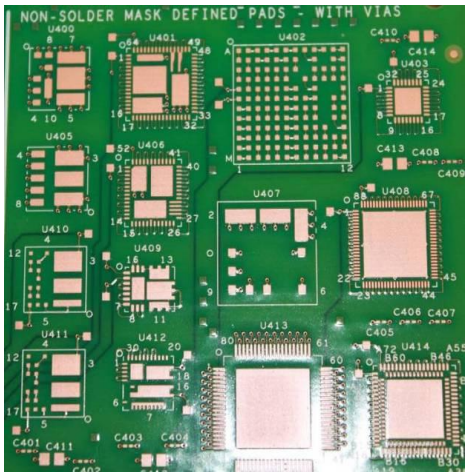

b)

Figure 1 - Company Bottom Terminated Component Test Vehicle a) Topside b) Various BTC Pad Design.

Components

Table 1 summarizes the component details tested in the reliability study. Both QFN and LGA component types were included in the reliability testing. We also included a BGA and FQFP component for data comparison. For the QFN component type, we had both symmetrical QFN (Figure 2) and non-symmetrical QFN components in the study (Figure 3). For the LGA component type, some LGA components had the same pad sizes for both signal and ground pins (Figure 4). Some other LGA components had various pad sizes for signal and ground pins (Figure 5).


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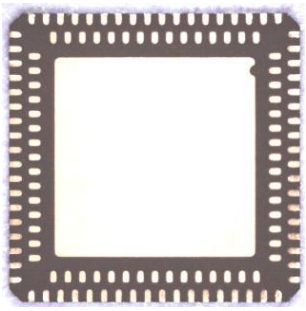
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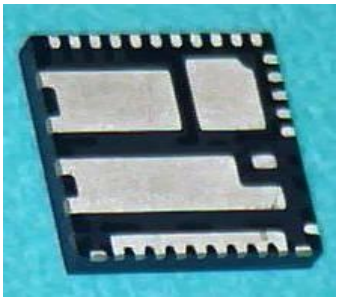
Figure 2 - Symmetrical QFN Component Images. a) QFN 88 b) Dual Row QFN132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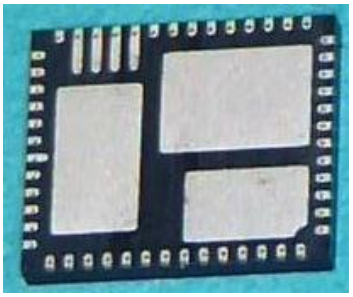
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Figure 3 - Non-symmetrical QFN Component Images.

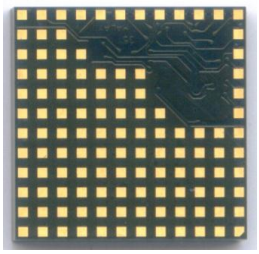


Figure 4 - LGA Images_ Identical Pad Size for Signal and Ground Pins.

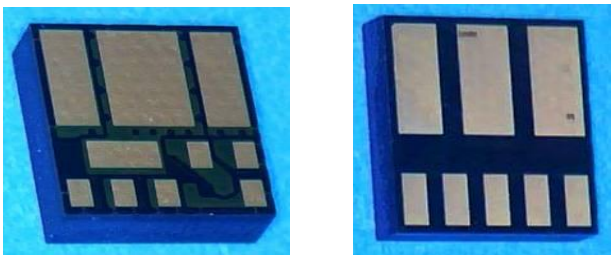


Figure 5 - LGA Images_ Non-identical Pad Size for Signal and Ground Pins.

Table 1 - Component Details

Process Condition	Component ID	Component Description	Component Type	Daisy Chain Information	Qty
1. Regular (more voiding)	QFN32	Typical QFN, 0.5mm pitch	QFN	Yes	30
	QFN88	Typical QFN, 0.4mm pitch	QFN	Yes	30
	QFN132	Dual row QFN, 0.5mm pitch	QFN	Yes	20
	QFN52	Non symmetrical QFN	QFN	Yes	30
	QFN 3550	Non symmetrical QFN	QFN	Yes	30
	QFN 3837	Non symmetrical QFN	QFN	Yes	30
	FQFP176	FQFP	FQFP	Yes	30
	LGA 2004	LGA, different pad size	LGA	No	30
	LGA 2005	LGA, different pad size	LGA	No	30
	LGA 1837	LGA, different pad size	LGA	No	30
	LGA133	LGA, same pad size for signal and ground	LGA	Yes	20
	LGA 118		LGA	No	20
	BGA196	BGA, 1mm pitch	BGA	Yes	20
2. Pretin Components (less voiding)	QFN32	Typical QFN, 0.5mm pitch	QFN	Yes	30
	QFN88	Typical QFN, 0.4mm pitch	QFN	Yes	30
	QFN132	Dual row QFN, 0.5mm pitch	QFN	Yes	20
	QFN52	Non symmetrical QFN	QFN	Yes	30
	QFN 3550	Non symmetrical QFN	QFN	Yes	30
	QFN 3837	Non symmetrical QFN	QFN	Yes	30
	FQFP176	FQFP	FQFP	Yes	30
	LGA 2004	LGA, different pad size	LGA	No	30
	LGA 2005	LGA, different pad size	LGA	No	30
	LGA 1837	LGA, different pad size	LGA	No	30
	LGA 133	LGA, same pad size for signal and ground	LGA	Yes	20
	LGA 118		LGA	No	20
	BGA196	BGA, 1mm pitch	BGA	Yes	20

Sample Preparation

Previous studies [1-2] showed that more solder generally resulted in less voiding. To study the impact of voiding on reliability, we built boards using two different process conditions to simulate different voiding levels in the solder joint. In one process condition, boards were built using a regular stencil which resulted in more voids in the solder joint. In the other process condition, pre-tinned components were used. This condition typically had less voiding in the solder joint.

Thermal Cycle Test Conditions

The thermal cycle testing was performed in an air-to-air thermal cycle chamber, from 0 to 100°C with 10-minute dwell time at each peak temperature, and a temperature ramp rate and cooling rate of approximately 10-15°C per minute. The chamber profile of temperature versus elapsed time is shown in Figure 6.

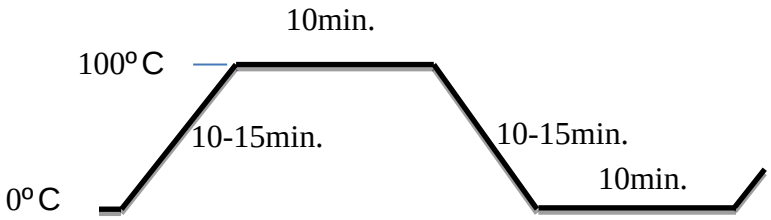


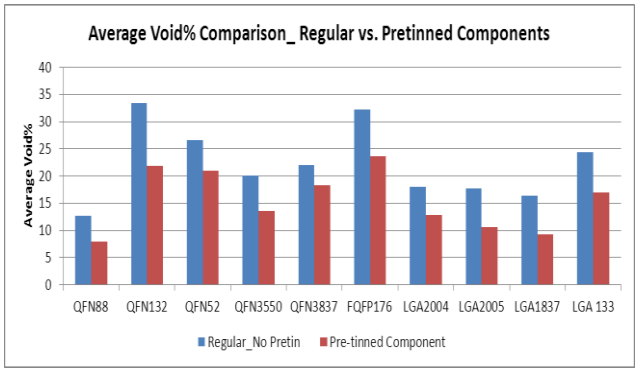
Figure 6 - Thermal Cycle Temperature Profile – 0 to 100 degrees C

Continuous monitoring was done on daisy chained components. Non daisy chained components were cross-sectioned after 1000 cycles, 2000 cycles and 3000 cycles.

Results and Discussions

X-Ray Inspection

Pre-tinned BTC components generally had less voiding than non-pre-tinned BTC components. However, voiding varied depending on the component type. Most of the components had an average void % of less than 25% except the dual row QFN132 component and FQFP176 component (Figure 7a). Maximum void percentage was seen up to 30%, 40%, 50%, depending on the component type, its pad size and process condition (Figure 7b).



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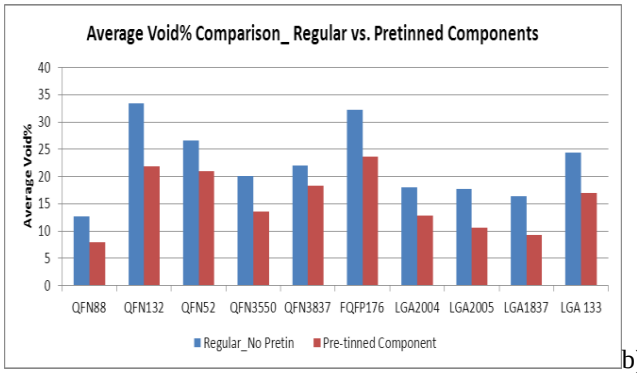
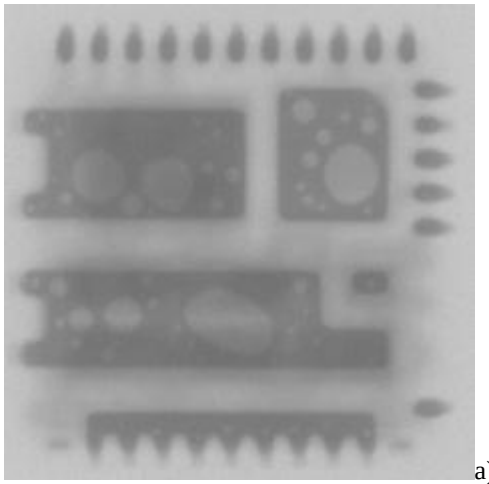


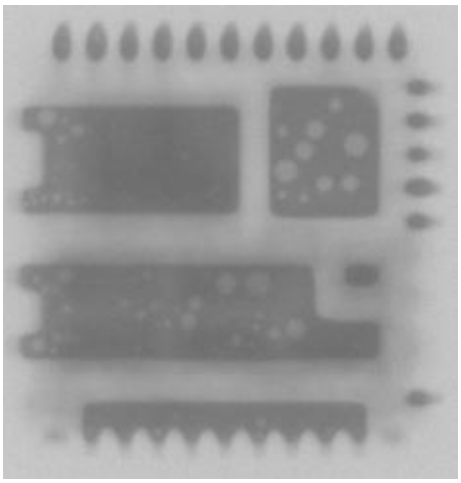
b)

Figure 7- Solder Joint Voiding Comparison for Sample Built with Pre-tinned BTC vs. Regular BTC. a) Average Void% b) Maximum void %.

Pre-tinned components did not eliminate voids. However, the size of the voids in the pre-tinned samples was typically smaller than the voids of solder joints using non pre-tinned component (Figure 8). The shape of the voids for pre-tinned sample was more defined and circular as compared to the non-pre-tinned solder joint sample (Figure 9).

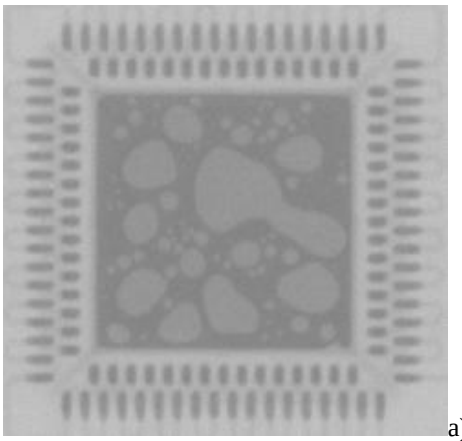


a)Non-Pre-tinned



b) Pre-tinned

Figure 8 - X-Ray Images of QFN 3550 Solder Joint Assembled with Non-Pre-tinned Component vs. Pre-tinned Component.


a) Non-Pre-Tinned

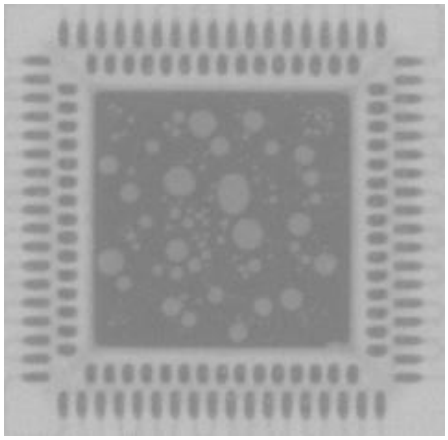

b) Pre-Tinned

Figure 9 - X-Ray Images of QFN132 Solder Joint Assembled with Non-Pre-Tinned Component vs. Pre-Tinned Component.

Solder Joint Microstructure – Time Zero Analysis

Cross sections of the BTC solder joints were performed to evaluate the solder joint microstructure and inter-metallic formation at time zero (prior to thermal cycle testing). Non-pre-tinned components had a standoff height of about 2mil to 3.5mil, depending on the component type. The pre-tinned component standoff height was between 4-7mil. It was approximately twice of the non-pre-tinned component standoff [Table 2]. The BGA196 component had a standoff height of around 11mil.

Table 2- Solder Joint Standoff Height of BTC Assembled Using Regular Process and Pre-tinned Components

Component ID	Solder Joint Height _ Regular_No Pretin [mil]	Solder Joint Height _ Pretined Component [mil]
QFN32	2.87	4.61
QFN88	2.28	3.56
QFN132	2.23	4.58
QFN52	2.83	3.79
QFN3550	3.22	6.42
QFN3837	3.52	5.89
FQFP176	3.12	3.74
LGA2004	2.99	6.73
LGA2005	3.14	7.07
LGA1837	3.46	6.22
LGA 133	3.5	7.06
BGA196	11.14	N/A

Good solder joint wetting and normal IMC layers were observed for all the components. No cracked solder joints were found at time-zero for all the samples (Figure 10, Figure 11 and Figure 12).

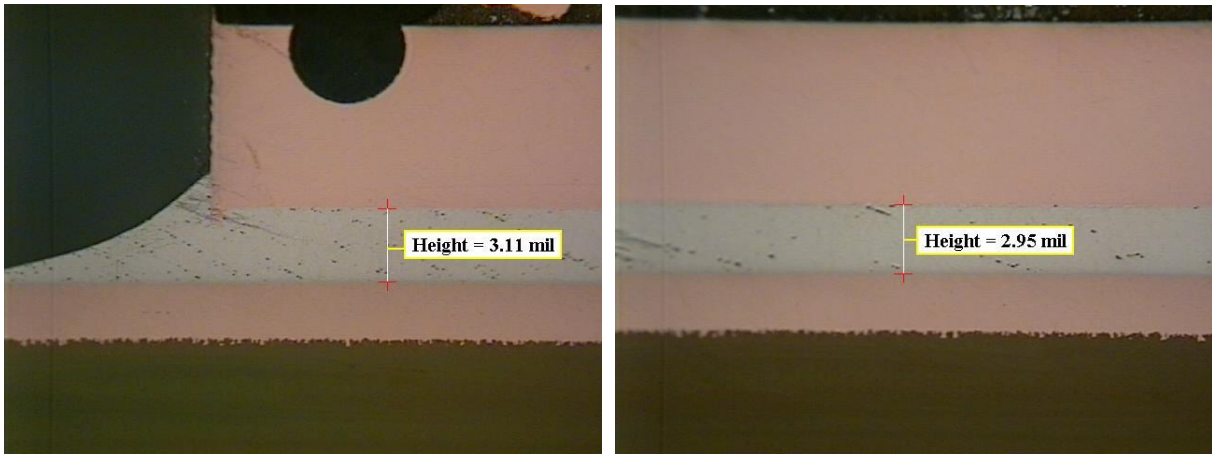


Figure 10 - Cross Section Images of a QFN component at t=0_ Non-Pre-tinned Component

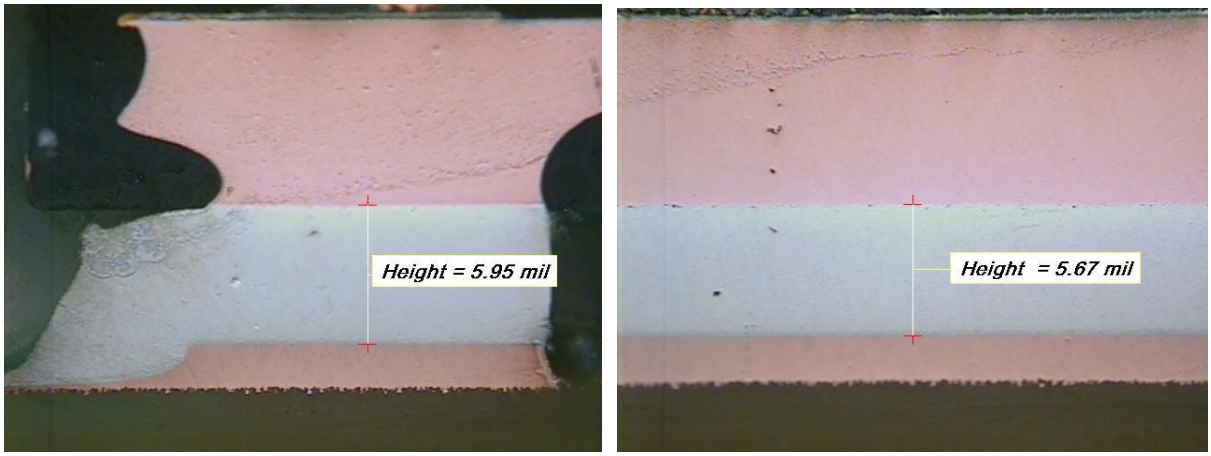


Figure 11 - Cross Section Images of a QFN Component after Reflow_ Using Pre-tinned Components

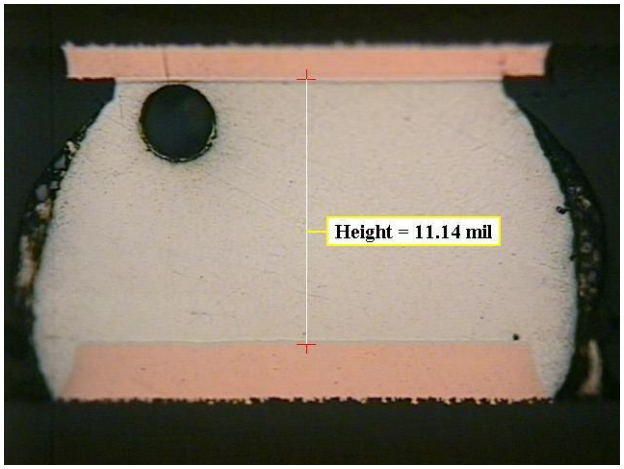


Figure 12 - Cross Section Images of BGA Component after Reflow

Failure Analysis after 1000 thermal cycles

The components were cross sectioned after 1000 cycles. Minor cracks were observed for some BTC components. Cracks were typically initiated at the edge of the component at the component side. No crack was initiated at the void location.

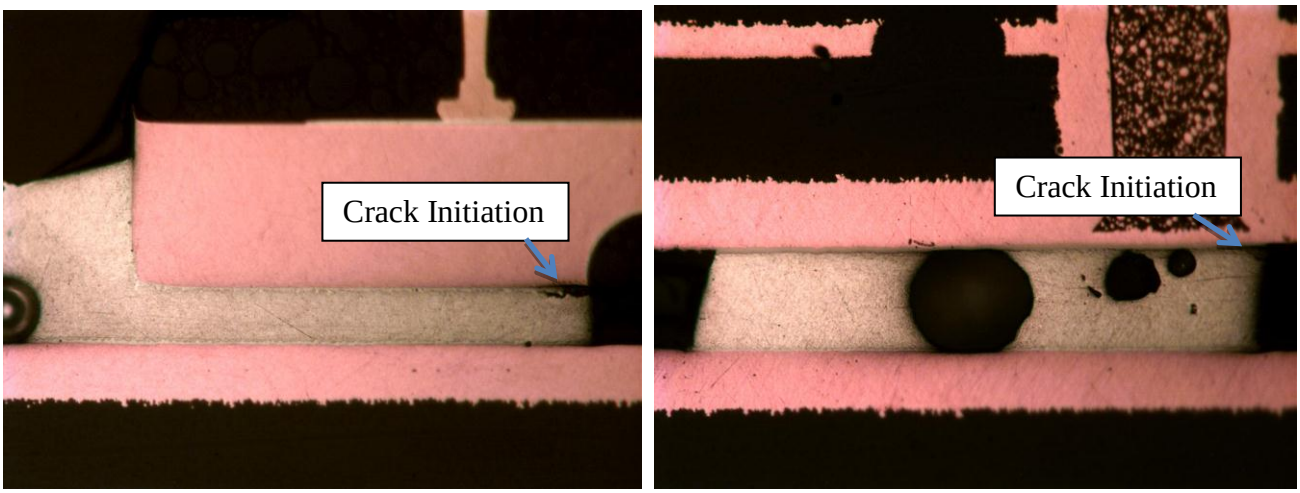


Figure 13 - Cross Section Images of BTC Component after 1000 Cycle.

Failure Analysis after 3000 thermal cycles

The thermal cycle test was terminated after 3000 cycles. No failure was observed for the daisy chain components after 3000 cycles. Cracks were more pronounced at certain BTC components such as the QFN132, QFN52, QFN3550 and LGA1837 components. Most cracks were observed at the component side (Figure 14 and Figure 15). Some cracks at the middle of the solder joint were also seen (Figure 16). Most of the cracks and the more severe cracks happened at the signal pins of the QFN components or when there was a large mismatch in pad design of the component. Thermal pads of QFNs and many LGA components with large pad sizes did not have major cracks after 3000 cycles.

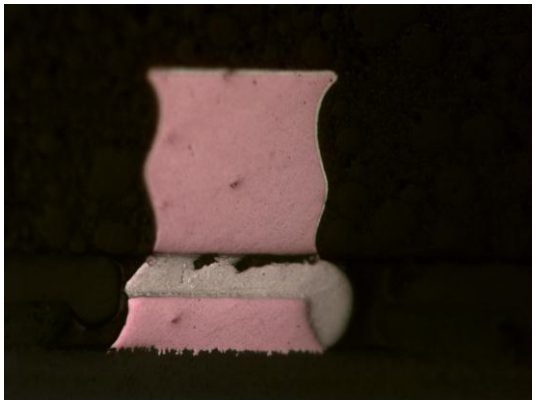


Figure 14 - Cross Section Images after 3000 Cycles for QFN52_ Non-Pre-tinned. Crack was usually seen at the component side.

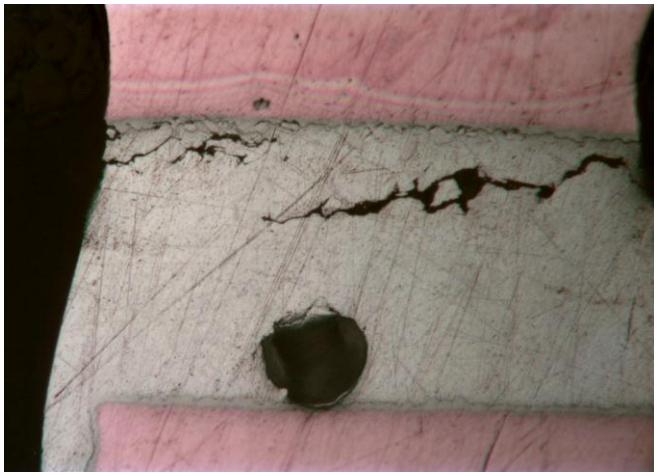


Figure 15 - Cross Section Images after 3000 Cycles for QFN88_ Pre-tinned Component. Cracks were seen at the component side and through the solder joint.

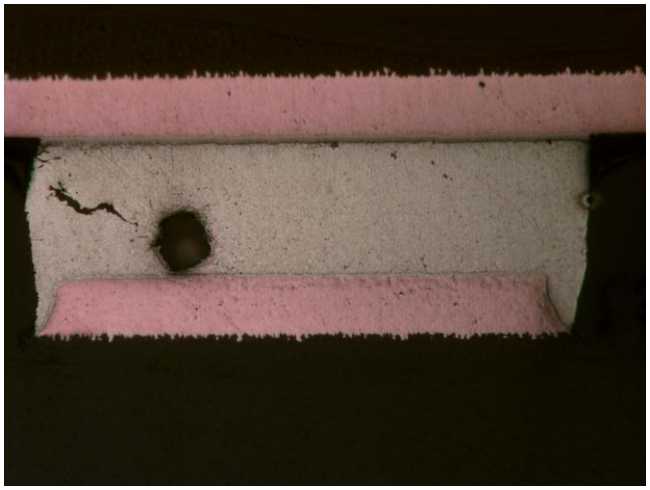


Figure 16 - Cross Section Images of QFN Component After 3000 Cycles. Crack initiated at the solder joint, not at the void area.

Thermal Cycle Test Summary

There was no correlation between voiding amount at the thermal pad of the BTC and its solder joint thermal reliability. Crack were not initiated from the voids. There was a lack of evidence that voids in the thermal pads accelerated solder joint cracks.

BTC Thermal Modeling

In this study we evaluated the impact of solder voids in the thermal pad of the BTC. The experimentation was done by creating a BTC model and using a thermal simulator to evaluate the heat transfer to the ambient air and PCB. The model includes all single elements in a BTC like packaging mold material, copper pad frame, lead free solder, PCB and copper traces. Also, silicon dies with dimensions and power dissipation information are included. After validating the model by comparing the results with the thermal behavior from the component supplier several voiding conditions were created from 0% up to 98% voids by changing the thermal resistance of the tin based solder and reading the surface temperature of the package. Additional scenarios were created by changing the power dissipation of the package and plotting the results.

Component Selection

For thermal simulation, we used a DC to DC regulator QFN IR3837. This chip incorporates a PWM controller IC and two power Mosfets (control and synchronous FET). This device can operate at different currents and shows considerable power dissipation that facilitates the analysis of the impact of solder voiding.

Model Development

All the parts from the package were constructed with the primary blocks available in the simulator; with properties like geometry, material type, thermal conductivity and power dissipation assigned to each part and joined all together as shown in Figures 17 and Figure 18.

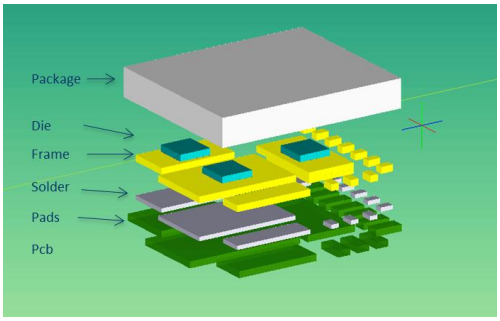


Figure 17 - Model Blocks

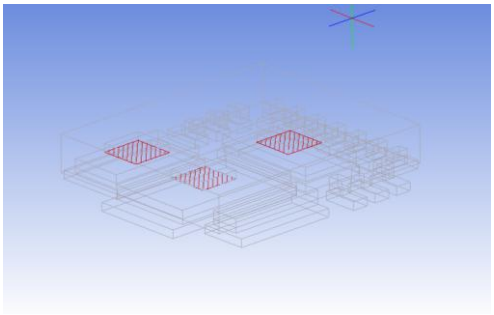


Figure 18 - Device Model Assembled

Model Validation

The model validation was done comparing the thermal behavior of the model against the information provided by the supplier, with the data recorded in Table 3. The analysis involved power dissipation at different currents resulting in a correlation index of 99% as shown in Figure 19.

Table 3 - Thermal Results from Model and Device Supplier Data

	IR Online Simulation Results				Icepack Results			
Device Current	Surface Temp	Crtl Fet	Sync Fet	Crtl IC	Surface Temp	Crtl Fet	Sync Fet	Crtl IC
2	37.39	37.15	37.44	37.44	36.7173	36.2868	36.9879	36.6717
4	41.26	41.1	41.33	41.21	42.6512	42.3661	43.0389	42.0689
6	46.87	46.51	46.97	46.67	49.6425	49.4236	50.1919	48.366
8	54.7	54.65	54.84	54.07	57.8273	57.6326	58.5849	55.6779
10	65.47	65.36	65.67	63.24	67.8698	67.7119	68.8932	64.6095
12	75.66	75.97	75.77	72.66	78.76	78.57	80.09	74.23
14	86.53	86.32	86.79	83.02	89.89	89.58	91.56	83.99

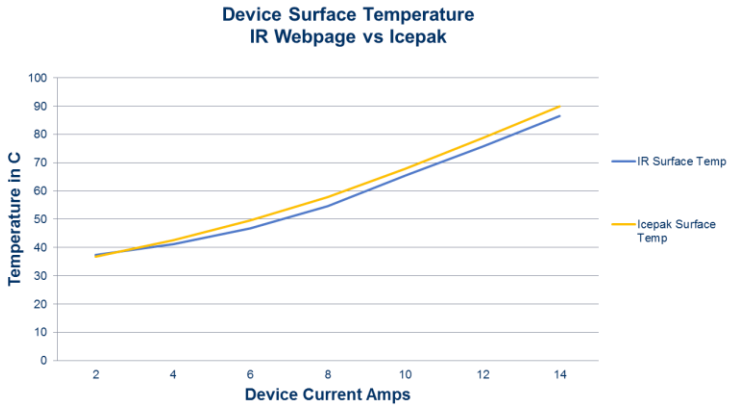


Figure 19 - Temperature Behavior from Model versus Device Supplier Data

Evaluation of Voiding Scenarios

With a good model that closely matches the results from the supplier data, the next step is to evaluate the voiding scenarios from 0% voids up to 98% voids and measure the temperature at the surface of the device at power dissipation from 0.5 up to 3.5 Watts. The results are plotted in Figure 20. These results revealed that the voiding percentage has minimal impact on the temperature reached by the product.

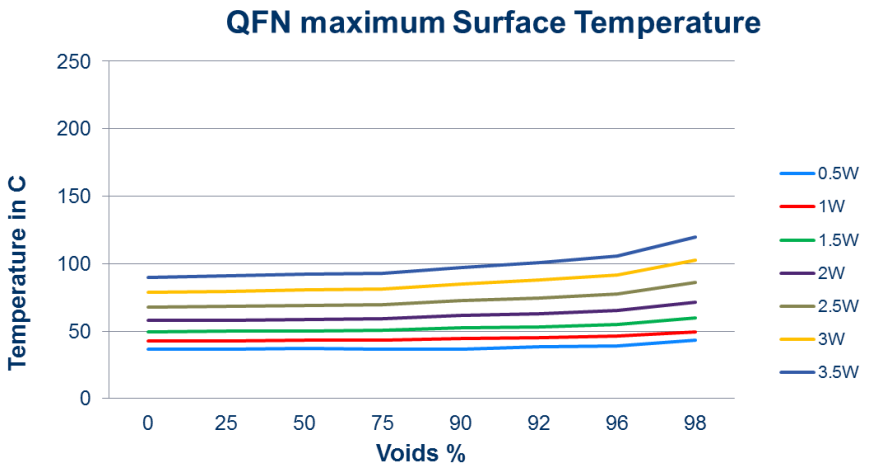


Figure 20 - Solder Voiding Impact on the Device Temperature at Different Power Dissipation

Figure 21 shows the results from the simulator in the scenario of 75% voids and 3.5W. The maximum temperature reading at the surface of the device was around 92°C. The internal semiconductor dies showed a maximum temperature of 95.4C for Synchronous FET and 91.9°C for the control FET. The control IC reported 84.3°C. Despite the solder voiding percentage in the thermal pad being 75%, the device was dissipating 3.5W, with the semiconductor die temperatures well within the specification for this device.

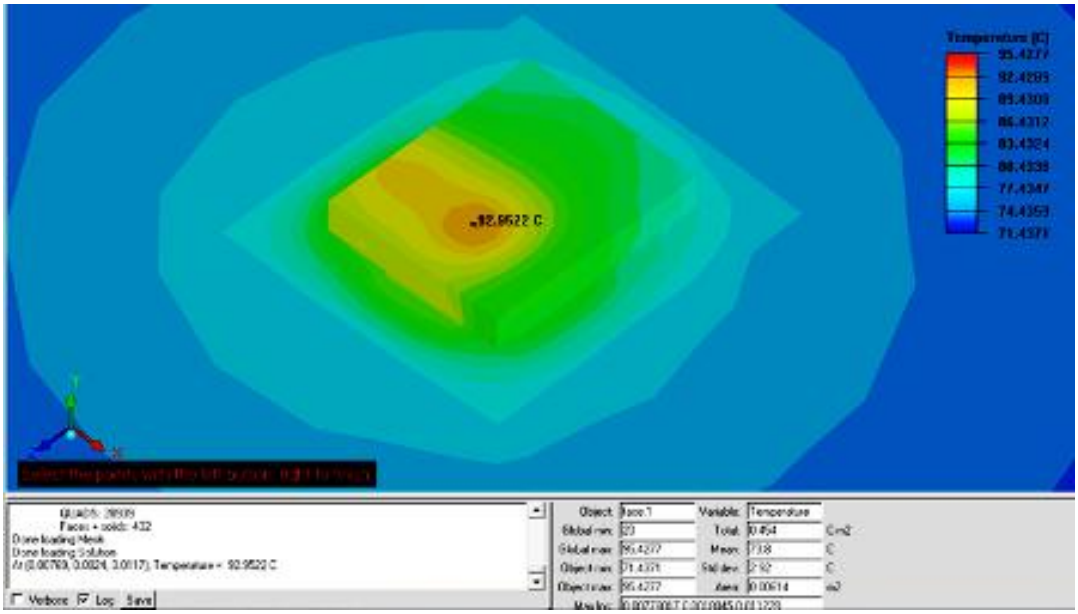


Figure 21 - Simulator Results for a Scenario of 75% Voids and 3.5W

Thermal Study Summary

With the aid of the thermal simulator it was possible to create and analyze solder voiding conditions in a BTC package that is difficult to do experimentally. The data indicates that the voiding in the solder joint does not significantly impact the temperature increase of the device because the rest of the elements in the package also help to conduct the heat generated. From the information collected it is possible to state that up to 50% of solder voiding in a thermal pad is acceptable for devices with power dissipation below 3Watts.

Conclusions

The study showed that voids did not initiate cracks in the solder joint of BTC components during thermal cycle testing from 0°C to 100°C. The data did not show that voids facilitate solder joint failure. Solder joints of small signal pins typically had

more severe cracks and would fail first. Thermal pads usually had more voiding, but lesser cracks were observed after 3000 thermal cycles. The thermal modeling study indicated that voiding did not significantly impact the temperature increase of the device with power dissipation of about 3Watts. Further analysis would be done evaluating the thermal behavior of other BTC configurations and trying to validate with known performance of real components.

Acknowledgements
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