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RELIABILITY CHALLENGES FOR BOTTOM TERMINATION COMPONENTS

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ABSTRACT:

There are many facets to PCB reliability and also a variety of strategies to ensure the most reliable assemblies. Bottom termination components, such as BGAs, CSPs, MLFs, QFNs, and D-Paks, pose additional challenges to some aspects of reliability. Three aspects will be addressed: electro-chemical reliability, assembly defects, and alloy reliability. For each aspect, unique challenges for BTCs, solutions, and strategies for optimization will be discussed. In order to maintain the highest quality of PCB assembly, all three must be considered and addressed at different phases of design and production.

Key words: bottom termination components, QFNs, reliability, voiding

INTRODUCTION:

Complex components designed to keep up with the demand for electronics with ever-expanding capabilities are challenging the performance of traditional solder pastes. The complexity of large arrays of small solder joints, such as BGAs, or a perimeter of small solder joints around a large pad, such as bottom termination components, requires finer precision and alternative approaches to maintain the highest quality PCB assembly. Components with these characteristics have been well-studied and several approaches have been proven to improve the reliability of these assemblies.

The combination of many small solder joints, along with a

large, confined solder joint in the center of these components causes unique challenges for bottom termination components. These challenges are present in all phases of PCB assembly: design, printing, reflow, cleaning, and both electro-chemical and alloy reliability. For each of these stages, approaches that have been proven to eliminate and improve these challenges are discussed and some initial results of ongoing testing demonstrate application of these improvements.

ASSEMBLY CHALLENGES:

In order to have any chance at long-term reliability, assemblies must have well-formed solder joints, and bottom termination components have unique challenges. The most common defects are head-in-pillow, non-wet opens, and voiding. Head-in pillow defects and non-wet opens are different types of improperly formed solder joints resulting from component warpage. Often, these defects will only affect one or a few of many connections on a component. Early detection of these defects is a further challenge because these connections can be conductive after reflow due to contact, but can easily be disrupted. X-ray detection can also be a challenge because these improperly formed solder joints often look the same if observed just in the zdirection.

In order to compensate for the challenges caused by component warpage, solder pastes have been modified to accentuate several properties: tackiness to maintain contact between the solder ball and paste as they are pulled apart; a wide reflow process window to accommodate different reflow profiling strategies; and a strong oxidation barrier, which maintains oxide-free molten solder surfaces to promote coalescence upon contact. Material solutions greatly improve solder joint formation for these defects, but there are some process considerations that play a role in forming the ideal solder joint. These will be discussed in the following sections.

Voiding can be present both in small solder joints, such as BGA balls or perimeter solder joints on a QFN, as well as in large solder deposits on a thermal pad. Because of the thermal requirements of these large solder deposits, large voids or a high percentage of voiding is unacceptable, and can cause components to overheat. Voiding is the result of two main mechanisms: non-ideal wetting to surfaces and entrapment of flux volatiles resultant during reflow. This first mechanism is often seen with older or improperly stored components or boards, so best practices are crucial for these complex assemblies. Entrapment of volatiles is a more complicated challenge because thermal pads are surrounded by other solder joints under components with low standoff heights. This causes all volatiles from the paste (50% by volume of which is flux) to escape through small channels on the edges of the solder deposit. In several previous works, Dr. Ning-Cheng Lee[1,3] has explored different ways to enhance the venting under these components, and his process solutions will be explored in the following sections.

Board Design Considerations

When incorporating these components into new board designs, there are ways to optimize pad geometries to create

a best case scenario for minimizing these defects. Voiding on thermal pads can be reduced by considering via size and placement, and thermal pad patterning.

When designing the thermal pad under a bottom termination component, there are a few approaches to take into consideration: breaking up the thermal pad into sections to create venting channels; deciding how large and how many vias are needed for thermal dissipation; and determining the placement of these vias. Dr. Lee has several studies published on many different patterns for thermal pad sectioning and has found that the critical factor is "venting accessibility"—the length of the venting pathways relative to the area of the pad. Another crucial discovery was that separating the thermal pad into sections with exposed board in-between the sections exacerbated voiding by allowing the board to outgas into the solder joint. Creating a pattern on the thermal pad by using solder mask facilitates venting by creating channels, and keeps the thermal pad continuous. Typically, stencil design for these patterned pads matches the pattern.

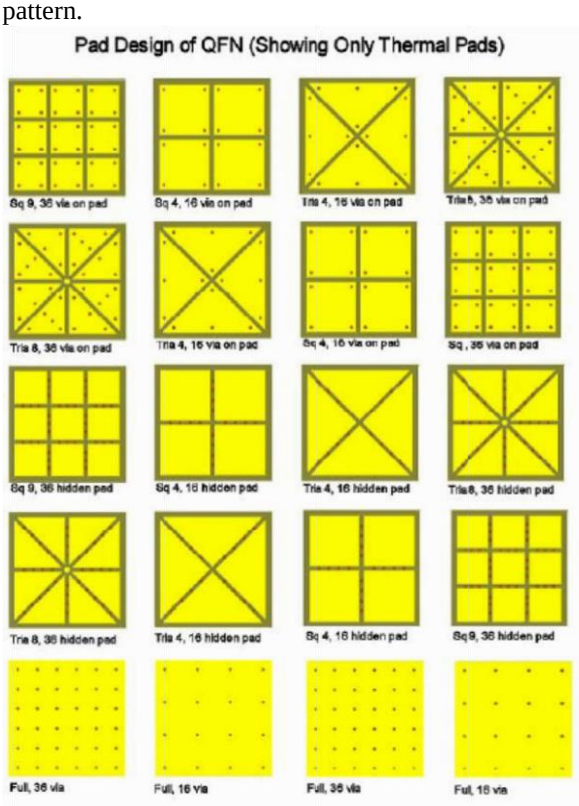


Figure 1. Pad design of the QFN test board showing thermal pad patterns[1]

In "The Effect of Thermal Pad Patterning on QFN Voiding"[1], Dr. Lee et al. calculated that venting accessibility is increased by having more channels. However, more venting area means more discontinuity in the solder joint. Therefore, choosing a pattern will depend on the size of the component and balancing the amount of venting area.

This concept was demonstrated in a recent study using a test board conforming to user specifications. Whereas the test board from Dr. Lee's study focused on 0.1mm width, 0.1mm depth vias, the user specified board design incorporated 0.2 and 0.3mm through-hole vias placed in the pad and in the pathway. The pathways, patterned with solder mask, were also wider on the more recent board.

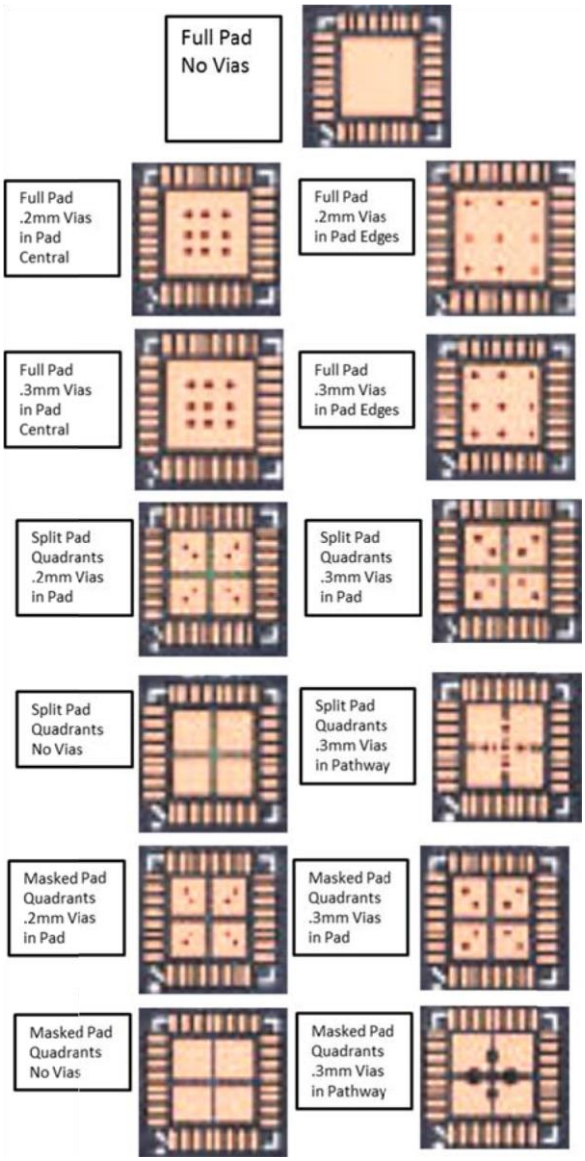


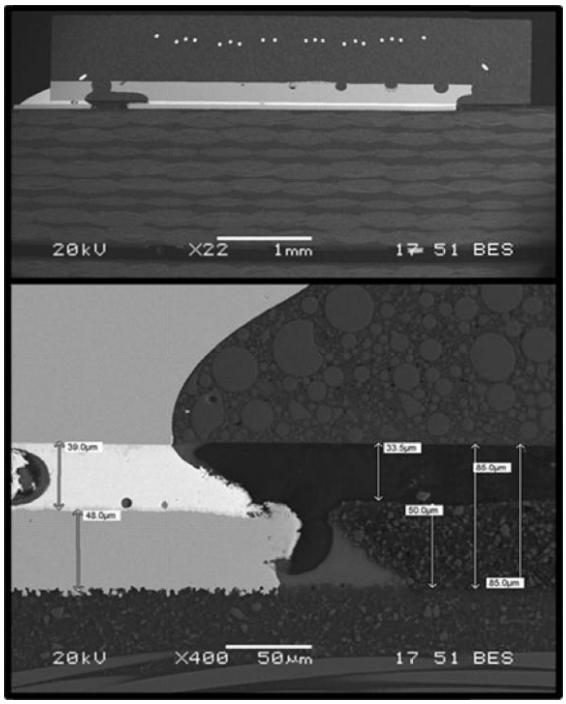
Figure 2. QFN thermal pad patterns tested

The quadrants pattern was chosen because of the small size of this component's thermal pad. Both separated pads and solder mask patterns (split and masked pads, respectively) were tested.

In this case, the benefits of thermal pad patterning were not fully realized because the channel width contributed considerably to the voiding area. It is important to balance the need for venting with the area of selective voiding.

Via placement also plays a significant role in reducing voiding by helping to dissipate large voids. As noted by Dr. Lee[3], the placement of some vias, particularly those near a channel, can create small voids that will help dissipate larger voids formed in the center of the solder joint. In this study, the vias were large and did not demonstrate these benefits. In fact, the only via designs with reasonable voiding performance were those with vias placed in the pathways.

Another challenge confronted with these via designs was the way solder volume wicked away from the thermal pad. This phenomenon was observed during inspection of crosssections to measure standoff height. Figure 3 illustrates the effects of via size and additional solder volume from a preform. When the components were cross-sectioned along the vias, it is clear that solder wets down into the via. This also explains the variance in appearance of the vias during x-ray analysis. Solder wetting down into the via causes lower standoff with insufficient solder alloy in the thermal pad area, potentially leading to more voided area. The lower standoff also causes the perimeter solder joints to spread on the pad outside the component area. This could pose a risk to the reliability of the perimeter joints as well. Work continues to further characterize this effect, but these results suggest that it is important to design blind vias or tented vias, if the vias are large enough to pull away significant solder volume.



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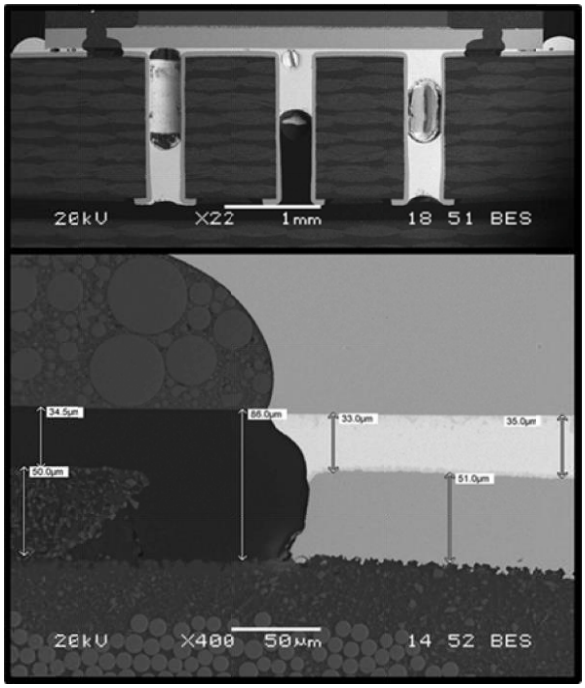

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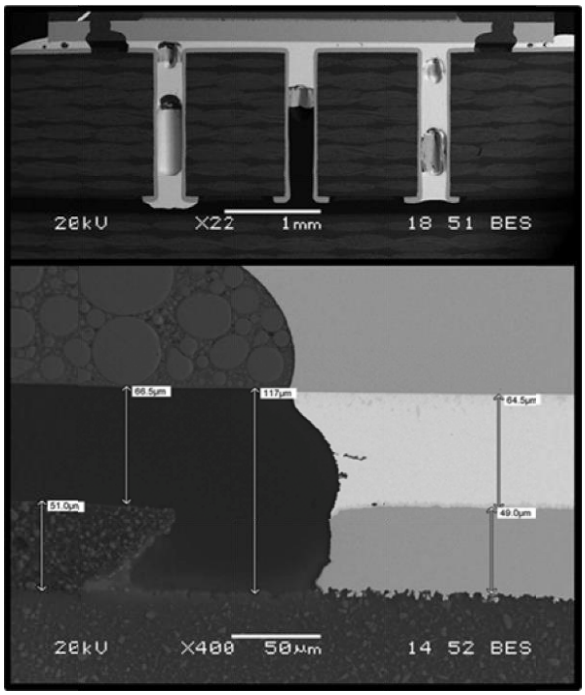

c.

Figure 3. SEM images of cross-sectioned components: a. full pad with 0.2mm vias; b. full pad with 0.3mm vias, paste and flux-coated preform; c. full pad with 0.2mm vias and flux-coated preform

Printing Challenges

Miniaturized components are often printing challenges. Apertures with area ratios less than 0.66 require application and adherence to best printing practices: sturdy board support,

high quality stencils, accurate aperture design, proper gasketing, and correct paste selection. Small deposits run the risk of insufficient transfer efficiency, or bridging if the deposit slumps or has excessive transfer efficiency Bridging occurs more often because of the fine pitch between these deposits as well.

Placement Challenges

Bottom termination components are complex, combining many solder connections into a small area, therefore, accurate placement is crucial. There aren't specific defects associated with improper placement; nonetheless, it is crucial to ensure that this part of the assembly process is repeatable. Placement force is also important to ensure that all pads or solder balls are in contact with the solder deposits before reflow.

Another case where placement has been researched is in the addition of preforms to the solder paste deposit under QFNs. This approach is considered in order to add solder volume to the thermal pad under the QFN. One aspect contributing to large area voiding is that solder paste is typically about 50%

flux, therefore, the volume of this space below the component is rarely filled with solder alloy after reflow. In

order to add alloy volume without adding flux, solder

preforms can be added to the paste. A flux-coated solder preform can be pick-and-placed into the paste, leaving a

small perimeter of paste around the preform on the large solder deposit. The component is then placed on top. In this case, placement pressure is crucial to not cause deflection of the preform or to squeeze out the paste, but also to make contact on all areas of the component.

Reflow Challenges

Reflow profiling is dependent on solder paste material. For some paste formulations, a ramp profile is ideal for dissipation of volatiles or to minimize head-in-pillow defects, whereas other formulations perform much better with a soak profile. Sometimes the temperature range for the soak is crucial. Another challenge of reflow profiling with these components is that most assemblies will combine a variety of these components, all with different requirements.

Figure 4 shows x-ray results for a typical solder paste, compared to one optimized to minimize QFN voiding. The challenge was to find a balanced profile that would minimize QFN voiding while maintaining BGA solder joint reliability as well.

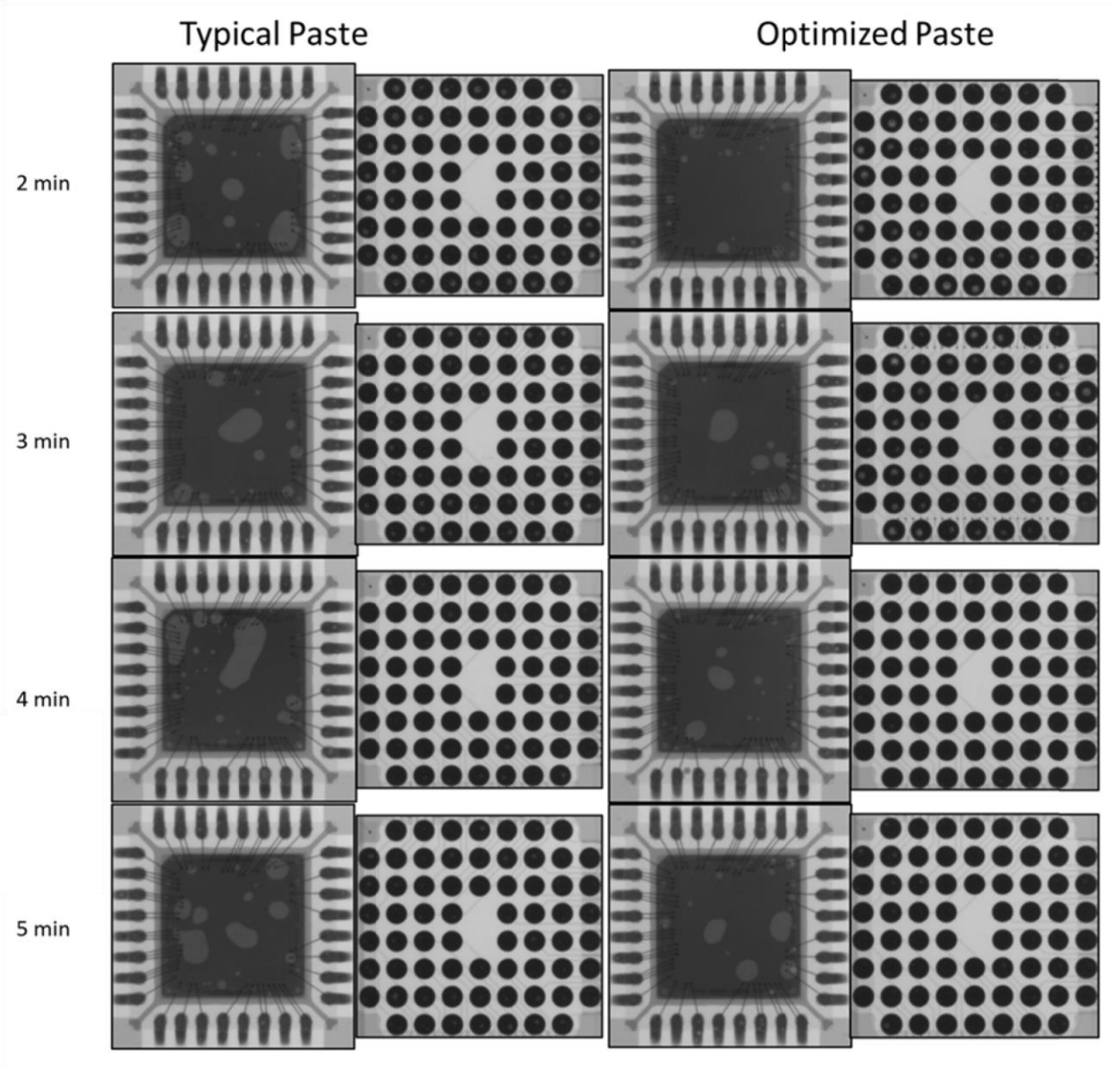

Figure 4: X-ray comparisons of reflow performance for QFNs and BGAs with a typical paste and a paste optimized to minimize QFN voiding

ELECTRO-CHEMICAL RELIABILITY:

Once the assembly is properly assembled, electrochemical reliability needs to be considered. Because these components have many connections and are close to the board (low-standoff), traditional water-wash processes are not able to remove flux residues trapped underneath. Water has a surface tension that is too high to get under the component and remove flux residues. Some solutions have been presented using chemistry to clean, but the question is always posed: "What will remove the cleaner?" No-clean solder pastes have proven to be a much better choice in these cases. The concern is that materials that require cleaning run a high potential for electro-chemical migration when not properly cleaned.

Eric Bastow has presented work simulating performance under low standoff components[2], using a glass slide over a comb-patterned SIR board. Because of this preparation, the glass slides were able to be removed after SIR testing to witness the nature of the flux residues. All water-wash formulations did not pass this testing, while most no-cleans did. After the glass slides were removed, it was found that the no-clean flux residues were not cured as well, or they were softer than exposed flux residues. This underscores the importance of considering the electro-chemical performance of materials, especially with low-standoff components.

LONG-TERM ALLOY RELIABILITY:

Long-term reliability of assemblies is dependent on proper solder joint formation. Testing of assembled boards is crucial to characterize potential defects before these devices are in operation. Often, testing is carried out on each type of assembly because these complex components pose unique conditions. BGAs have long been used in thermal cycling and drop tests because of the number of small solder joints per package. Small solder joints have a higher potential for fracture along the IMC layer than solder joints with a larger pad area.

Components assembled with excessive voiding will also have decreased reliability. In the case of voiding on the thermal pad, this can shorten the component's lifetime due to higher operating temperatures and insufficient thermal dissipation.

CONCLUSION:

These components are already being used in various electronics assemblies and can be reliably and repeatably assembled. These proven approaches can be used alone or in combination to achieve continuous improvement. The strategies behind these studies define parameters in which to consider areas of process optimization: board design (pad patterning, via placement), printing process (best practices, aperture design), placement, reflow profiling, cleaning, and reliability. Using materials such as specially designed solder pastes and flux-coated solid solder preforms also solve these challenges.

Research is on-going for several of these approaches. The full results associated with the preliminary examples presented here will be published at IPC ESTC in May, 2013, and SMTA International in October, 2013.

REFERENCES:

1. Lee, N.C., et al., *The Effect of Thermal Pad Patterning on QFN Voiding.* APEX, 2012.
2. Bastow, E. *The Effects of Partially Activated No-Clean Flux Residues Under Component Bodies and NoClean Flux Residues Entrapped Under RF Cans on Electrical Reliability.* APEX, 2011.
3. Lee, N.C. et al., *Thermal Pad Design and Process for Voiding Control at QFN Assembly.* APEX, 2011.
4. Homer, S., Lasky R.C. *Minimizing Voiding in QFN Packages Using Solder Preforms.* SMTAI, October2011.