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Preparing for Increased Electrostatic Discharge Device Sensitivity

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Abstract
With the push for ever improving performance on semiconductor component I/O interfaces, semiconductor components are being driven into a realm which makes them more sensitive to electrostatic discharge, potentially increasing in sensitivity by 50% every 3-5 years. Today, the majority of modern day semiconductor components are being designed to meet 250Volts of charge device model sensitivity, and that could decrease to 125Volts in the next 3-5 years, and could again decrease to 50Volts-70Volts in the following 3-5 years. The entire electronics industry must prepare for this challenge.
In preparation for this upcoming challenge, we along with some other semiconductor companies are embarking on an educational awareness and preparedness initiative with ODM's/OEM's. This includes awareness of the industry technology roadmap, and educating them on what they need to do to prepare for this challenge. As part of the preparedness initiative, we request that they start considering real time electrostatic discharge (ESD) detection within their "high-risk" modules; such as automated surface mount equipment, where direct measurements have confirmed semiconductor components are directly exposed to ESD events.
The call to action for automated surface mount equipment manufacturers is to start to evaluate, and implement, real-time ESD detection technologies in areas where direct contact with the component (i.e.. pick and place) occurs, and incorporating this real-time detection into their new equipment designs, as well as preparing retrofit kits for existing equipment sets. This is not a trivial task and will require time to develop and implement, so we urge the equipment manufacturing community to begin the process now in preparation for the increase in device sensitivity. In this paper, we will share what has learned about real-time ESD event detection in hopes it aids the equipment manufacturer's preparedness.

Introduction

Semiconductor components continue to push the envelope in looking to provide the customer outstanding performance and value. This is in part accomplished by reducing transistor geometry, and innovative circuit and package design. These three aspects will be focused on as they have a direct impact on the performance of the component as it relates to "ESD survivability." As process technology progresses, transistor size decreases, See Figure 1. The reduction in transistor size has a direct impact on the ability of a given transistor to withstand the effects of an ESD Event.

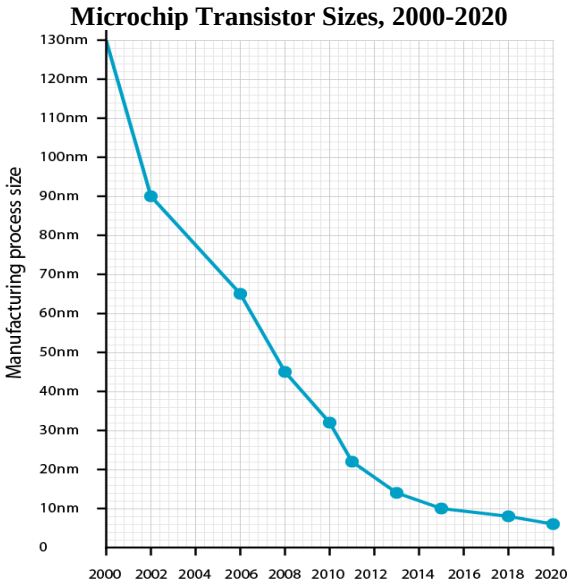

Figure 1.[i]

A contributor to this increase in transistor level ESD sensitivity is gate oxide thickness. As the gate oxide becomes thinner (See Figure 2.) it becomes prone to "breakdown," when exposed to the stresses of an ESD event. This can lead to the immediate

destruction of the transistor, or it can lead to a "weakening" of the transitor. The latter is of major concern as it may result in transistor current leakage, which may result in degraded transistor performance, or worse yet, it can lead to a "latent" transistor failure that does not manifest itself until later in the life of the transistor.

Gate Oxide Thickness Trend

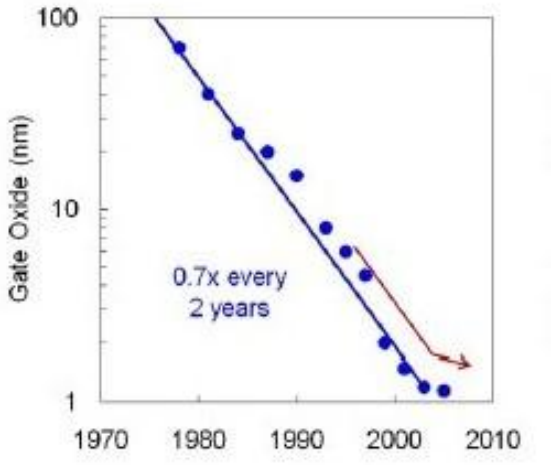

Figure 2.[ii]

Semiconductor component performance is often gauged in terms of data transfer rate performance. It is often stated; "The faster the data can be reliably transferred, the better." The trend for higher data transfer rate performance is only expected to increase as we look to the future (Figure 3.) To this end, semiconductor component designers are tasked with achieving this deliverable, at the component level. This is often accomplished through innovative designs and layouts, at the transistor level. There is a time though, when the laws of physics place hard barriers on the designers. One such physics barrier is component I/O capacitance. The higher the I/O capacitance, the lower the data transfer rate performance, and conversely, the lower the I/O capacitance, the higher the data transfer rate performance. This is where the problem herein lies, from a component level ESD survivability perspective. If the customer demands high data transfer rate performance, the designer is left with having to reduce capacitance in the signal path. When one looks at the I/O design of a typical semiconductor circuit, they find that the ESD protection diodes are right at the end (output) of the component circuit I/O signal path, and for good reason (See Figure 4.) I.e. The I/Os lead into the component, and must be protected from external high-speed electrical stressors, such as ESD. The protection diodes have a relatively high capacitance, and that capacitance limits data transfer rate capability. The only way to physically achieve high data transfer rate performance is to reduce the size of the ESD protection diodes. This translates to exposed I/Os being less robust to ESD effects. This becomes a concern once the component is packaged and has I/Os that are facing "the outside world," and are being handled by equipment and personnel that have the potential to electrically discharge to an I/O.

High Speed I/O Transfer Rate Trend

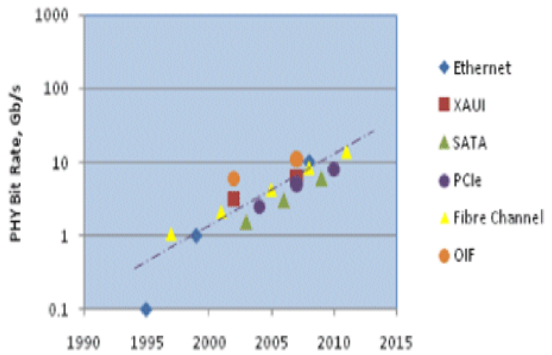

Figure 3.

Typical Double Diode ESD Protection[iii]

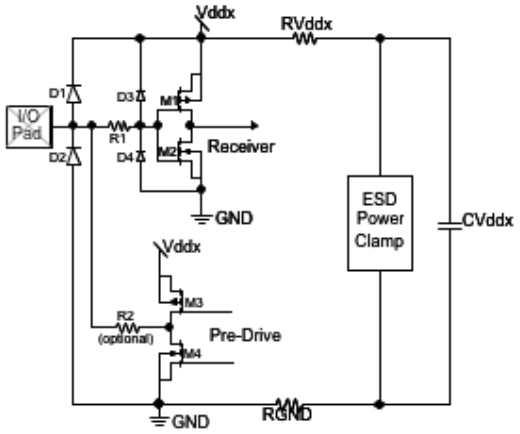

Figure 4.[iv]

Package size, or more specifically, package surface area, directly contributes to the amplitude of the current discharged from an electrically charged component (See Figure 5.). The larger the component (larger the surface area), the larger the current associated with the electrical. One way to visualize this is to think of the component as a water bucket, and the water within the bucket as electrical charge. The larger the bucket, the more water it can hold. The same principal holds true for a component, in terms of electrical charge. I.e. the larger the component package (larger surface area), the more charge it can hold. This increase in electrical charge carrying capacity relates to the amount of current that releases during an ESD event, where larger currents pose a high risk to the component.

Peak Current As A Function of Package Size (500V)

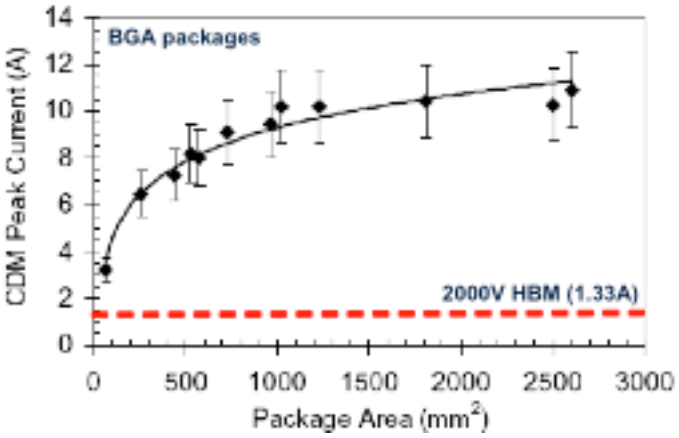

Figure 5.[v]

Reduced transistor geometry, increased I/O data transfer rate performance expectations, and potential increase in package surface area, have major implications to the electronics industry. One can expect higher component level ESD sensitivities as the electronics industry progresses into the future (See Figure 6.). All parties involved, from semiconductor manufacturer to electronics assembler must prepare for this challenge. This requires a higher degree of diligence in terms of electrostatic charge control in all manufacturing and assembly environments. Increased areas of focus should include, but are not limited to:

1. Selection and use of low charge generating, static dissipating materials within equipment and manufacturing/assembly environments. Particularly those items that will come into direct contact, or within 30cm of the ESD sensitive component. All items that come into direct contact or within 30cm should be characterized for static charge generation using items that are likely to come into direct contact with the component during manufacturing/assembly and maintenance activities.
2. Higher degree of diligence applied in terms of proper personnel grounding, equipment grounding, and facility level grounding. Ideally all items that will, or are likely to, come into direct contact with the ESD sensitive component should have a static dissipative path to ground. This includes the path from the point of contact with the ESD sensitive component, all the way to a known facility level ground.

ESD Sensitivity Roadmap (Charge Device Model)

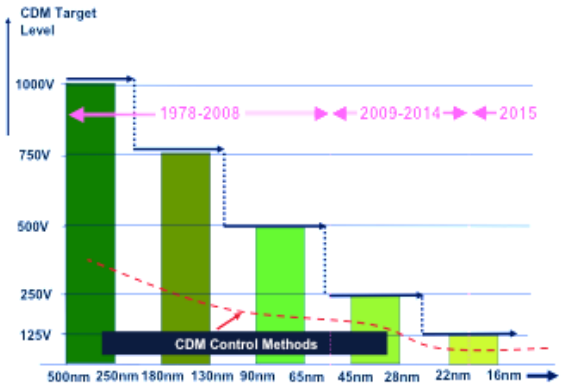

Figure 6.[vi]

If the measures described above are in place, and working as intended, ESD risk will be greatly mitigated. One issue is that it is not always possible to eliminate charge-producing insulators from the manufacturing/assembly process, nor is it always possible to provide static dissipative paths to ground from all items that come into contact with the component. In some cases air ionization can be used to neutralize the charge on the surface of the object, but it has its limitations in terms of how quickly (efficiently) it can dissipate charge. i.e. Many manufacturing and assembly operations occur at speeds that are much faster than a typical air ionization solution can dissipate a built up electrical charge.

Materials properties and performance can vary over time. It is not uncommon to have a material that was qualified as "ESD-safe" to be found to be an ESD risk at a later time. Much effort has been placed in attempting to understand these phenomena. Here are some of the findings.

1. Some materials are coated with antistatic or static dissipative layers, and those layers wear over time, leading to charge producing surfaces being exposed to the ESD sensitive component
2. Materials develop insulative films on their surface. Typically dirt or grime. These films/layers tend to be insulative and many lead to charge generation of the ESD sensitive component.
3. "ESD-safe" materials are unknowingly replaced with insulative materials, for whatever reason, during normal preventative maintenance activities. Ex. Suction cups
4. Homogeneity of the material itself. Variation in electrostatic material performance can occur across a given surface, from item to item, lot to lot, and over time. There are many theories as to why this is occurring, and there is enough material documented to warrant an additional paper on the topic.

This implies that one must be diligent about the ESD control program they have in place. One cannot say that they qualified a process, or piece of equipment, and therefore it must be "ESD-safe," for all time. This is an incorrect assumption. One must assume that ESD performance WILL vary over time, and therefore must be carefully monitored.

This is where real-time ESD detection is introduced. What is of great importance is whether an ESD event is occurring to the ESD sensitive component. For over a decade an oscilloscope coupled with an antenna, sensitive to electromagnetic emissions from an ESD event ,was used to identify whether ESD was occurring (Figure 7.)

Antenna and Oscilloscope

Figure 7.

The method of using an antenna and oscilloscope works quite well when the user knows how to set up the oscilloscope properly, and understands what the ESD signature looks like (Figure 8 and 10.) This method has been used numerous times to solve ESD issues in the past, and continues to be a vital tool in the ESD engineer's arsenal. The concern is that it only provides a "snap-shot" in time. This is because it is not practical to purchase and set up oscilloscopes and antennas at every area of concern throughout the manufacturing/assembly process.

Typical Antenna Setup to Detect ESD In Equipment

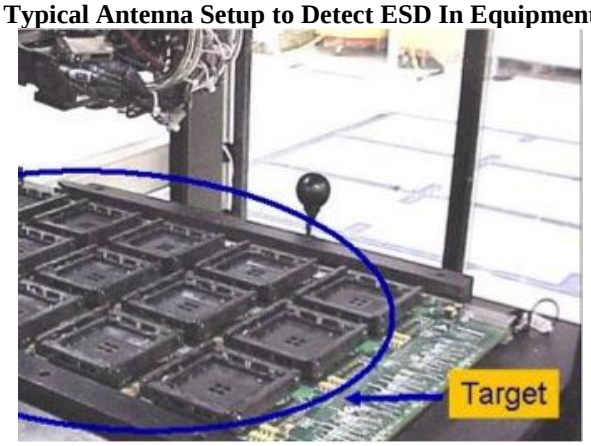

Figure 8.

This drove the need for real-time ESD detection (Figure 9.). A method was needed that was capable of accurately, and repeatedly being able to detect an ESD event. It had to be small in form factor so that it could be placed internal to equipment. It had to be relatively low cost, and it had to have capabilities of integrating with equipment so it could be internally powered, and provide output signals to the tools controller, or external controller, that in turn could be used to create an "action" by those monitoring the tool, or the event controller.

Block Diagram of ESD Event Detector

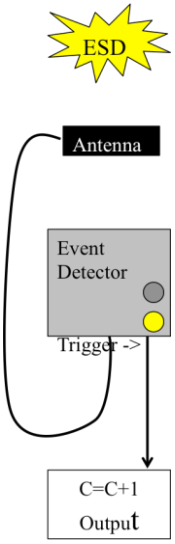

Figure 9.

Methodology

The project started by meeting with several electrostatic equipment manufacturers and relaying desired outcome and features of a real-time ESD event detector. This required strong collaboration between the parties. An important aspect of this discovery phase was to fully understand what was to be detected. The collaboration teams agreed that looking at the radiated signal of the electrostatic event would be the best approach. This required a thorough understanding of the radiated electrical characteristics of an ESD event. Data was collected using an industry standard charge device model tester as the discharge source. For this discovery work the receiving antenna was placed at a fixed distance from the discharge source, and numerous discharges were produced and recorded using an omni-directional antenna and oscilloscope (See Figure 10). The discharge target (component) was held at a constant surface area (capacitance), and a constant discharge voltage was applied (+250V in this case). It was determined that there were 3 major components associated with the radiated ESD event that would be

recorded. They were; Peak-Peak Voltage, rise time, and fall time. It was learned from these discharge experiments, which for detection purposes, the main variable was the rise time (How fast the signal appeared to the detector). For a typical charge device model ESD event, the rise times were measured to be in the 100's of Pico-seconds to lower 10's of Nano-seconds. It was interesting to note that there was slight variability in the amplitude and rise time of the discharge events from event to event. After further investigation it was determined that the variation was due to the air discharge mechanism itself. It was also found that fall time didn't play as much of a role as was initially thought, and was removed from the ESD detector design criteria. Because the event amplitudes varied from discharge to discharge, and knowing that in the "real world" there would be different amplitude of discharges, and the antenna-target distances would likely vary, it was determined that an adjustable threshold would be required.

Typical Radiated Signature of An ESD Event

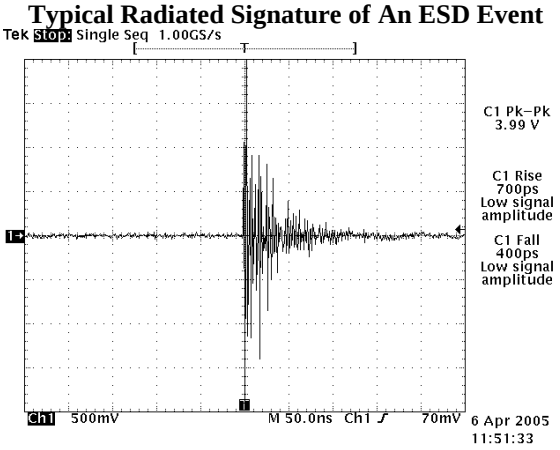

Figure 10.

A single manufacturer of ESD event detector was selected based on numerous criteria, and a project was initiated to further refine the ESD event detector concept. Initial investigation of the prototype detector was promising, but areas for improvement were identified. It became evident that proper antenna design would be key to the success of the project. The issue encountered was that the initial antenna sensitivity was too "high." This resulted in picking up signals from areas outside of the area of concern, leading to "false-triggering." A determination was made that a directional dipole antenna would be required, and the antenna was redesigned to be small enough to be usable in confined spaces. After several iterations, an antenna was finally designed that had minimal gain, had a small form factor, and was cost effective enough to pursue (See Figure 11.)

Example of ESD Detection Antenna

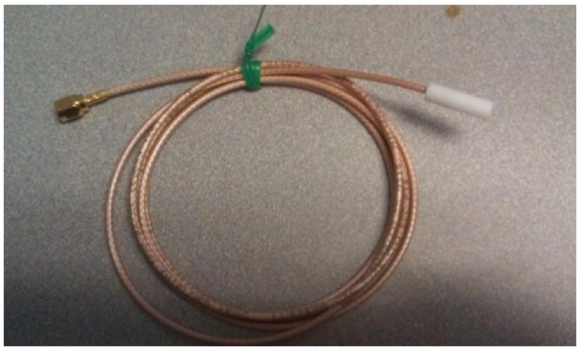

Figure 11.

Improvements were made to the internal circuitry of the ESD event detector to provide better resolution and stability. Essentially focusing on proper electromagnetic compatibility design practices and fine-tuning component selection. Effort was also placed on designing an easier to use and operate interface. These efforts resulted in a robust, user-friendly design.

The next stage of the project was to collect large data sets from equipment within the manufacturing environment/facility to show that the ESD event detector was ready for wide spread implementation. Numerous challenges were encountered during

this phase of the project. From how to safely install and route the antenna close to the target area in such a manner as not to interfere with the operation of the equipment see Figure 12.

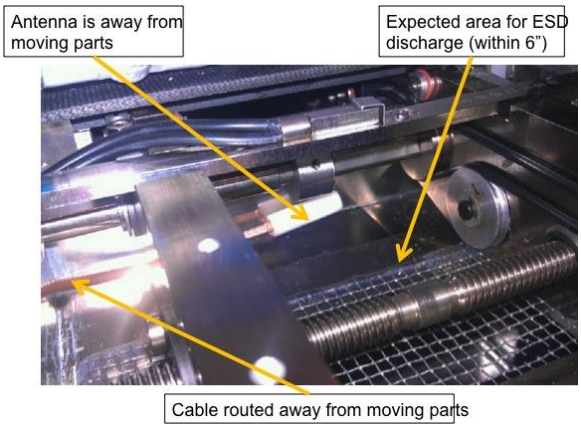

Figure 12: Example of Routing Antenna to a Target Location.

"Tuning" the detector so that it was capable of discerning an event of a given discharge voltage was found to be a challenge. It was initially hoped that tuning the event detector using the charge device model tester would directly translate for use in the equipment which was wrong. What we learned is that each type of equipment has its own unique discharge signature. At first this was very frustrating to the team. It was eventually understood that this was due to the radiation qualities of the equipment itself. You can think of an equipment chamber as an echo chamber, and the electromagnetic wave as a sound wave. You can visualize how different sizes and shapes of chambers and items within the chamber will effect how that sound will be heard at a given location, for a given input volume. That is what we were dealing with, except in terms of electromagnetic waves. This finding was key and drove the need for the introduction of a tool that would produce a known repeatable/reproducible quantity of charge that in turn could be discharged to an area of interest, and from that, could be used to calibrate the ESD event. This proved to be a key turning point. The team embarked on developing a charge tool, and within months a tool was available for trial (See Figure 13.).

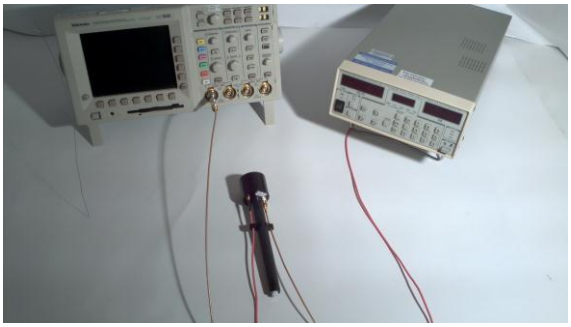

Figure 13: Charge Packet Generator Connected to Voltage Source and Oscilloscope.

The "charge tool" as it was termed provided very stable and repeatable discharges with great waveform shape (See Figure 14). Knowing what the capacitance of a given package was, and knowing the associated discharge current, one could replicate that charge packet in the manufacturing environment, on any tool, and get a meaningful correlation back to an industry standard test method (Charge Device Model tester). This correlation of what the charge device model tester recorded, and what was measured in the field, was of great value. It gave the user the ability to determine "real" risk in the end use environment.

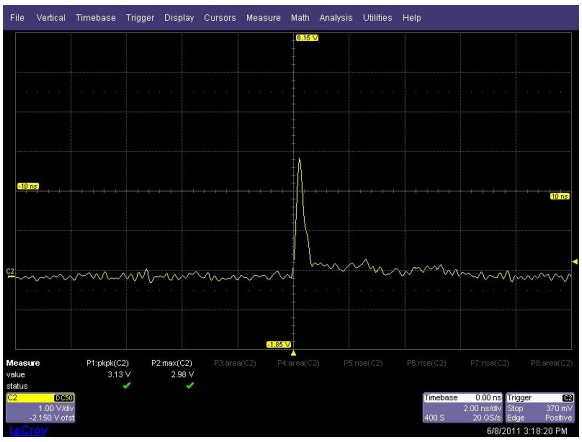

Figure 14: Shape of Discharge Current Waveform emitted by Charge Generation Tool.

Data

The data collected in the manufacturing environment showing how the ESD event detector performs is considered proprietary information and cannot be shared at this time. Below is a typical event detector set up table (Table1.) The ESD event detector is calibrated so that it triggers on events above a given level, and does not trigger on events lower than a target level. That trigger level is determined based on the sensitivity of the device to a charge device model type discharge. Because each event is slightly different from one another in terms of its peak-to-peak output voltage, a statistical approach was taken to determine the trigger level on the ESD event detector.

Column 1 is the sample point. Column 2 represents the discharge voltage applied by the power supply. Column 3 represents the tool being calibrated. Column 4 represents the location within the equipment being monitored. Column 5 represents the lower bounds of the recorded DC voltage measured from the ESD event detectors output. Column 6 represents the upper bounds of the recorded DC voltage measured from the output of the ESD event detector. Column 7 represents a statistically calculated value that shows the ESD detectors detection capability at a given location. In this example the ESD event has detection sensitivity of 17Volts at location 1, and 20Volts of detection sensitivity at location 2.

Example of Calibration Table

Table 1.

	Target ESD Voltage (V)	Test #	Power Supply (V)	Module	Location	LB Moving (V)	LB Moving (V)	Activation Delta from LB (V)
1	100	1	50	Test Tool	Entrance Gate	1.7	1.67	17.5
2	100	2	75	Test Tool	Entrance Gate	1.76	1.83	17.5
3	100	3	100	Test Tool	Entrance Gate	1.91	1.89	17.5
4	100	4	125	Test Tool	Entrance Gate	1.98	1.97	17.5
5	100	5	150	Test Tool	Entrance Gate	2.08	2	17.5
6	100	1	50	Test Tool	Testing Location	1.35	1.36	20
7	100	2	75	Test Tool	Testing Location	1.48	1.47	20
8	100	3	100	Test Tool	Testing Location	1.53	1.51	20
9	100	4	125	Test Tool	Testing Location	1.57	1.55	20
10	100	5	150	Test Tool	Testing Location	1.64	1.59	20

Conclusion

It has been shown that real-time ESD event detection is feasible, and that it can be directly related to what the component experiences in an industry standard charge device model tester. Its implementation does require the end user to expend engineering resources to calibrate and integrate into a given piece of equipment, but this effort provides the end user of the equipment the ability to determine ESD risk in real-time. That is a valuable asset as component level ESD sensitivities increase as process technology progresses, customer demand for increased data throughput performance increases, and package sizes remain large and can potentially grow in surface area.

The call to action for equipment developers/manufacturers, and end users, is to begin to investigate the implementation of real-time ESD event detection in future equipment designs, and also consider how this technology can be retrofitted into existing equipment configurations, if the need arises.

Addition information:
Additional information relevant to this discussion may be found at https://sites.google.com/site/esdpubs/documents/emc13-proof.pdf.

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[i] Future timeline.net image from Google images search. http://www.futuretimeline.net/subject/computers-internet.htm
[ii] i-micronews.com From Google images search. http://www.i-micronews.com/lectureArticle.asp?id=7607
[iii] design and reuse.com. From Google images search. http://www.design-reuse.com/articles/27135/ultra-low-jitter-wide-band-lc-pll.html
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