

PANEL LEVEL PACKAGING – A MANUFACTURING SOLUTION FOR COST-EFFECTIVE SYSTEMS

R. Aschenbrenner, K.-F. Becker, T. Braun, and A. Ostmann
Fraunhofer Institute for Reliability and Microintegration
Berlin, Germany
aschenbrenner@izm.fraunhofer.de

ABSTRACT

Developing demands and the market show two main trends helping to shape the ongoing development of system integration technologies. First of all is an ongoing increase in the number of functions directly included in a system — such as electrical, optical, mechanical, biological and chemical processes — combined with the demand for higher reliability and longer system lifetime. Second is the increasingly seamless merging of products and electronics, which necessitates adapting electronics to predefined materials, forms and application environments. Only by these means systems sensors — which are often installed in extremely harsh environments — and signal processing can be implemented near to the point where signals are occurring.

Large area mold embedding technologies and embedding of active components into printed circuit boards (Chip-in-Polymer) are two major packaging trends in this area. This paper describes the potential of heterogeneous integration technologies researched at Fraunhofer IZM with a strong focus on embedding in printed circuit boards and embedding in molded reconfigured wafers with an outlook of advanced large area encapsulation processes for multi chip embedding in combination with large area and low cost redistribution technology derived from printed circuit board manufacturing.

INTRODUCTION

Most electronic systems available today are realized through an organic printed wiring board, on which the individual components are placed. The wiring board is exclusively used with regard to electrical and mechanical function. However there are numerous attempts and necessity in the development of modern electronic products, which have to lead to the integration of further system functions into the board.

Future board and substrate technologies have to ensure a cost efficiently integration of highly complex systems, with a high degree of miniaturization and sufficient flexibility in adaptation to different applications. Their functionality will be considerably enlarged by integration of non-electronic functions such as MEMS, antennas or optical components. New production methods will ensure a high throughput at very low cost.

To ensure high data transmission and processing rates new cost effective cooling technologies and 3D-

Packaging concepts will ensure a stable operation mode. The following priorities are seen for multi functional board and substrate technologies:

- Embedded devices technologies
MEMS, passives, antennas, IC's
- Low cost finer line & smaller via substrate and interposer
- Impedance controlled wiring
- Flexible substrates (reel to reel manufacturing)
- Integrated optical interconnects

To reach these priorities new materials for embedding and encapsulation have to be developed:

- High K and low K dielectrics
- High Tg polymers
- CTE matching between dies and substrate

On the following pages an overview will be given on the recent technological developments towards heterogeneously integrated SiPs, focusing on embedding technologies.

EMBEDDING INTO PCB

Integration technologies for electronic systems or subsystems have attracted research and developments efforts in recent years. Device miniaturization and increasing functional density are pushing not only CMOS fabrication technologies to decrease feature sizes on the semiconductor devices. Also packaging, interconnection, and circuit board technologies have to keep pace with miniaturization requirements.

The EU-funded project “HERMES” [i] has initiated, with wide participation of European industries and research institutes, advancing the embedding technology borders at R&D level and more importantly of bringing embedding technology in real manufacturing PCB production [ii].

Embedding technologies offer the advantages of direct contact to the chips without use of long wires or solder bumps and thus improved electrical performance, capability of 3D-stacking, reduced package thickness if thin components are available, and enhanced thermal performance for components assembled on thermal interfaces and heat sinks, as in the case of embedding power components. The emergence of embedding packages steadily changes the packaging value chain and consequently sets new roles for all players in the whole packaging value system. The initial value share of substrate suppliers for production of FCBGAs was

about 20% but now with embedded technologies the substrate suppliers can also perform the assembly of components before embedding and thus count for 55% of the embedded package value [iii]. However, it should be underlined, that the shift to embedding technologies marks also necessary adaptations to the supply chain which will potentially burden the value system. For instance, the necessity of RDL layer for chip pitch enlargement that makes chip components compatible with existing embedding capabilities or copper pad deposition should be definitely accounted for before the shift in embedded packages. Initial applications for embedded packages will be low cost, low pin counts applications such as analog and power devices (DC/DC converters, Power MOSFETS etc.). There are forecasts for a half billion dollars extended market by 2015 [iii].

In a number of European cooperation projects with partners from industry and research, embedding of power chips, like IGBTs and power MOSFET, is of high interest [iv]. In this paper current achievements of these projects will be shown, especially examples of realized devices and their characteristics. The dominating technology for power chip embedding is a face-up technology. Chips are bonded with their backside (drain contact) to a Cu substrate using highly conductive adhesive or solder. Using the face up assembly, a direct contact to the backside of the die is possible, allowing a lot of benefits for driving high currents and applying an efficient thermal management for the power devices. Then the chips are embedded by vacuum lamination of prepreg or RCC (resin coated copper) layers. Via holes to the top contacts (gate and source) are formed by laser drilling. The vias are metalized using conventional Cu plating. Finally conductor structures are etched in the top Cu layer, finalizing the circuit.

On the following pages the technology developed in the EU-funded project “HERMES” is described whose scope is to further develop all embedding technologies at advanced R&D level and more importantly to bring embedding technology in real manufacturing PCB production with a concrete goal of embedding components in 18”x24” PCBs.

Power System-in-Package Demonstrator

The combination of two or more embedded dies e.g. MOSFET or diodes, but also controller chips, results in embedded Power System-in-Packages (*Figure 1*). Here the embedding technology offers a variable technology platform for the realization of a large variety of packages on the same process line. One big advantage of such packages is their short interconnects, resulting in low inductances which allow faster switching speed.



Figure 1. Embedded Power SiP

The project goal is to embed the power devices into the PCB and to place the application-specific logic devices and passives on top of the PCB.

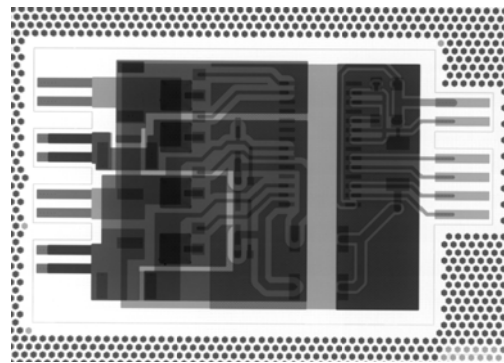


Figure 2. X-ray of a power module with four embedded power dies

This concept provides high flexibility for the logic parts combined with a careful power removal design for the power devices embedded in the PCB and isolated from the heat sink. The challenges for this solution are particularly great since in addition to the embedding process the high thermal conduction under electrical isolation has to be implemented. Therefore suitable materials for this isolation layer were investigated, which provide the needed thermal conductivity and fulfill the electrical isolation specifications. In *Figure 2* an x-ray picture of such an embedded power module, without the SMD components which will be assembled on top finally, is shown. The embedded MOSFET die has a thickness of 120 μm and is attached to a 70 μm thick copper foil using highly thermal conductive silver glue. Then the die is embedded into epoxy prepreg layers. The backside of the die is isolated to the thermal pad at heat sink location by a thermal laminate layer which is able to provide the needed thermal conductivity. In total the module is a four layer construction, containing four embedded power chips. All needed SMD components for the logic part are assembled on top of the module. These modules are currently under a fully qualification.

EMBEDDING INTO MOLDING COMPOUNDS

There are two main approaches for embedded die technologies:

First, there is the ChiP technology, the embedding of active dies into PCB as described above. Second, there is wafer level integration, where dies are embedded into polymer encapsulants and 3D vertical integration, where dies are embedded into the substrate. For wafer level integration a lot of activities are running worldwide. Main drivers are here the Embedded Wafer Level Ball Grid Array (eWLB) by Infineon [v] and the Redistributed Chip Package (RCP) by Freescale [vi]. Singulated dies are assembled on an intermediate carrier and encapsulated by compression molding, forming a polymer wafer with embedded silicon dies. This “reconfigured” wafer is then released from the carrier. Using thin film technology, an electrical redistribution layer is routed on the wafer.

Finally, the wafer is singulated by sawing into single packages. One trend in eWLB technology is at the moment a double sided eWLB packaging with integration of vias through the encapsulant by integration of preformed PCB based vias allowing the stacking of eWLB packages [vii].

The combination of both concepts embedding into polymer by molding and redistribution by PCB technologies has the potential for highly integrated low cost packages and was successfully demonstrated for a 2-chip LGA package [viii]. The direct integration of Through Mold Vias (TMVs) can be easily integrated in such packages as vias are a standard feature in the PCB manufacturing process and can be adapted for the proposed concepts of embedding into polymer by molding and redistribution by PCB technologies. A principle draft of a Package-on-Package assembly (PoP) based on a wafer level embedded package with PCB based redistribution technology is shown in Figure 3. Within this section the development and evaluation of such a packaging technology with TMVs is described.

Process Flow

The general process flow starts with the lamination of an adhesive film to a carrier. This special adhesive film has one pressure adhesive side and one thermo-release side, i.e. by heating up the tape above a certain temperature, the thermo-release side of the tape loses its adhesion strength. On this carrier-adhesive film sandwich dies are precisely placed, the active side facing down towards the carrier. High accuracy is needed as die pads have to match with the redistribution layer. Molding is done by large area compression molding.

For chip redistribution, low cost PCB based technology with RCC has been selected. After lamination of the RCC film on both wafer sides in one step, μ vias are drilled to the die pads and through mold vias in the same process step to connect to and bottom side.

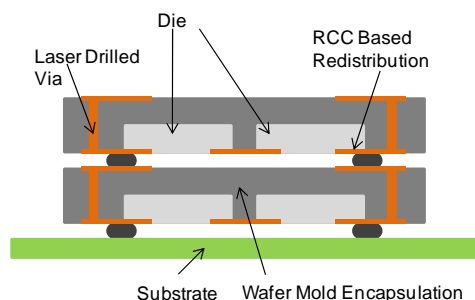


Figure 3. Schematic of a Package-on-Package assembly based on wafer level embedded package with PCB based redistribution technology

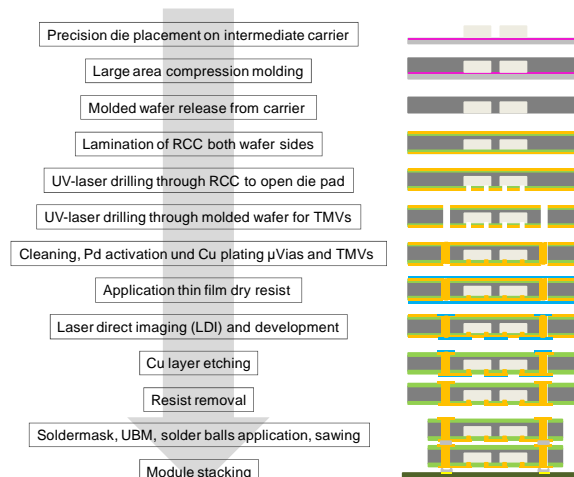


Figure 4. Process flow: PoP assembly based on wafer level embedded package with PCB based redistribution technology

Next process steps are cleaning, palladium activation and copper plating. By plating both, via filling and die pad connection to the copper layer and the top copper layer to the bottom copper layer are achieved. Conductor line formation is done by laser direct imaging (LDI) in combination with a dry film resist and copper etching. Finally, a solder mask and solderable surface finish as NiAu and solder balls can be applied. After package singulation by sawing the package can be stacked and connected by reflow soldering. The process steps described above are summarized in Figure 4.

Demonstrator Manufacturing

Reconfigured wafer assembly and compression molding was done on 6" wafer size. For compression molding a liquid compound with a maximum filler size of 55 μ m has been selected. Wafer thickness was set to 670 μ m due to sensor thickness of 550 μ m to allow homogeneous overmolding of the components without damaging the stress sensitive MEMS components by the filler particles.

The embedded sensor and ASIC dies need to be prepared with an under bump metallization (UBM) to avoid incompatibilities with the used PCB processing. Typically, NiPd pad reinforcement is applied to the silicon wafer or to the reconfigured mold wafer.

Double sided redistribution has been processed accordingly to the process described above. A filled RCC material and process parameters as for the TMV evaluation have been used. Laser drilled via diameter was set to 150 μ m which gave homogeneous and reproducible via drill and metallization results in the 670 μ m thick mold wafer. **Figure 5** depicts the final acceleration sensor package with pads on the package top side for stacking of the pressure sensor package and TMV for 3D routing to the package bottom to connect ASIC and acceleration sensor as well as the substrate.

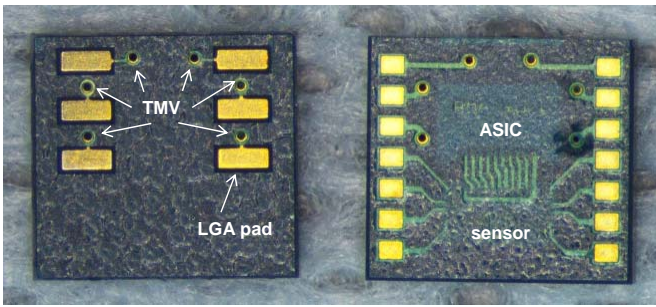


Figure 5. Photograph of an acceleration sensor with ASIC package, package top (left) and bottom (right)

ASIC and sensor show a minimum contact pitch of $110\ \mu\text{m}$ and pad size of $80 \times 80\ \mu\text{m}^2$. Die positions have been measured after molding and automatically used to adapt the μvia drill position to the die pads and the wiring of the conductor lines to compensate the die shift during assembly and molding. Therewith, a good alignment between μvias and die pads could be achieved without shorts or off target positions (s. **Figure 6**).

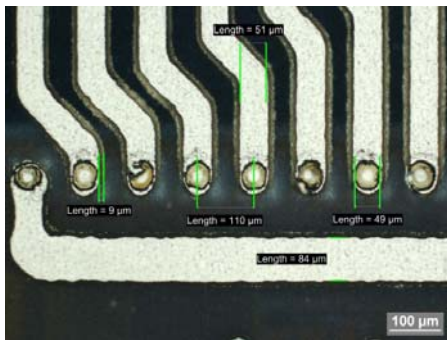


Figure 6. Optical micrograph of an RCC based RDL μvia interconnection to ASIC pads with $110\ \mu\text{m}$ pitch

Figure 7 depicts an X-Ray image of a manufactured demonstrator package showing the interconnection of the top and bottom package metallization by the through mold vias.

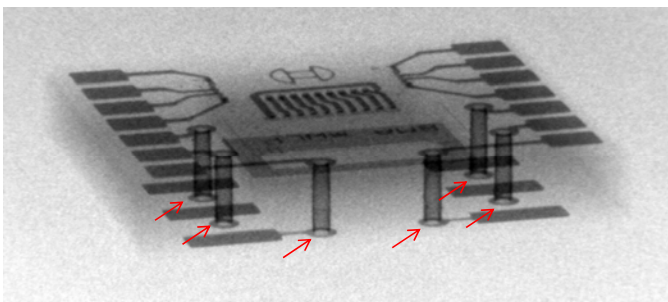


Figure 7. X-Ray image of an acceleration sensor and ASIC package with through mold vias (TMV) marked by red arrows?

Cross sections has been done to investigate μvia interconnects as well as through mold vias. **Figure 8**

shows the interconnection between ASIC and acceleration sensor with the μvia connection the conductor line with the dies. μvia are well aligned and Cu-filled without any air entrancements.

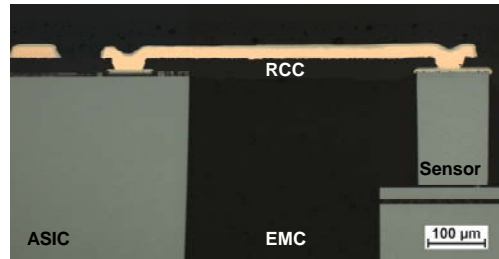


Figure 8. Cross section of a mold embedded acceleration sensor and ASIC package with RCC based redistribution

Through mold vias are homogeneously metallized with Cu with a thickness of around $15\ \mu\text{m}$ depending TMV wall roughness (s. **Figure 9**). Via edges are also well connected to the top and bottom metallization. Solderable surface finish NiAu was also applied in the TMVs resulting in a constant layer thickness of $5\ \mu\text{m}$ as TMVs were not plugged or covered during the electroless metallization process.

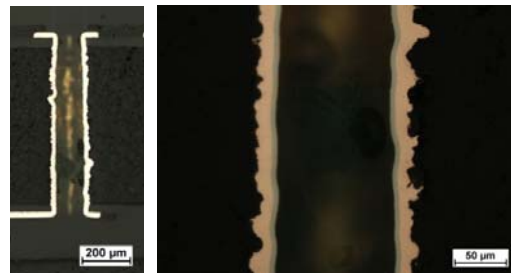


Figure 9. Cross section of a metallized through mold via; left: TMV overview, right: detail via metallization

Pressure and acceleration sensor packages were stacked and assembled on board by soldering. Demonstrator as shown in **Figure 10** allows now the functional testing of the entire sensor stack and therewith the proof of technology.

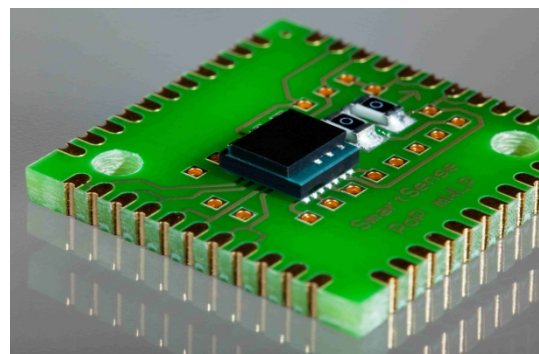


Figure 10. Photograph of a demonstrator stack with acceleration and pressure sensor package

Fan out wafer level acceleration sensor and ASIC package with RCC based redistribution technology and through mold vias as a single package as well as a stacked package have been successfully tested on their functionality. The acceleration sensor performed properly within its specification range. Hence, it can be derived that the above described technology is well suited also for stress sensitive components as MEMS devices and sensors.

PANEL LEVEL PACKAGING

Cost is a major driver of technological developments in microelectronics packaging, so the increase in size found with wafer diameters having evolved from 2" in the 70s to 300 mm today is mimicked by embedding technology. Currently, wafer form factor is mandatory for the manufacturing of mold embedded components, as cost effective thin film RDL technology is only available for circular shapes. But with the PCB-derived redistribution layer application as a feasible fine pitch alternative, a cost effective upscaling of wafer level mold embedding to panel level molding will be a promising path.

Technologically speaking, there is a variety of compression molding compounds for embedded wafer level molding from different suppliers on the market available at the moment. For mold embedding technology materials should have low chemical shrinkage, low cure temperature and match thermo-mechanical properties for low warpage of the molded wafer and low die shift after molding. Flow properties should allow homogeneously filling of large cavities. Basically, state of the art materials can be divided in liquid and granular compounds. From the processing point of view, the liquid materials are dispensed in the middle of the cavity and flow during closing and compression of the tooling to fill the entire cavity. In opposition to the liquid, the granular compound is distributed nearly homogeneously all over the cavity. The compound melts and the droplets have to fuse during closing and compression of the tooling. With a view to large area encapsulation up to 610 x 457 mm² granular compound is the material of choice as here processing is not influenced by cavity size where for liquid compounds larger cavities mean longer flow lengths or application specific dispense pattern with a risk for incompletely or inhomogeneously filling of the cavity.

Sheet or roll lamination under vacuum are alternative process options for large area encapsulation especially as state of the art compression molding machines at the moment only allow encapsulation of areas up to 300 mm in diameter or side length respectively. For encapsulation by lamination, highly filled epoxy resin films are used with material properties comparable to liquid or granular compounds and available film thicknesses range from 50 µm up 1000 µm defining also final product thickness.

Standard PCB lamination presses allow the processing of full format sheets up to 610 x 457 mm² under pressure,

heat and vacuum. Here, drawback is the quite long cycle time due to heating and cooling of the entire press during lamination. However, there is the possibility to process more than one sheet in one cycle, what also leads to a higher yield of the process. Short cycle presses even eliminate the heating and cooling time during lamination cycle as these machines work with preheated plates making the process much faster.

There is also potential for using PCB lamination presses for low cost, large area encapsulation of reconfigured wafer sheets with well-known wafer level molding compounds as described above. At the same time tooling costs for lamination are expected to be much lower as for compression molding. With this technology combination already today the manufacturing of large area mold embedded components is feasible.

CONCLUSIONS

Heterogeneous integration bridges the gap between microelectronics and its derived applications. Two main forces drive progress in this area — emerging device technologies and new application requirements. New technologies and architectures are arising to bring the progress made in microelectronics, microsystem technologies, and bio-electronic or photonic component technologies into application. The future belongs to integration technologies that combine several components into a highly integrated assembly in one package.

One target application was a multi sensor device for indoor navigation purposes integrating magnetic sensors, an acceleration sensor and a pressure sensor – based on sensor development within the MST-SmartSense project. For demonstration purposes the wafer level approach has been applied to pressure sensor / ASIC and to acceleration sensor combinations. For each combination the best suited technology variant was chosen and package stacking could be demonstrated. Successful functional testing of this stacked device also proves that this packaging technology is suited for stress sensitive sensor ICs.

Apart from showing the overall suitability of embedding technology the special focus was put on z-axis routing possibilities, where through mold vias have been evaluated regarding process and reliability.

In this paper a wide variety of technologies has been described that allow the generation of maximum miniaturized microsystems or SiPs, consisting of at least two components – all technologies bear the possibility to integrate multiple heterogeneous components, fulfilling this demand to heterogeneous integration.

REFERENCES

- i For information on HERMES refer to:
<http://www.hermes-ect.net/>
- ii A. Ostmann, D. Manassis, H. Stahr, M. Beesley, J. De Baets, M. Cauwe, "Industrial and technical Aspects of chip embedding", Proceedings in the 2nd ESTC 2008 Greenwich, September 1-5, 2008, pp. 315-320
- iii Yole Development report, "Embedded Wafer-Level-Packages", 2010
- iv D. Manassis, L. Boettcher, A. Ostmann, K.-D. Lang, "Embedded Power Dies for System in Package", International Workshop on Power Supply On Chip October 13-15, Cork, Ireland;
<http://www.powersoc.org/index.php>
- [v] T. Meyer, G. Ofner, S. Bradl, M. Brunnbauer, R. Hagen; Embedded Wafer Level Ball Grid Array (eWLB); Proceedings of EPTC 2008, Singapore.
- [vi] B. Keser, C. Amrine, T. Duong, O. Fay, S. Hayes, G. Leal, W. Lytle, D. Mitchell, R. Wenzel; The Redistributed Chip Package: A Breakthrough for Advanced Packaging, Proceedings of ECTC 2007, Reno/Nevada, USA.
- [vii] Y. Jin, X. Baraton, S. W. Yoon, Y. Lin, P. C. Marimuthu, V. P. Ganesh, T. Meyer, A. Bahr; Next Generation eWLB (embedded Wafer Level BGA) Packaging; Proceedings of EPTC 2010, Singapore.
- [viii] T. Braun, K.-F. Becker, L. Böttcher, J. Bauer, T. Thomas, M. Koch, R. Kahle, A. Ostmann, R. Aschenbrenner, H. Reichl, M. Bründel, J.F. Haag, U. Scholz; Large Area Embedding for Heterogeneous System Integration; Proceedings of ECTC 2010, Las Vegas, USA.