A PACKAGING PHYSICS OF FAILURE BASED TESTING METHODOLOGY FOR SEMICONDUCTOR IC PART RELIABILITY ASSESSMENT

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ABSTRACT

Functional testing is repeatedly performed at several IC part manufacturing stages, from post wafer fabrication to packaging, it is very important to understand its inefficiencies and weaknesses, such as, time zero static electrical functional testing without finding or predicting potential lifetime and operating stress associated quality and reliability issue. Reducing or eliminating these inefficiencies and weaknesses enables an IC part manufacturer to drive down the risk of delivering a bad part or potential a bad part in the lifetime to customers and associated cost of the final product. It is also important to understand the reason and physics of failure before finalize the testing and quality/reliability assurance flow. In this paper, a risk assessment testing methodology built in the fundamentals of packaging physics of failure is discussed in terms of reliability tests and package assembly process flows, associated with package structure, bill of materials (BOM) and failure mode effects analysis (FMEA).

Key words: physics of failure, IC testing, reliability assessment.

INTRODUCTION

There are three major manufacturing stages of the semiconductor IC parts, wafer fabrication, packaging and testing. Every packaging technology of IC parts has its own potential weakness induced by its structure, material, process characteristic and assembly flow, even though, when the parts are well fabricated, the weakness won't certainly result in an obvious defect or failure and can be suppressed during its lifetime. Due to unavoidable statistical flaws in the materials, equipment tooling and process used to fabricate parts, it is impossible to realize 100% yield on any particular IC parts, where yield refers to the ratio of good IC pats to the total number of IC parts. A good IC part is one that satisfies all of its performance specifications under all specified conditions. The probability of a bad semiconductor part increases in proportion to its structures and materials complexity. It also increases by manufacturing sensitivities that occur in semiconductor parts that rely on the control and/or matching of semiconductor components or parameters to achieve their specified functionality. The shipment of bad parts leads to an incurred replacement cost, potential loss of reputation and furthermore possible loss of market share. The other side of this problem is not much better as well. When good parts are represented as bad, it decreases the part yield and, correspondingly, it decreases the earnings of the semiconductor manufacturer.

It has been well known that, testing is repeatedly performed at several IC part manufacturing stages, such as wafer probing after a wafer fabrication, open/short testing after a packaging process and automated testing equipment (ATE) functional testing after a component level assembly. However, it is still very important to understand its inefficiencies and weaknesses, for example, time zero static electrical functional testing without finding or predicting potential lifetime and operating stress associated quality and reliability issue. Reducing or eliminating these inefficiencies enables an IC part manufacturer to drive down the risk of delivering a bad part to customers and associated cost of the final product. It is also important to understand the reason and physics of failure before finalize the testing and quality/reliability assurance flow.

Currently, the most frequent quality assurance method after component assembly is to use sample burn-in pulled from finish goods post final testing (FT), which is the method relatively more detecting a potential die level defect rather than packaging level defect after assembly. This flow was developed based on very old and simple packaging structure, such as low pin count low complexity lead frame types packages, for instance, Small Outline Integrated Circuit (SOIC), Quarter Flat Package (QFP) and so on. At those decades, compared to a fast growing wafer level technology, the package technology was relative matured and less complicated and challenge for most semiconductor parts. It is understandable that semiconductor industry is more focus on the die level quality and reliability post FT and goods shipment. Sample Burn-in was a right choice to add into QA flow after final testing.

However, now days, as packaging technology flying, the packaging structure and process are becoming more and

more complicated and challenge. The low pin count low structure complexity of packaging has been a history, the packaging induced defects or potential defects are making up of more and more share in the FT rejects. Furthermore, the defects which can cause long term reliability issue, in addition to time zero quality issue, is also receiving more and more concern from both component and system level manufactures. Obviously, a risk assessment testing methodology, based on the fundamentals of packaging physics of failure, is also needed to detect these inefficiencies and weakness, especially in terms of reliability tests and package assembly process flows, associated with package structure, bill of materials (BOM) and failure mode effects analysis (FMEA).

METHODOLOGY

There are many issues that affect the perceived quality and reliability of a semiconductor product that is delivered to a customer. For the manufacture supplier, the rules have changed quite radically with time. Failure mechanism driven packaging QA and reliability monitor draws upon the physical concepts and implementation of process or assembly line controls, process stability and effective monitor programs in lieu of qualifying a product based solely on a fixed list of tests. A manufacture must identify those failure mechanisms that may be actuated through a given packaging structure/process change and design and implement reliability tests adequate to assess the impact of those failure mechanisms on component level reliability.

Historical sample burn-in based quality assurance step for major semiconductor manufacturing flow as described below in double solid arrow, while newly added assembly risk assessment testing in single solid arrow below.

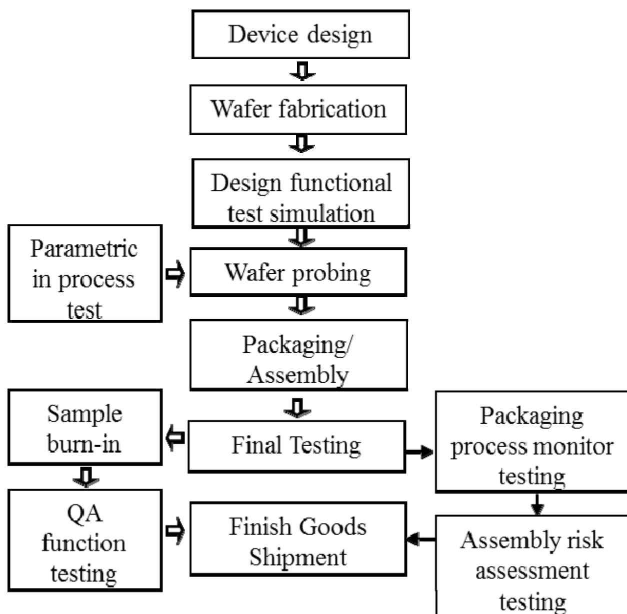

Figure 1. Typical QA Flow for Semiconductor Finish Goods Shipment after Consideration of Packaging Assembly Risk

As described in the above flow, the finish goods shipment not only depends on final testing result and traditional burn-in result, but also depends on the assessment of packaging assembly risk, especially for those complicated or new packaging structures and processes. Well-designed reliability and monitor testing methods are an essential to ensure the parts shipment as well as the component and system level QA and reliability of semiconductor finish goods.

The semiconductor assembly industry uses a technique called acceleration testing to assess packaging reliability. Elevated stresses are used to produce the same failure mechanisms as would be observed under normal use conditions, but in a shorter time period. Acceleration factors are used by device and assembly manufactures to estimate failure rates based on the results of accelerated testing. The needed QA flows and concerns are very obvious to the component and system level manufactures, but problem is that, the adequate selection of risk assessment test targeted to effectively detect the various package structure or process induced defects is difficult. It needs a deep understanding of the risk and failure mechanism associated with the process, machine, procedure, criteria and very often, experience as well. The incorrect selection of a risk assessment testing method could result in a total failure of defect detection and serious customer return, such as apply a burn-in testing to detect a potential moisture sensitive defect, or use a high temperature storage testing to detect a chemical corrosion related defect. It could also cause serious financial loss if apply the incorrect risk testing method during lots disposition, such as apply a component level reflow method to detect the contact related failure of lead frame type package.

Failure mechanism driven reliability monitor draws upon the concepts and implementations of line controls, process stability, Failure Mode Effect Analysis (FMEA) and effective monitoring programs in lieu of qualifying a product based solely on a pre-designed and fixed list of tests. A manufacture must identify those failure mechanisms that may be actuated through a given product or process change, and design and implement reliability tests adequate to assess the impact of those failure mechanisms on component and system level reliability. In order for this to be effective, the manufacture must establish a thorough understanding and linkage to their reliability-monitoring program, though it is very difficult to cover all of potential cases in the whole assembly process.

Different from Statistical Process Control (SPC), reliability monitor program is more for monitoring and improving reliability involving identification and classification of failure mechanisms, development and use of monitors, and investigation of failure kinetics allowing prediction of failure rate at use conditions. Failure kinetics are the characteristics of failure for a given physical failure mechanism, such as the stressing, the acceleration factor, activation energy, median life, standard deviation,

characteristic life, instantaneous failure rate, and furthermore, more important, lifetime prediction of a component mounted into system level product.

In the packaging reliability monitor program and risk assessment, the reliability testing chosen for the detection of failure rate and defect nature at accelerated conditions is critical to generating lifetime data in a much shorter period of time. Release of a reliable product to customers is dependent on this concept. Stressing experienced in the use of environment are accelerated or intently enlarged to a level to accelerate the time to failure of an individual failure mechanism. The key is to not only duplicate the same failure mechanism but also failure rates as occur in use conditions. Development of acceleration model is performed through knowledge of physics of failure, packaging processes, structures, materials and operating conditions. An acceleration factor is calculated as compared to the use conditions. A summary table of some known semiconductor failure mechanisms and accelerating stresses is described below in Table 1.

As discussed earlier in this paper, packaging complex of a device has dramatically grown and its failure phenomena and mechanisms are much more complicated than before, for example, 3D or 2.5D packaging technologies. Not only their materials, processes and structures are very different from the traditional lead frame packages, such as SOIC, TSOP, TO etc, but their impacts on a silicon die are also very different. In terms of reliability and lifetime prediction of a component, their stress field and their process-induced impact on the ultra-low K device are much more complicated and challenging. Obviously, it is necessary to modify the accelerating factors in the table 1, based on the new packaging structures, processes, bills of materials (BOM), to satisfy the need of the new generation of packaging technologies and processes.

The new field of packaging technologies does not have a long history of known failure models when compared to traditional packages as described in table 1. There are no easily obtained acceleration factors for 3D through silicon via (TSV) or 2.5D silicon interposer (TSI) or copper wire or silver wire or copper pillar, micro-bump, coreless substrate, multi-rows lead frame packages, package on package (POP), wafer level packaging and stacked dies etc.

Through previously established models, which were the results of the extensive study of standard integrated circuits reliability science on old wafer node and packaging technologies, it is possible and feasible to consider that the acceleration factors are composed by two physical components, silicon device related and packaging related. For each model in the table 1, for instance, Thermal effects (Arrhenius model), the final acceleration factor can be represented as the result of the dual impacts by both silicon device and packaging by means of activation energy. Different structures, materials, processes of packaging, will apply different stress into silicon device with ultra-low K material, resulting in different activation energy in the thermal effect model and then, different time to failure, failure rate and predicted lifetime.

In the other hand, for a pure packaging related failure rate and lifetime prediction, in which the silicon related activation energy can be fixed, the packaging related activation energy can be determined by experimental testing and reliability testing result, such as a measurement of resistance in a DOE. The activation energy parameter will have a big impact onto the time to failure (TF) and acceleration factor (AF), such as for a failure case on copper pillar bump, well defined and accurate activation energy is very critical to the failure rate and time to failure estimation.

TEST DESIGN AND ASSESSMENT

Traditionally, reliability test focuses on acceleration while electrical test focuses on functionality or failure modes. Achieving an electrical test design with the capability of IC reliability assessment needs to address test design and assessment issues primarily including:

- The quantity of failure modes or faults that can be detected by a set of tests is properly assessed and identified. A reliability prediction result will be impacted by those failure modes or faults that can be detected in a test.
- Those failure modes or faults to be detected in the test are also properly accelerated and duplicated in the test, so to ensure their occurrence as long as defects leading to the failure modes or fault do exist
- The dependency relationship of different failure modes and/or faults are fully understood and properly modeled, so the detection coverage of a test is properly assessed and reliability prediction is correctly conducted.

Below are provided discussions associated with each issue.

Test Coverage

Test coverage is a key quantitative measure of a traditional electrical test in terms of its capability and effectiveness in fault and failure detection. This detection capability and effectiveness apparently is a major factor to reliability prediction as the detection results are to be used to identify failures or faults in the prediction.

Test coverage is defined as the fraction, which can be detected by a test, of all failure modes or faults that can occur for a device under investigation. Therefore, it can well be understood that a hundred percent coverage is usually not possible to achieve in a test. Some primary reasons include, but may not be limited to:

- Insufficient knowledge or lack of understanding about root causes or mechanisms of certain failures or faults to support duplication, acceleration, and/or detection of those failures or faults in a test
- Lack of effective approaches or tools to test or detect

- Non-technical considerations such as cost and time necessary for a test to be implemented

Fault and/or Failure Mode Duplication and Acceleration
For electrical test results to be also used in reliability assessment, failure or faults need to be accelerated or the same failure modes or faults to be duplicated during a limited testing period under certain accelerated environmental stress conditions. It is necessary to ensure at least theoretically that test results exactly reflect what is supposed to happen in actual field operations.

Traditionally, an electrical test is defined associated with failure modes while a reliability test is defined primarily according to environmental conditions and acceleration factors. In an IC test capable of both parametric/functional and reliability assessment, those two definitions need to be established with certain connection and their relationship to be clearly stated.

Figure 2 provides a key aspect of the relationship. The figure indicates an approach of how a set of failure modes to be correlated with accelerated environmental stresses through correspondent failure mechanisms which can be obtained in some routine engineering practices, such as failure mode, mechanism and effect analysis (FMMEA).

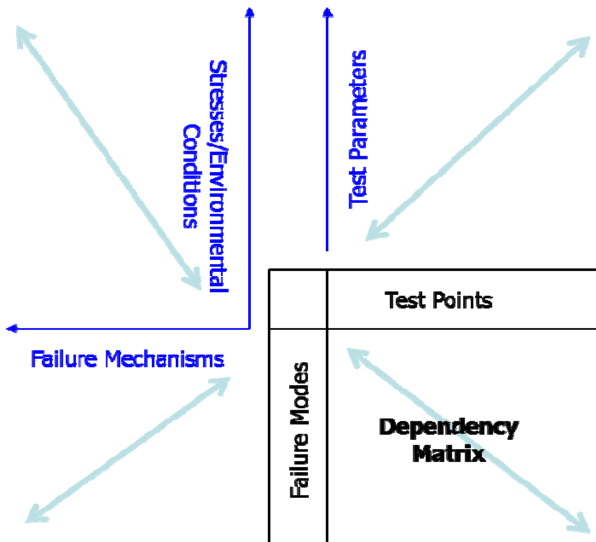

Figure 2. Failure Modes vs Test Points in a Traditional Dependency Matrix

A Duplication Criterion of Known Failure Mechanism
A failure/fault duplication criterion is needed in a test design to define necessary information to duplicate required failure modes in an accelerated stress environment. According to the rules to design an acceleration test and to estimate the correspondent acceleration factor, the criterion can be determined and is stated as:

Failure mechanisms or the physical processes leading to the failure modes or faults to be duplicated or accelerated in a test be fully understood.

As a failure mechanism defines a physical process leading to occurrence of certain failures under clarified conditions, identification and knowledge of mechanisms responsible for faults and/or failures under investigation is essential for the duplication or acceleration of the same faults and/or failures. As a failure mechanism is always associated with certain conditions under which it happens, these conditions also lead to the conditions to accelerate the process to achieve the occurrence of the faults and/or failures during a limited testing period.

With this duplication criterion being applied, traditional electrical tests can then be designed under certain accelerated environmental conditions and results can then be used for reliability assessment purposes.

Basic Failure Mechanisms
The term “basic failure mechanism” is defined in this study to describe those failure mechanisms that are well known in industry and well documented and uniquely defined physical processes with known environmental stresses and factors to accelerate.

Basic failure mechanisms meant in this study primarily include, although may not be limited to:

- Material fatigue and overstress mechanisms, such as
  - ✓ Mechanical vibration induced fatigue
  - ✓ Thermal fatigue
  - ✓ Creep
- Semiconductor and metallization failure mechanisms, such as
  - ✓ Electromigration (EM)
  - ✓ Hot carrier injection (HCI)
  - ✓ Time dependent dielectric breakdown (TDDB)
  - ✓ Negative-bias temperature instability (NBTI)
- Electrochemical, chemical, and oxidation processes, such as
  - ✓ Electrochemical migration
  - ✓ Dendrite growth
  - ✓ Tin whisker
  - ✓ Wet and dry corrosion etc.

It can be understood that this concept of basic failure mechanisms helps standardization of failure mechanism information and correlating acceleration tests that serve the purpose of this study with those of regular industry standards for reliability assessment.

Root and Induced Failure Mode
“Root failure mode” and “induced failure mode” are two additional concepts introduced in this study. Considering facts that failures modes and/or faults may not necessarily be independent from each other and one failure/fault can be a consequence or an effect of another, these concepts are hence used to define such possible dependency relationship among different failures modes or faults. As an example that a part or a component failure can lead to malfunctioning of

an assembly or equipment, the former is considered the cause while the latter the effect.

Therefore, root failure modes and induced failure modes are defined as respectively that:

- Root failure modes are those independent failure modes which are considered sources of failures;
- Induced failure modes are those dependent failure modes which are considered as consequences or effects of other failures or faults.

As a result, it is understood that root failure modes and induced failure modes are associated with the following characteristics that:

- Root failure modes are considered being directly associated with some root causes of failures/faults as well as failure mechanisms at specified local sites;
- Root failure modes can be accelerated and duplicated as long as correspondent failure mechanisms are known and failure conditions are applied, while any original induced failure modes are not considered duplicable unless their correspondent root failure modes are all identified and duplicated.
- A root failure mode, due to its relative simplicity compared to its induced failure mode counterpart, can generally speaking, more likely be defined parametrically, while an induced failure mode, depending upon packaging level in discussion, may be defined in observations or appearance.

Based on the discussion above, it is understood that the concept of root and induced failure modes helps differentiating those failure modes that are more likely associating with basic failure mechanisms (the concept of which are defined in the previous section) and can hence be ensured with clearly defined acceleration in test, from those that cannot. This concept also helps specifying requirements for description and modeling of failure mode dependency, which is to be discussed in the following section.

Failure Mode Dependency and its Modeling

As discussed previously, not all failure modes or faults are independent, which means that detection of some induced failure modes can also be used to sense the occurrence of other failures or faults if it is a necessary condition and leads to the occurrence of those induced failure modes. A dependency matrix, also known as a D matrix, provides this detection relationship. As a result, not all failure modes need a specifically designed test to detect. Only those independent ones or failure mode sets do.

A failure mode dependency matrix is a matrix with failure modes vs test points/locations or defined test tools. A dependency matrix can be derived from the logic flow of functions, and in the case of ICs, from the relationship of logic blocks, signals, parameters and functions, which are usually defined in logic designs and schematics.

IMPLEMENTATION ISSUES

Traditionally, electrical tests serve the purpose of functionality check or verification, while reliability tests focuses on acceleration usually with simplified functional tests and/or parametric measurements for failure detection. Both categories of tests develop in two relatively independent systems with different sources of supportive information. To serve the reliability assessment purpose, an electrical test needs to be taken consideration of reliability information, such as that of FMEA, Failure analysis (FA) and root cause analysis. This need poses challenges to implementation in existing industrial practices and systems.

Some key issues that need to be properly addressed to achieve effective implementation are discussed in detail in the following sections.

To Determine the Total Number of Potentially Existing Failures and/or Faults

A primary shortcoming of the existing approach of test coverage assessment is the assumption of a known total number of potential failure modes, which is unfortunately mostly likely unknown and needs to be determined for a given product. It is therefore in this study proposed that the total number of faults and failure modes are assessed and determined from some original sources of failure information, such as FMEA. This approach leads to results that are considered close to the true number and will continuously improve with its assessment accuracy as people's knowledge accumulates and product quality and reliability improves within existing quality systems.

The figure below shows the expected self-correction mechanism of the approach with the assessment process flow to obtain the total number of potential failure modes and faults.

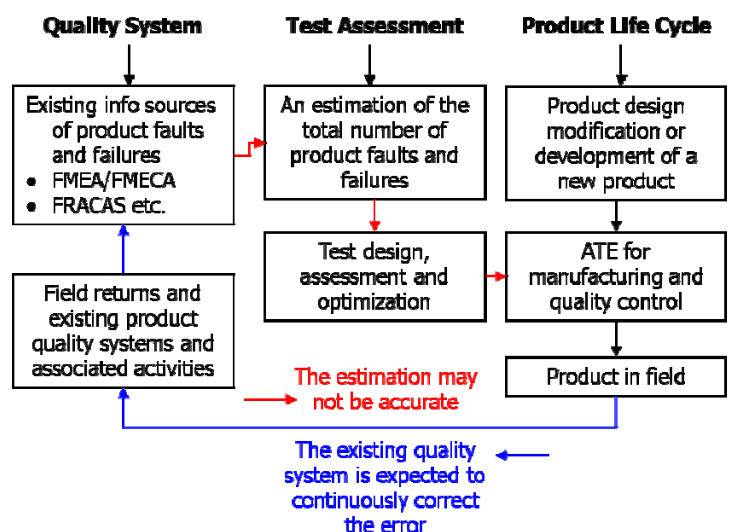

Figure 3. Self-correction Mechanism of the Proposed Approach to Estimate the Total Number of Product Potential Faults and Failures

To Determine Failures and/or Faults Applicable to a Specific Product or a Product Design
The process to determine failures and/or faults that are applicable to a given product or product design from all potentially existing ones is also known as reliability risk identification. The objective is to identify all reliability risks or potential failures or faults that need to be considered for targeting a specific design or a product, which in this study is an IC under investigation.

This process is little possibly conducted manually, and hence practically, requires automated computer process, to be discussed in the following session.

To Achieve Information Standardization and Processing Automation
The fundamental requirement to achieve automated processing is information standardization. Basic information needs to be extracted from its original sources. The term, basic information, here means information that is restrictedly defined, standardized, and computer-recognizable.

Three categories of basic information are identified to serve the objectives of this study, including:

- Knowledge or information in knowledgebase
- Facts or input design information
- Resources or other information in libraries and databases

In which the terms of “knowledge” and “facts” are concepts defined in computer science of artificial intelligence (AI) and expert system.

The libraries and the knowledgebase mentioned above include:

1. Fault and Failure Knowledgebase
This knowledgebase as a primary part of built-in expert system contains information of logic reasoning and inference. It defines the following but not limited to:

- Definition of objects
- Required conditions
- Correspondent faults and/or failures including descriptions of modes, sites, mechanisms and root causes
- Duplication or acceleration conditions
- Test parameters etc.

2. IC Part and Package Libraries
These two libraries define IC and associated configurations and features.

Information in an IC Part Library includes:

- IC part numbers (P/Ns) and codes
- Suppliers
- I/O definitions
- Logic blocks
- Packages etc.

Information in an IC Package Library includes:

- IC package names and codes
- Geometrical features and dimensions
- Materials
- Lead definitions etc.

3. Library of IC Logic Blocks
This library defines internal logic configurations of ICs to be used as a key source of information for IC level test modeling and test coverage assessment. It contains information including:

- IC logic blocks and categories
- Major I/Os
- Test parameters etc.

4. Basic Failure Mechanism and Acceleration Library
A failure mechanism indicates a physical process to undergo with the presence of certain conditions or stresses. This library is hence to carry information of correlation between well acknowledged failure mechanisms and their known acceleration or duplication conditions, including:

- Failure mechanisms
- Phenomenon descriptions
- Factors and conditions to accelerate or duplicate
- Associated industrial test standards for references etc.

5. Test Tool Library
This is a library of defined test tools for debugging, ATE and other test applications, with information including:

- Test names and codes
- Test point definitions
- Test parameters
- Required inputs and conditions
- Test descriptions etc.

To Identify Individual Tests in a Design
In an automated information processing flow, a set of applicable test tools need to be identified and a test coverage assessment result needs to be provided in a test design. Figure 4 provides a basic processing algorithm to achieve an automated process to identify test tools for a given IC part.

With a set of test tools identified and the test coverage also assessed for a test design, detection of failures and faults is then fully defined. Considering with an identified correlation of failure modes and mechanisms and then determined acceleration conditions and information, a test can then serve the purpose of reliability assessment.

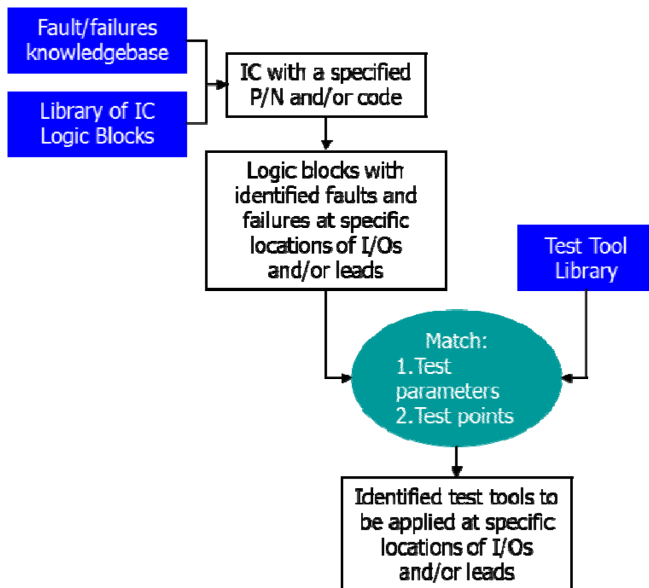

Figure 4. An Automated Process Flow to Identify Applicable Test Tools for a Specified IC

SUMMARY

In this paper, we have first discussed the failure mechanism and physics based risk assessment methodology and lifetime prediction for new semiconductor packaging in the production quality monitor and lot disposition. Traditional models have been examined and the modification of these models has been proposed to meet the production monitor requirement of the new packaging technologies. Due to the complexity of new packaging technologies, materials and assembly processes, the acceleration factor and time to failure are critical to the risk assessment result and decision of parts shipment. The adequate selection of a monitoring testing method and fully understanding of testing result and risk assessment based on the physics of failure are not only a pure technical decision, but also, very often, is a serious business decision in the semiconductor parts production, parts shipment and capital investment.

We have then reviewed in details the test assessment, design and implementation issues for enabling IC tests to also serve the reliability assessment purpose. An integration of traditional IC electrical tests and reliability tests can be achieved with theoretical issues being well addressed while with a computer assisted implementation approach yet to be achieved. This study poses a promising practical approach to provide IC designers and providers with potentially much more enhanced reliability assessment information with extensive electrical tests.

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Table1. Some Known Semiconductor Failure Mechanisms and Accelerating Stresses

Mechanism	Model	Assumptions
Temperature, humidity mechanisms	Peck's $TF = A_0 \times RH^{-N} \times \exp[E_a/kT]$ AF (ratio of TF values, use/stress) $AF = (RH_{Stress}/RH_{use})^{-N} \times \exp[([E_a/k)(1/T_{use} - 1/T_{stress})]$ When calculating variables that stay constant between Stress 1 and Stress 2 they will drop out of the equation.	• AF = acceleration factor • TF = time to failure • A_o = arbitrary scale factor • V = Bias voltage • RH = relative humidity as % • N = an arbitrarily determined constant • E_a = activation energy for the mechanism (0.75 eV is conservative) • k = Boltzmann's constant, 8.162×10^{-5} eV/°K • T = temperature in Kelvin. There are other models for THB mechanisms and they should be checked for the fit to the data.
Thermal effects	Arrhenius $TF = A_0 \times \exp[E_a/kT]$ AF (ratio of TF values, use/stress) $AF = \text{Exp}[(E_a/k](1/T_{use} - 1/T_{stress})]$	• AF = acceleration factor • TF = time to failure • A_o = arbitrary scale factor • E_a = activation energy for the mechanism (0.75 eV is conservative) • k = Boltzmann's constant, 8.162×10^{-5} eV/°K • T = temperature in Kelvin
Thermo-mechanical mechanisms	Coffin-Manson $N_f = C_0 \times (\Delta T)^{-n}$ AF (ratio of N_f values per stress cycle, stress/use) $AF = N_{use}/N_{stress} = (\Delta T_{stress}/\Delta T_{use})^n$	• AF = acceleration factor • N_f = number of cycles to failure • C_o = a materials dependent constant • ΔT = entire temperature cycle-range for the device • n = empirically determined constant • Assumes the stress and use ranges remain in the elastic regime for the materials • The Norris Lanzberg modification to this model takes into account the stress test cycling rate