

Nanocopper Based Paste for Solid Copper Via Fill

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Abstract:

This paper discusses a nano copper based paste for use in via filling. The company manufactures nano copper and disperses the coated nano copper into a paste in combination with micron copper. The resultant paste is injected or fills a via. The via is subsequently sintered by means of photonic sintering, or by heat in a reducing environment. The process will be accomplished in under an hour and results in filled solid copper vias.

Background:

Solid copper vias are instrumental in both electrically conductive and thermally conductive applications as copper is an excellent conductor of both heat and current. In addition, solid vias provide sufficient stability on which to place components. The current method for creating solid copper vias is panel plating the vias in a specifically formulated electrolytic acid copper plating bath¹ (M. Lefebvre et.al., Rohm and Haas, 2011) for 4 to 24 hours. The plating baths may use one of several types of technology such as PPR (Periodic Pulse Reversal²) (Atotech, 2012) rectifiers, or DC rectification with proprietary ionic suppressors in the copper brightener systems. Solid copper vias can be either blind or thru vias, the latter taking extremely long plating cycles to fill completely without trapping solution in the center of the hole due to the “coke bottle” effect of copper plating. These systems require many hours of slow, low current density plating to “fill” the vias and minimize surface copper. Minimizing surface copper is required for consistent etch definition of fine lines and features on the surface copper.

Electrical conductivity requirements may be relaxed for predominantly thermal applications. As such, for thermal applications, via fill materials utilizing epoxy are a good solution. Current conductive fills have bulk resistivity in excess of 20X that of bulk, while standard epoxies are insulators. Several approaches have shown promise for fulfilling this need including DuPont’s CB100, and IBM’s efforts³ (SK Kang et. al, IBM Thomas J. Watson Res. Center, Yorktown Heights, NY , 2001). There are additional approaches and challenges when filling vias on flexible substrates⁴. (Oka et. al, Sumitomo, 2012)

Of great value to the industry is a via fill material that does not require electroplating, reduces cycle time, maintains high conductivity, and is cost effective.

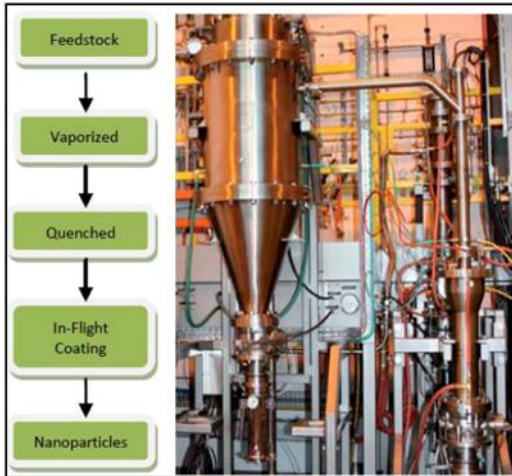
Summary of Findings

The company developed a nano particle generation process whereby very pure nano copper particles are generated, coated, and dispersed. Added to the mixture is micron copper which may also be coated. The coating of the nano particles prevents oxidation, allows air handling of the paste and provides shelf life. Comparable company pastes have a shelf life guaranteed to 4 months although material has been used one year after formulation with no adverse results.

The material is deposited in vias using any one of many standard techniques including injection or squeegee. Once deposited, the paste is dried. It is not yet conductive. In order to form conductive copper, the material must be sintered. Sintering is the process of heating the material sufficiently to remove the coating and to fuse the nano particles and micron together. Because the nano material has a large surface area, the required energy is lower than is required for larger particles. As a result, the material can be laser sintered when used on a non-copper-clad board. When used on a copper clad board, it is preferable to bake the board at relatively low temperature in a reducing environment for less than 1 hour. Our finding of oven sintered copper pastes containing both nano and micron sized copper particles demonstrates resistivities of approximately six times that of bulk copper at a fraction of the processing time of electroplating. The technology allows for the vias to be flash plated then filled with copper paste using industry standard procedures, sintered into pure copper and then over plated to meet the IPC full copper wrap specification.

Nanocopper:

The company has created a fundamentally new approach for making a broad range of nano scale materials. Our scalable plasma nano manufacturing process cost-effectively produces metals, and our process overcomes the inherent instability of metal nano particles through a patented process shown in **Error! Reference source not found.**. In the described process, feedstock is fed into the generator, vaporized, and the nano material begins to nucleate. When an appropriate size is reached the reaction is quenched, the material coated and packaged.

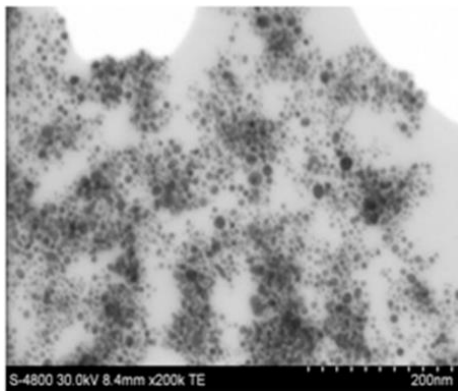


The ability to protectively coat copper nano particles offers several advantages, including: prevention of agglomeration, surface oxidation and other electrostatic challenges; trouble-free dispersion of the nano particles in a variety of media, photonic curing at room temperature, and high conductivity on a range of substrates. The size, scale and composition of the nanoparticles can be tightly controlled and the copper nano particles are dispersed into ink and paste solutions. Typical nano particles are under 100 nm for the paste formulation demonstrated. Shown in

Figure 1 Nano copper formulation is a dispersion containing copper nano particles an ink. For Via filling additional micron content is used to increase the metal content. Inkjet inks carry approximately 15% solids and must be only nano particles. Pastes have a higher solid content closer to

80% which is mixture of nano and micron. The nano material provides the low temperature sintering, and the micron provides metal loading.

Figure 1: Nano manufacturing



The company conductive copper screen pastes and ink are additively printed and cured photonically at room temperature. Copper nano particle inks that are deposited via additive printing methods such as inkjet or screenprint, and are cured via lasers and can be printed on temperature sensitive, flexible substrates such as plastics and metal. Since the features are photonically sintered, not baked at high temperatures, temperature sensitive substrates do not experience damage and degradation as they may have in a conventional electronics process. Shown in

Figure 2 SEM of Sintered Copper is sintered copper material on a plastic substrate that is undamaged.

Figure 1 Nano copper formulation

This means, the material is easily incorporated on the top and the bottom of devices. Additive printing is scale independent, so processing large arrays is not process limited. Focused laser sintering enables creation of fine lines allowing even more compact devices.

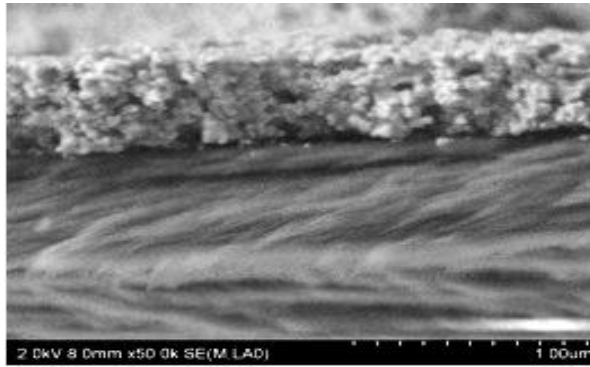


Figure 2 SEM of Sintered Copper

Shown in

Figure 3: Printed and *Sintered* is a transformation from printed to sintered copper

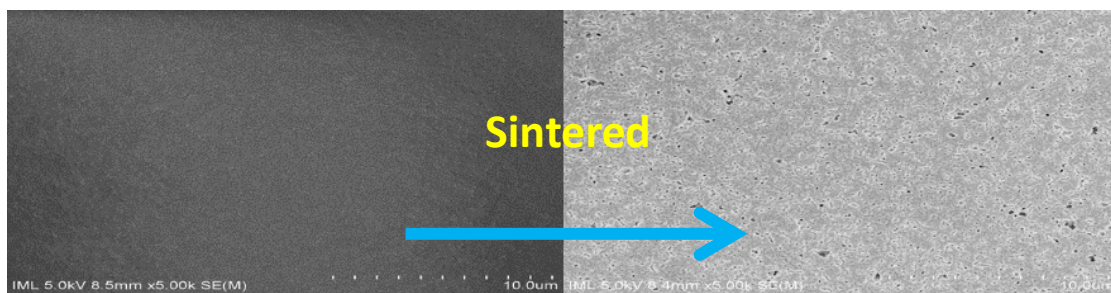


Figure 3: Printed and Sintered

IM paste and inkjet formulations are currently utilized for electronics metallization in products including, but not limited to PCBs and Display backplanes. IM's current manufacturing capacity is 1 ton annually and expanding. IM, in conjunction with manufacturing partners, has demonstrated the viability of our copper paste into OLED Devices⁵. (Orbotech Inc., 2013) and PCB. For the display applications, Intrinsicq has demonstrated integrated devices, on pre-production lines with line widths of less than 5 um, laser sintered, and conductivity equal to that of 50% of bulk copper.

Shown in **Error! Reference source not found.** are the typical operational parameters for non-via fill applications.

Table 1 Material Properties

	CI	CP
Print Method	Ink-Jet	R2R, semi-automatic, manual screen printing
Viscosity	10-12 cps	10,000-30,000 cps
Resistivity	2-3 x bulk	5-7 x bulk
Typical Cured Thickness	0.3-0.5 μm	15-20 μm
Substrates	PI, Glass, PET, Paper	Paper, Glass, PI, FR4
Curing System	Broadband flash, IR lasers	Broadband flash, IR laser, Oven

Via filling experiments:

Initial test sample boards of standard FR4 were supplied. The samples contained blind 0.005” vias of varying depth mechanically drilled into the substrates and subsequently plated with copper as per standard procedure. The samples were both etched into pads and left as copper clad panel plated specimens.

Etched copper pads:

The etched copper pads provided a baseline for Intrinsic CP-004 copper paste as a via fill. The samples were filled by first defining a channel by placing tape on either side of the row of vias. A small amount of the paste was applied to the end of the samples, which were subsequently sealed into a vacuum bag. The paste was spread over and into the vias using a spatula over the top of the sealed bag. This crude simulation of a vacuum environment assists in the blind via being completely filled.

The samples were then sintered using the Intrinsic LAPS-60 laser system containing an 808 nm diode laser. The energy was adjusted to fully sinter the nano copper paste and not burn the laminate material. This resultant filled and sintered via is shown in **Error! Reference source not found.**

It is also interesting to examine the results of the cases for which the vias were not properly filled as it gives insight into the material properties. The laboratory process of via filling is inconsistent as it is crude. Consequently, there were a few samples that were not filled. Interestingly, the adjacent paste simply tented over the via and retained rigidity when sintered. The material was sintered well enough to maintain the tenting, but sufficiently porous to permit potting compound to enter the via and partially fill it. This is shown in Figure 6 the Tented Via.

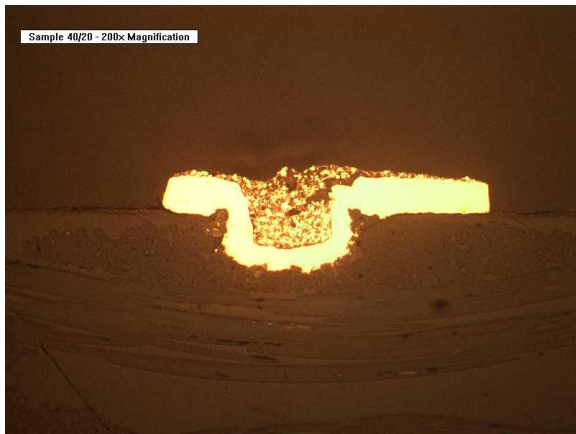


Figure 4 Filled and Sintered Via

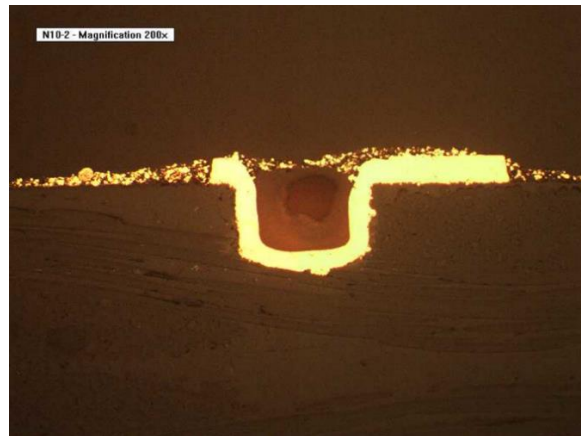


Figure 5: Tented Via

In another experiment shown in Figure 7: Shallow via in what was thought to be a filled via. However, the drilling was very shallow. The paste passed into the shallow via giving it the appearance of filled from the top. Another interesting finding was the result on a thru via. One thru via was found to have been partially filled with ink and it appears to be sintered into the hole. More experiments are necessary to determine usability as a full thru hole via fill.

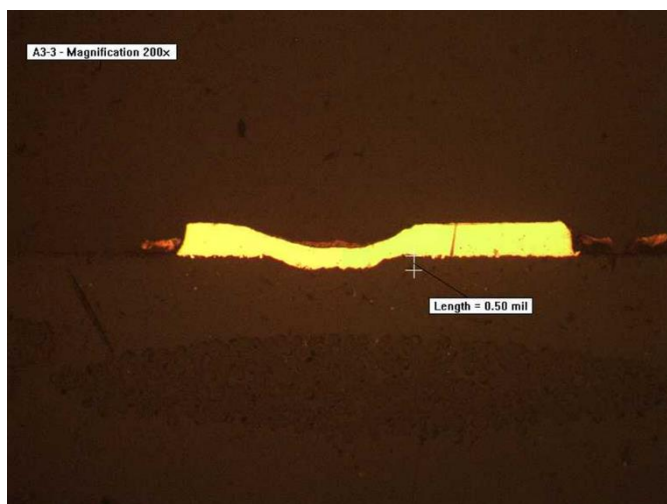


Figure 6: Shallow via

In further testing, six samples were filled using the vacuum bag and a spatula. A dollop of paste was applied to the edge of the samples, then spread into the holes using a spatula after the vacuum was pulled. A channel was formed using tape on either side of the test holes. This resulted in a more uniform deposit (approximately 50 microns) that sintered well on the surface and in the holes. This is shown in Figure 8 Uniform Metal Fill.

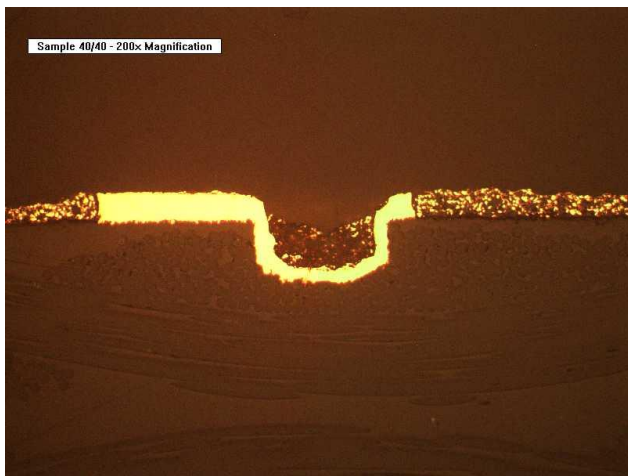


Figure 7 Uniform Metal Fill

Copper Clad: The fully copper clad samples were then prepared as above, using the same methodology employed with non-clad boards including laser sintering. The fill failed to sinter with the laser sintering. This result is not unexpected as the copper cladding conducts the heat away from the via so that insufficient energy is imparted to the nano material surface to allow the coating to volatilize and the particles to fuse. However, the top surface of the nano copper paste sintered while the underlying paste further in via did not sinter. The unsintered material is highly soluble and washed out in the microsectioning process leaving only the sintered material. The experiment with fully copper clad material was repeated with a reducing environment oven to engage the sintering process of the nano

copper paste. The reducing environment was created by bubbling Argon gas thru Formic acid into a ceramic tube furnace

containing the via filled samples. This proved only marginally effective in sintering the material at 250 Degrees C. This temperature for the 1 hour dwell time also destroyed the FR-4 samples.

Reformulating the paste using both nano and micron copper along with other nano additives functionally reduced the sintering temperature to 225 degrees C. This sintered the paste very well and there was no visible damage to the substrate. The picture below is a mechanically drilled blind via, flash copper plated, via filled, and oven sintered in a reducing environment. The via was then planarized and over plated with copper.

While there is some open space due to incomplete filling of the via due to the crude laboratory process, the copper particles have sintered well and take on the same appearance as the plated copper in this micro section photograph, Figure 9: Sintered Via on Clad Material.

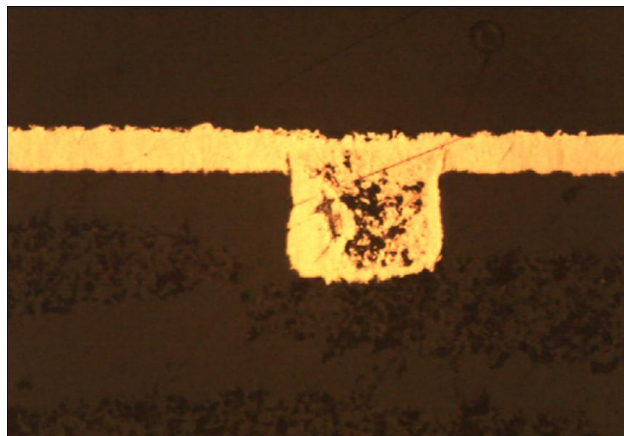


Figure 8: Sintered Via on Clad Material

Conductivity and Adhesion

It is difficult to accurately measure the bulk resistivity of the copper once the via has been sintered, as it is not simple to isolate the conductivity of the sintered paste from the surrounding copper. As such, a standard test pattern was used to calculate bulk resistivity of the oven sintered paste. A series of traces were screen printed onto standard glass slides and oven sintered in the same reducing environment and temperature. Example test patterns are shown in

Figure 10 Glass strips. Resistance measurements were taken with a multi meter and the trace profile was measured using a profilometer. These measurements were used to calculate a resistance to DC current of 6X that of bulk copper which is 1.68×10^{-6} ohms-cm. The pencil hardness of the resulting traces exceeded 4H. (ASTM 3363). Tape test for the materials run on the flat glass surface passed the ASTM 5B standard.

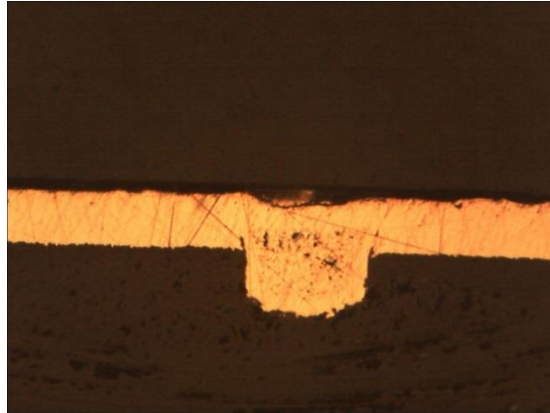


Figure 9: Sintered via post solder float

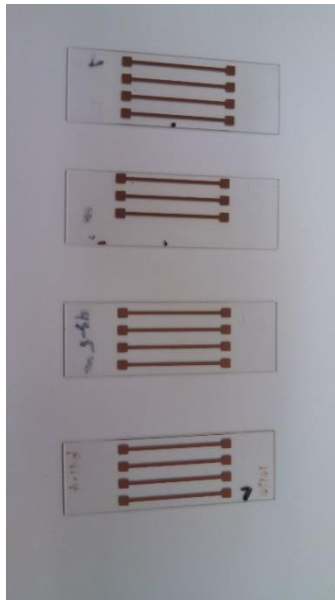


Figure 10 Glass strips

Solder Float testing:

Series of Solder float tests were run to ensure the downstream viability of the filled vias through significant temperature excursions. The test was repeated with 2 paste formulations each carrying different percentages of nano additives to promote lower temperature sintering. The samples used the same process as stated previously, including a planarization step of copper over plating.

Six samples of each paste were used for solder float testing. The samples were floated for 10 seconds at 288 degrees C (550 degrees F). The samples were allowed to cool to ambient temperature before they were refloat. This process was repeated to provide each sample with up to 5 sequential solder floats. After washing, the samples were visually examined for signs of blistering via failure, then micro sectioned. Figure 10: Sintered via post solder float is an example of a via after 3X solder floats. As can be seen in the image the via survived the temperature excursions. The primary intent of the solder float test was to ensure the density of the sintered copper was sufficient to prevent air-bubbles from cracking the board during temperature changes.

Additional samples were prepared, oven sintered, planarized (sanded flat), cleaned then electroplated over. This was performed to mirror the standard PCB via fill process. The samples were subjected to multiple solder float tests to determine survivability of the material encapsulated in the now sealed via. The Figures 12 Sintered Vias show the promising results.

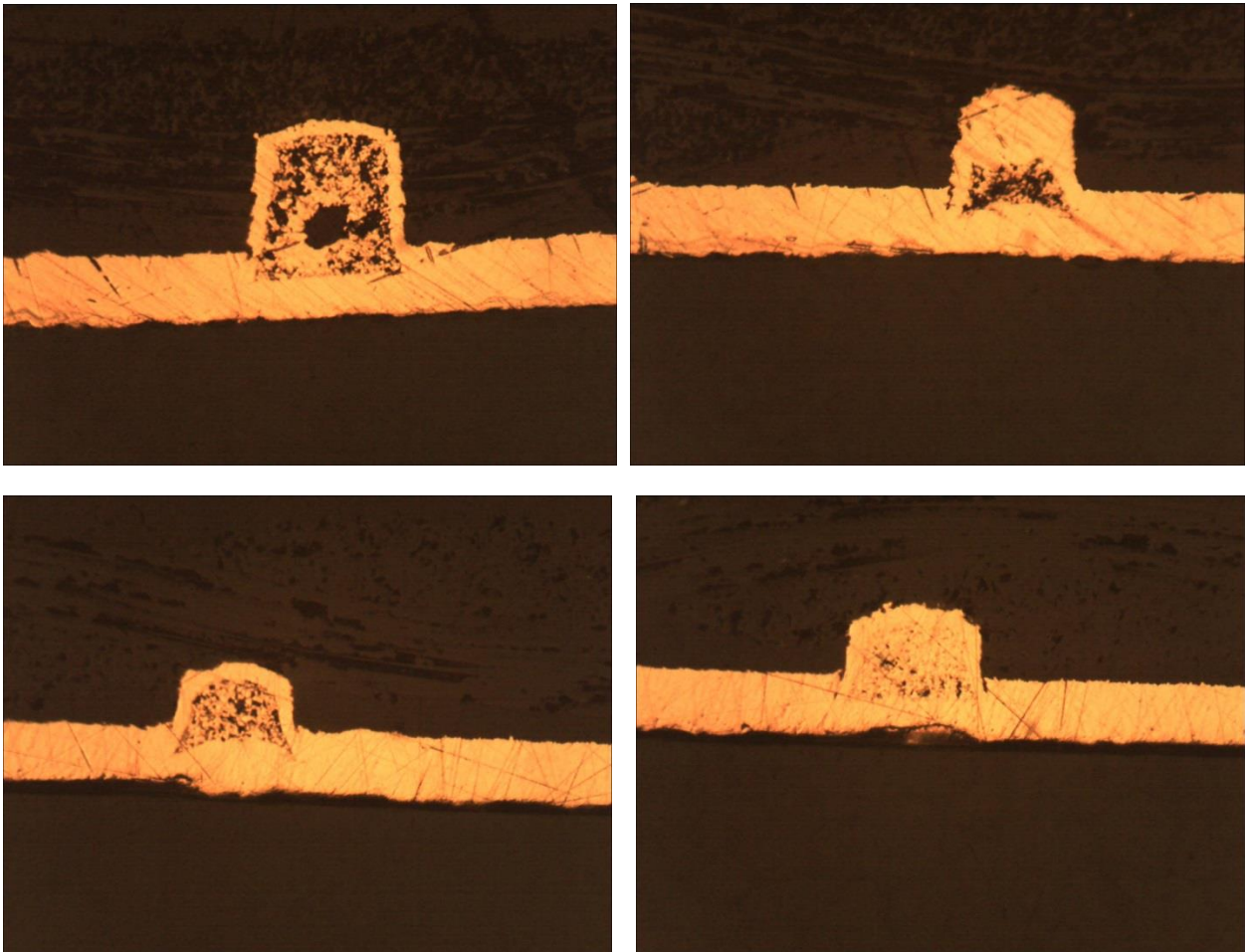


Figure 11: Sintered Vias

Conclusions and Next Steps:

A process flow is shown in Figure 12 Via Fill Process Flow.

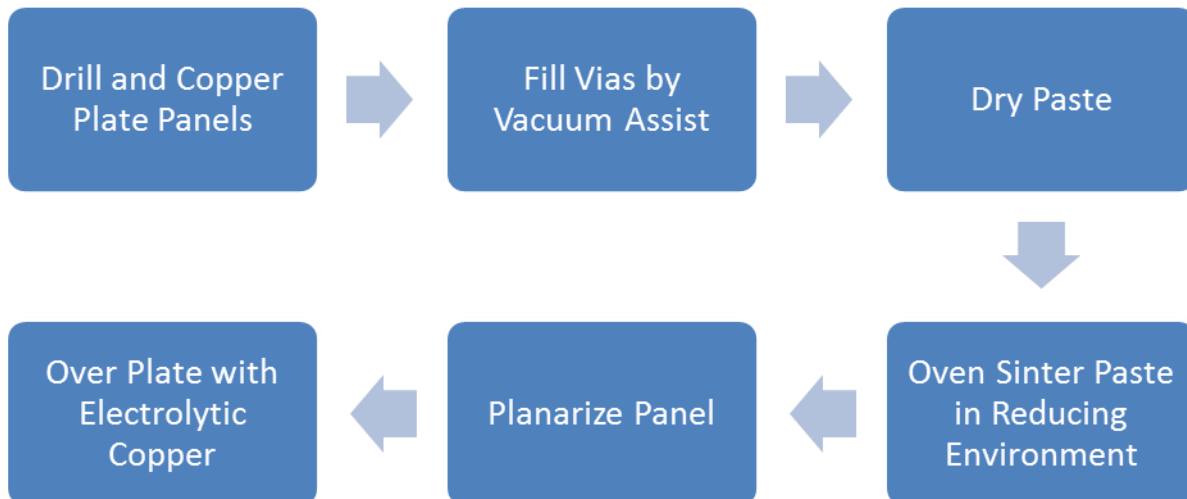


Figure 12 Via Fill Process Flow

A summary of approaches and substrates is shown in Table 2 Summary of Results. The results point to the suitability of nano copper based via fill followed by oven sintering as an excellent approach for solid copper via fill.

Table 2 Summary of Results

Substrate	Conductivity	Sintering Method	Adhesion	Additives
	<i>X Bulk Copper</i>		<i>Tape Test</i>	
Etched FR-4	12X	Laser	Pass	
	100X	BB Flash	Fail	
	>100X	Oven 250C	Fail	
	8X	Oven 225C	Pass	Nano
Clad FR-4		Laser	Fail	
		BB Flash	Fail	
	6x	Oven 250 C	Pass	Substrate Fail
	6x	Oven 225C	Pass	Nano
Glass	8X	Oven 225C	Pass	Nano

The company has developed a nano copper based paste well suited for via filling. With high conductivity, long life, and environmentally cleaner process, the Intrinsic paste offers an excellent option. This paste can be utilized with standard via fill, and may enable quick turn manufacturing. The next steps include investigating us of a more typical Hydrogen/Nitrogen flow in the oven. In addition, Intrinsic plans to work with industry standard via fill techniques.

Acknowledgements

With Thanks to Brett Austin and Nationwide Circuits

References:

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