

BVA: Molded Cu Wire Contact Solution for Very High Density Package-on-Package (PoP) Applications

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Abstract

Stacking heterogeneous semiconductor die (memory and logic) within the same package outline can be considered for less complex applications but combining the memory and processor functions in a single package has compromised test efficiency and overall package assembly yield. Separation and packaging the semiconductor functions into sections, on the other hand, has proved to be more efficient and, even though two interposers are required, more economical. The separated logic and memory sections are configured with the same uniform outline for vertical stacking (package-on-package). The most common configuration places the logic section as the base with second tier memory section soldered to a mating contact pattern.

This paper addresses the primary technological challenges for reducing contact pitch and package-on-package interface technology. Research results will be presented that will illustrate multiple methods for forming smaller and finer pitch contacts on the base package section using existing wire-bond and transfer mold technology. The process developed utilizes copper bond-wire that enables several profile variations and can furnish an array configured contact pitch at or below 200 μ m. The benefits are immediately seen. This interconnect solution is very economical and lends itself to a wide variety of 3D packaging, including multiple-rows and area array, fan-in and fan-out, flat or step mold, bond wires present on bottom or top package, bottom package face-up or face-down die orientations.

Background

Although package-on-package methodology is currently considered a primary assembly solution for the logic/memory applications, greater processor and memory functionality is forcing developers to resort to further reduction in contact pitch for both upper and lower package sections. Interconnecting the upper and lower package sections with smaller sized solder balls or adopting solder filled cavities in the lower section mold cap has temporarily addressed existing requirements but it cannot meet the even smaller projected package size-to-I/O aspect ratios. To achieve greater PCB area utilization for mobile electronic manufacturing companies are finding success in integrating multiple semiconductor die elements within a single package outline. By implementing multiple die packaging companies are experiencing increased product functionality and greater performance potential. Assembly of semiconductor die onto a substrate is essentially the same as those used for lead-frame based packaging; however, substrate based IC packaging for multiple die applications enable the adoption of a wider range of materials and assembly process methods.

Companies that have already implemented multiple die semiconductor packaging are experiencing success in both stacked-die and stacked-package innovations. Although multiple die package technology has reached a level of maturity, there remain a number of issues that must be considered when selecting the specific methodology to be utilized in developing a multiple die package. For example, when vertically stacking two or more semiconductors for wire-bond assembly, the die elements will ideally have a progressively smaller outline typical of that illustrated in **Figure 1**.

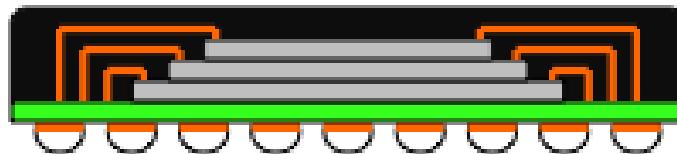


Figure 1. Progressively tiered die-stack and wire-bond package assembly.

This ‘tiered’ configuration allows all die to be sequentially attached on top of one another in a single operation leaving the edge of die elements accessible for the subsequent wire-bond operation. In addition, this tiered die format will generally furnish the lowest overall multiple die package profile.

Package-on-Package Assembly

Vertically mounting one or more packaged die (package-on-package) has evolved as a preferred alternative to die stacking for multiple heterogeneous semiconductor applications. The logic die element is most often packaged as a solo unit before joining the additional package section because logic will often require very specialized electrical test methodology. The second or upper level package section will likely furnish the memory or other related functions. An example shown in **Figure 2** is a heterogeneous (logic and memory) package-on-package assembly.

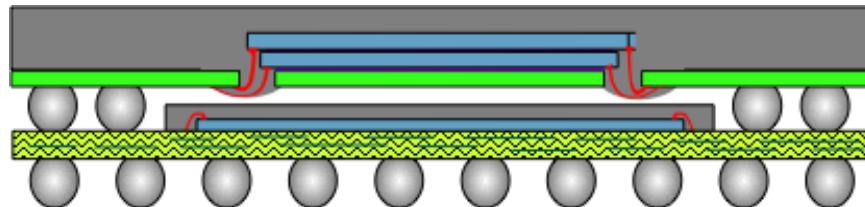


Figure 2. Package sections joined following electrical test.

This technology provides an efficient solution for system level packaging because each section can be fully tested before joining. Logic die may have a significantly larger outline and more I/O than semiconductor(s) in the upper package section. Because of the relative complexity of the newer generations of high performance semiconductors, die outlines are shrinking and I/O counts are expanding. With the reduced outline, the semiconductors perimeter wire-bond spacing is also impacted. In regard to the contact spacing currently established for the package-to-package and package-to-PCB interface, the industry has established several variations. The base or lower package section is allowed to use three contact pitch options; 0.50mm, 0.65mm and 0.80mm. The second tier or upper package section is limited to two pitch variations; 0.50mm and 0.65mm. Greater spacing between contact locations allows the use of larger diameter solder balls to enable the standoff height needed to avoid interference with the mold cap on the lower package section.

Issues and Concerns

Although the PoP assembly methodology has become mainstream, a number of issues continue to trouble users. Many have observed that a great deal of improvement can be made in both performance and power control by closer coupling of the primary signal paths and minimizing circuit interconnect length. The current PoP interconnect technologies have attempted to improve package interface density with smaller sized solder balls, using solder filled laser drilled vias in the mold cap or adopting higher density PCB interposers. Higher density multi-layer circuit routing has had some success but the HDI substrates are not cost effectively achieving required aspect ratios for finer pitch semiconductors. The challenge facing our industry is how we address a number of multiple die package issues:

- How to reduce the overall package outline
- How to accommodate greater I/O semiconductors
- How to enhance package performance
- How to maintain lower power operation
- How to minimize package warp during SMT assembly
- How to maximize existing infrastructure capability

As far as containing physical robustness and controlling package warp at high processing temperatures, the physical attributes (modulus, glass transition temperature and material compositions) for both substrate and mold compounds must be closely matched. And, in consideration for controlling PoP assembly cost, all elements of the package assembly process must utilize the existing manufacturing infrastructure.

Challenge for Innovation

In an attempt to overcome the limiting aspects of the current POP assembly methods an alternative substrate interconnect solution has evolved. The molded bond via array (BVA™) is a wire-bond based package stacking interconnect technology was developed to enable a substantial reduction in interface contact pitch between the lower and upper PoP sections. The main features of the concept are that the wire-bond contact is encased in the mold compound that encapsulates the lower package semiconductor. The bond-wire extends from the top surface of the lower substrate to matching contact locations on the bottom surface of the upper package. Reduced contact pitch will easily accommodate a higher number of interconnects in the PoP perimeter stacking arrangement.

The detail shown in **Figure 3** illustrates the basic BVA interconnect process that enables very-fine pitch contact interface between the upper and lower sections of the package.

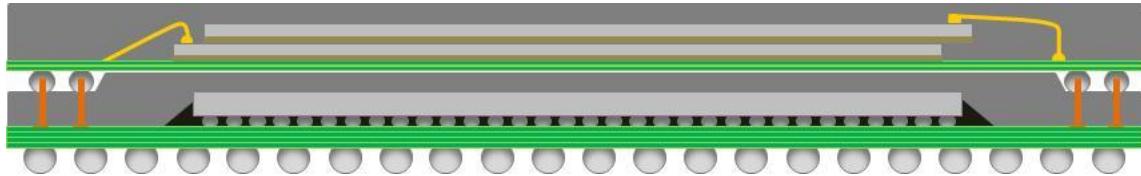


Figure 3: Bond Via Array with very-fine pitch copper wire-bond interconnect

The molded wire process was developed at the Invensas Laboratories in San Jose California offering a very robust, warp resistant stacked package innovation that enables a much greater I/O capability while utilizing the existing, low cost copper wire-bond infrastructure. The current BVA assembly process provides a contact pitch as small as 100 μm , significantly closer pitch than currently possible with solder ball configured package technology. Length of the wire can be extended to a precise elevation to accommodate upper and lower package interface. This interconnect technology lends itself to a wide variety of 3D packaging, including multiple-rows and area array, fan-in and fan-out, flat or step mold, bond wires present on bottom or top package, bottom package face up or down, etc.

BVA Molded Cu Wire Process Development

The ‘Phase 1’ stage of development focused on the integration of processes and materials used to produce 50 μm diameter solid copper wire interconnections having a >8:1 aspect ratio. The lower substrate of the BVA package-on-package test vehicle design was based on the current industry capabilities having 0.5mm pitch solder balls and was used for early evaluation. The substrate outline for both lower and upper sections of the BVA PoP test vehicle was 14mm x 14mm. The Cu wire contacts were bonded onto the top surface of the lower section in a two-row pattern with 0.30mm pitch. This pattern provided a uniform perimeter array with more than 400 contact locations and enables the shortest possible routing path between the over-molded processor on the lower section to the memory contained in the upper section. An identical contact pattern is provided on the bottom surface of the upper (memory) section. Following the assembly of the upper section a pattern of solder paste is printed onto the contact pattern and reflowed to form a uniform spherical shaped solder bump profile. Extending the profile of interconnect protrusions above the molded top surface (**Figure 4**) of the lower package assures consistent joining yields at smaller solder ball diameters of the upper section while achieving reduction of overall PoP profile.

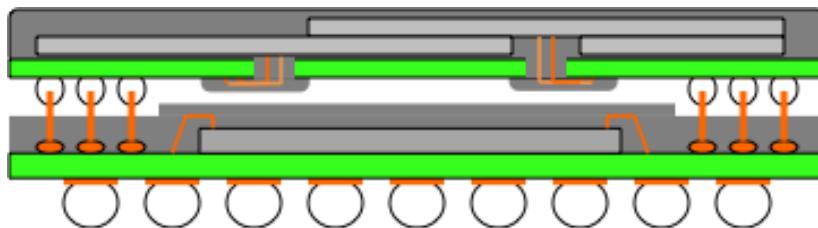


Figure 4. Molded BVA wire contact to solder bump protrusion on upper package section

Copper wire bonding was selected as the method for forming the PoP interconnects as copper provides advantages over gold in cost, stiffness and electrical conductivity. The bonding equipment used was capable of processing copper wire with a maximum diameter of 50 μm and hence 50 μm diameter wire was chosen to maximize structural strength, electrical and thermal performance.

The primary challenges identified and solved during the development of the molded Cu wire technology included:

1.) How to terminate the wire tip at a prescribed height and X-Y position repeatedly with acceptable tolerances- Various approaches to bonding and forming the copper wire on the bottom package substrate were evaluated. Because a free-ended wire would offer finer pitch in both directions, this method was evaluated for positioning and bonding copper wires.

Wire formation with Electronic Flame-Off (EFO) balls was studied, as was wire formation without EFO balls. The copper bond-wire contact array shown in **Figure 5** were formed without applying the flame-off process.

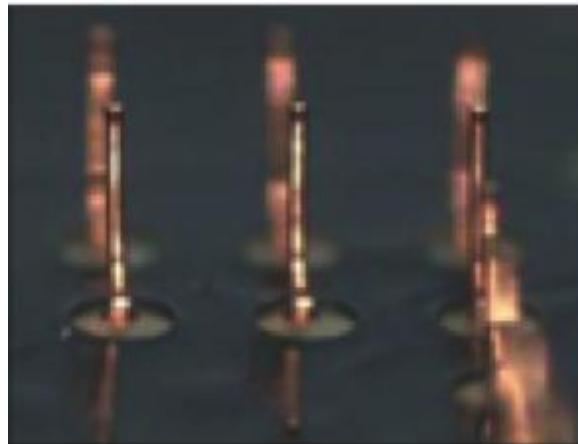
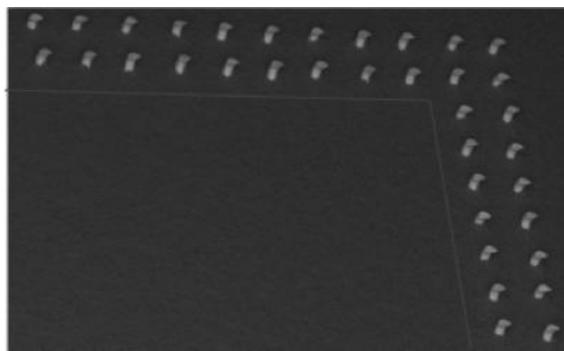


Figure 5: Free ended BVA wire interconnects formed in early experiments at 0.5mm pitch.

2.) How to expose a solder-compatible wire tip above the mold cap- A number of methods were explored to address the second challenge, which is exposing the end of the wire through the molding compound for soldering to the upper PoP package. These included:

- Fully molding the wires and then exposing the loops, balls or wire tips by means of surface grinding, laser ablation, sand blasting or wet blasting the entire top surface of the molded package.
- Coating the wire tip with a water soluble protective coating before molding and then rinsing the coating off to expose the wire.
- Laser ablation to form a semi-spherical cavity around every wire ball or tip.
- Package face grinding to expose the balls or wires and applying metalized pads using metal loaded paste, paint or by seed metal deposition, patterning and plating.

The ultimate solution employed a film assisted molding process, a mature technology commonly found in many packaging assembly operations. The process adapts a mold chase design with mold cavities only slightly deeper than the formed Cu wires. When the mold is clamped to the substrate, the Cu wires are pushed through the mold film. The mold cavity is filled with the molding compound, the molding compound is cured and when the mold is opened the mold film is pulled away from the package exposing the wire tips. The photograph shown in **Figure 6** shows the exposed wire tips. They are completely free of any mold compound residue and maintain an average exposure height of 65 μ m.



**Figure 6. High magnification photo of Cu wire pin tips
After molding and mold film release.**

Mold film thickness actually determines the resulting wire tip exposure. Additional process development was needed to optimize the wire tip exposure, however, no special molding parameters were needed to provide a repeatable wire tip exposure. The Cu wire profile above the mold surface was controlled to an average value of 110 μ m with a standard deviation of 9 μ m.

3.) How to connect the top package solder balls to the exposed tip with good yield and reliability- Several methods for connecting the Cu interconnects to top package solder balls were evaluated. For the soldering experiments a water soluble flux designed for solder ball attach to substrate solder ball pads prepared with a commercial organic solder process compatible preservative (OSP) surface finish. The flux provided the needed surface activation so that the solder would better wet to OSP coated copper surfaces. Initial evaluations made use of manual solder ball placement and shear testing to compare relative strength and examine failure modes. Additional soldering experiments were performed to evaluate the process capability and reliability performance of reflow soldering of the solder balls on the upper section onto the exposed Cu wire tips on the lower section (**Figure 7**).

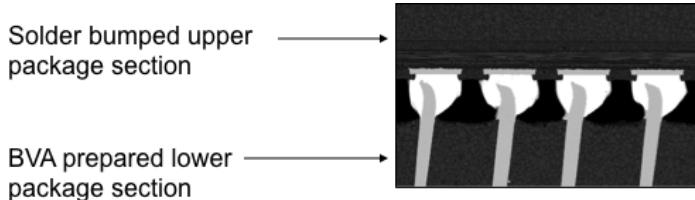


Figure 7. Cross section micrograph of BVA Cu wire tips protruding into the solder-bump contacts on the upper package section.

To inhibit potential Cu-Sn intermetallic growth and minimize the associated embrittlement within the interface, palladium coated copper wire was evaluated. It was anticipated that Pd coated Cu wire would broaden the process window for the bonding of the wire to the substrate and it would also slow the Cu-Sn intermetallic compound formation. The coating would not completely cover a wire tip as the fractured end of the wire would be exposed to the solder but the perimeter of the wire would have the Pd barrier reducing the surface area for solder contact directly to the Cu wire core. The use of Pd coated Cu wire is also commonly used in the industry but the Pd coated wire is not as effective in inhibiting intermetallic compound growth as the ENIG coated wire.

Extensive computer modeling was conducted throughout the package design and development program. Test vehicles are currently being subjected to a broad range of physical testing that is in compliance with their intended use environment. The environmental test plan developed for the molded wire contact PoP program is shown in **Table 1**.

Table 1: BVA test vehicle technology environmental test plan.

Test	Standard	Test Condition	Sample Size
Moisture Sensitivity Level-3	IPC / JEDEC J-STD-020C	125 °C for 24 hours; 30 °C / 60% RH for 192 hours, 3X Pb-free reflow	22
High Temperature Storage	JESD22-A103D Condition B	150 °C, 1000 hours	22
Unbiased Autoclave	JESD22-A102D Condition D	121 °C / 100% RH, 2 atm for 168 hours	22
Drop Test	JESD22-B111	>30 drops, 1500 G, 0.5 ms of half sine pulse	20
Temp. Cycling (Package level)	JESD22-A104B Condition B	-55 °C to 125 °C, 1000 cycles	45
Temp. Cycling (Board level)	JESD22-A104B Condition G	-40 °C to 125 °C, 1000 cycles	45

Drop testing has been conducted on the Phase 1 BVA test vehicles per JEDEC standard JESD22-B111. Test samples were prepared with and without underfill. The standard specifies a physical shock of 1500Gs, 0.5mSec of half sine pulse. In preparation for testing, a portion of the test vehicle units were physically reinforced using an industry standard board level underfill material. Polymer filler material was applied between the top and bottom PoP sections as well as between the bottom package and the test board. The test vehicles with underfill reinforcement passed drop testing but those without underfill reinforcement did not pass minimum drop test criteria.

Phase 2 Test Vehicle Design and Environmental Test Strategy

In order to fully characterize the entire BVA package assembly flow for yield and reliability, a new daisy chain test vehicle was designed (**Figure 8**). The test package outline is 14mm x 14mm with two perimeter rows of Cu wire interconnect at 240µm pitch for a total of 416 top-to-bottom package connections.

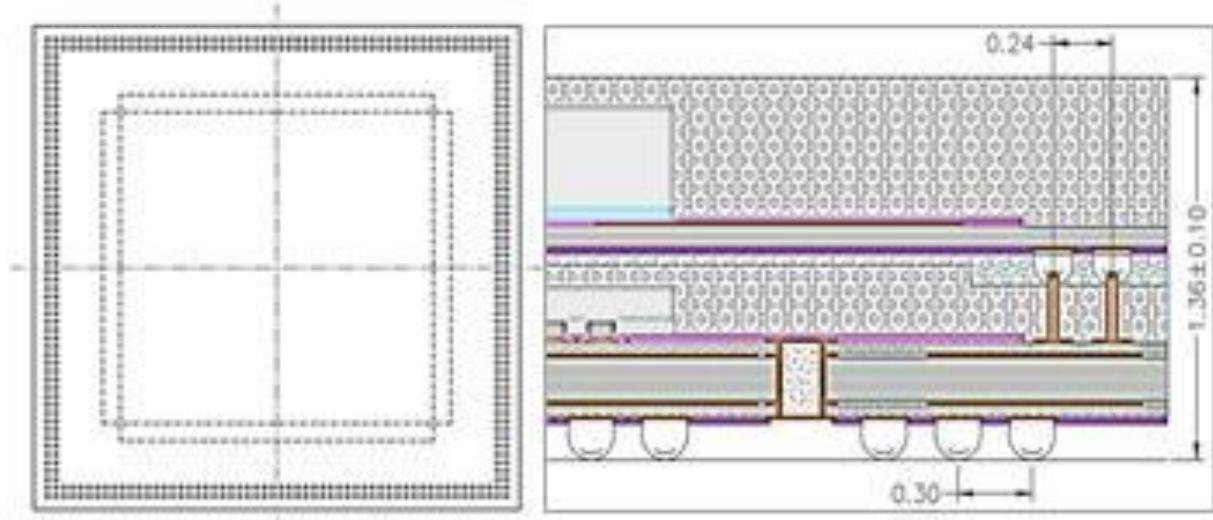


Figure 8. Molded Cu wire PoP bottom substrate and package test vehicle design.

The daisy chain test vehicle substrate was designed and fabricated that featured bond pads at 240 μm pitch, significantly smaller than current PoP interconnect pitch (**Figure 9**).

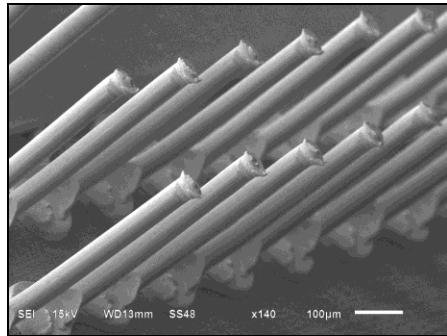


Figure 9. High magnification photo of two rows of 400 μm high Free-ended Cu wires at 240 μm pitch.

Daisy chain connection pattern link only the package sections and substrate platform together. The Phase 2 test vehicles do not include connections to test silicon die elements within the package sections. The next phase of the BVA development program will include the design of an even lower profile PoP configuration and transfer the process to a high-volume supplier. Additionally, plans are underway to design a BVA package with 1000 I/O and investigate alternative applications for the bond-wire contact process.

Summary and Conclusions

Increasing demand for product miniaturization and high-performance computing continue to call for higher density devices and modules. The mobile electronics markets continue to see significant growth. Developers of UltraBook, smart phones and tablet products are now adopting multi-core processors and they need greater memory bandwidth. To meet these market trends, manufacturers are expecting faster process capability and greater memory bandwidth to be packed into less space with reduced power. Developers continue to design products that furnish greater functionality. Their goals often include reducing product size and weight. To achieve the expanded functional capability, however, leads to adapting more complex and higher I/O semiconductors. The ideal package outline for many of these products will range between 10mm square to 14mm square. The semiconductor die outline and I/O requirement is often the primary limiting factor on the ultimate package outline dimensions. The 14mm square BVA package outline with 0.2mm contact pitch between the lower and upper PoP sections can accommodate up to 1440 I/O using the same amount of area currently required for a 288 I/O, 0.5mm pitch FBGA configured PoP. **Table 2** furnishes several contact pitch-to-row combinations that can be selected to achieve specific I/O goals.

Table 2: Contact potential for the 14.0mm square BVA package technology.

Pitch (mm)	No. of I/O rows					
	2	3	4	5	6	
0.50	200	288	-	-	-	
0.40	248	360	-	-	-	
0.30	336	492	640	-	-	
0.25	408	600	784	960	-	
0.20	512	756	992	1220	1440	

The processes and equipment required to assemble and stack the molded Cu wire bond via array packages are quite common to typical package assembly lines found throughout the industry. All process steps for wire-bond are commonly found in packaging assembly factories but, the open-end BVA package assembly process is unique. Primary differences are the copper wire formation technique and film assisted molding process. Design specific tooling may be required for handling and test to avoid contact with the exposed wire tips and pick-and-place assembly systems will need very precise (+/- 20µm) positional accuracy. A modified flux or paste for stacking will be required if soldering to bare Cu lands but suitable formulations are available from major flux suppliers.

In regard to board level (SMT) assembly, most EMS suppliers using commonly found SMT package placement equipment will have the necessary capability. The top and bottom package can be pre-joined before board mounting or sequentially stacked in place and simultaneously reflow soldered onto the product board.

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