LOW TEMPERATURE SOLDER INTERCONNECT RELIABILITY AND POTENTIAL APPLICATION IN ENTERPRISE COMPUTER AND AUTOMOTIVE ELECTRONICS

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ABSTRACT

Journal Nature of June 14, 2018 report that the Antarctic ice sheet lost nearly three trillion metric tons of ice from 1992 to 2017[1]. In just the last five years, the frozen continent has shed ice almost three times faster on average than it did over the previous 20 years. Combined all the water raised the global sea level by average 7.6mm, the researcher said about two-fifths of that rise occurred in the last five years. iNEMI Board Assembly Technical Roadmap[2] of 2017 predict that the low temperature soldering (LTS) usage will increase to 20 plus percent by 2027. The drivers for this LTS technology trend are three folds, the energy and CO_2 emission reduction, overcome material limitation in electronic component and PCB, and low soldering process to match with electronic miniaturization.

This article is a series of study on new low melting temperature solder interconnect application and reliability on various product categories, enterprise computers such as server and storage, AIO (all-in-one desk top), POS (Point of Sale), tablet, and automotive electronics. First, the raw LTS SnBiAg material properties range from power particle size, Halogen content, flux characterization, viscosity, wetting, SIR, Electrochemical migration etc. are assessed. Then five product emulators are selected as test vehicle to represent the broad scope of various electronics products. Due to the nature of brittleness of Bi contain in the LTS as shown in earlier publications3,4 the material drop cycle to failure reliability of LTS is substantially below current SAC305 which widely used in various electronics. Mechanical strengthening mechanism such as corner bonding material is attached along the BGA to observe the susceptibility of mechanical shock in later two product emulators, tablet and automotive electronics. Since all BGA incoming with solder composition are in SAC305 nowadays there is a backward compatibility issue with new LTS. Inhomogeneous microstructure as well as potential solder defect was observed in SEM micrograph. Experiment of adding various LTS paste volume so as different Bi percentage in mixed alloy join are studied to see crack propagation and failure interface due to Bi diffusion and intermetallic compound formation when product emulator subject to accelerated stress test. While observe the crack propagation in microstructure, potential strengthening mechanism such as solid solution, precipitation hardening and phase size refinement can be determined in the of SAC and LTS mixed and Bi percentage variation alloy.

Finally BFT (board functional test) will be conducted in between accelerated thermal and mechanical cycling test to offline but real-time monitoring the reliability of solder joint of passive, PTH, BGA of active IC and CPU. The benefit of using product emulators with BFT is an advantage in the transition of LTS from SAC.

Key words: LTS, Low Temperature Solder, SnBiAg, Technology Roadmap, Climate Change, Extreme Weather, Product Emulator, SAC305, Mixed alloy, Inhomogeneous microstructure, mixed alloy, Crack Propagation, Intermetallic Compound, Strengthening Mechanism

INTRODUCTION

Excessive CO2 emission in the atmosphere has been proved to cause extreme weather events such as heavy rain, violent storm, droughts and heat waves. Recent study from Max Plank Institute for Biogeochemistry, Germany5 indicates the extreme events not only cause suffers in the whole ecosystems but also create more CO2 emission to form a vicious circle of climate change due to self-reinforcing effect as shown in Figure 1. Reducing CO2 emission is the most urgent endeavor in environmental protection to ensure the sustainability of tour planet ecosystems. Satellite data over last 25 years show the change of ice sheet thickness. It is clear to the environmental science Antarctica is affecting the climate change and it's responding to the change of ocean temperature. The overwhelming scientific consensus indicates that the planet is warming at a rate accelerated by the greenhouse gases from human activity.

Reducing CO2 emission through alternative material application such as lower soldering temperature can be a potential major contribution from electronic industry. On the cost saving aspect, the reduced electricity saving from SAC to LTS soldering is very substantial in monetary term of $8500 per oven per year. iNEMI Board Assembly Technical Roadmap2 of 2017 predict that the low temperature soldering (LTS) usage will increase to 20 plus percent by 2027 or

earlier. Reducing CO2 emission through alternative material application so as to reduce soldering temperature can be a potential major contribution from electronic industry.

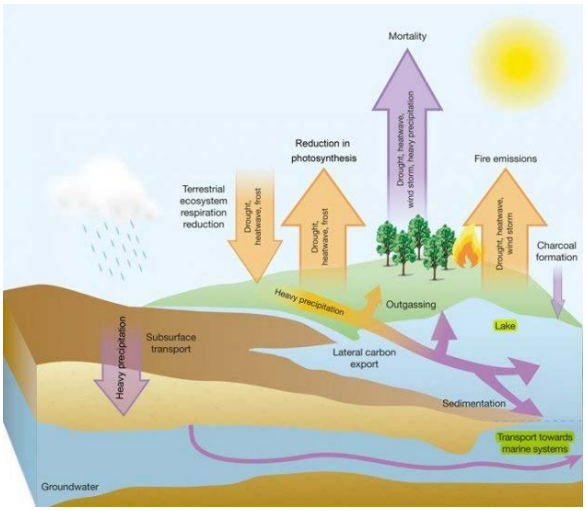


Figure 1. CO2 emission due to extreme weather forming a vicious circle of climate change due to self-reinforcing effect5.

This article is part 1 of a series of study on new low temperature solder interconnect application and reliability on various products, enterprise computers such as server and storage, AIO (all-in-one desk top), POS (point of sale), tablet, and automotive electronics. First, the raw low temperature solder, SnBiAg material properties will be studied. Then product emulators are selected as test boards to represent the broad categories of electronics products in our portfolio of interest.. Due to the nature of brittleness of Bi contain in the LTS, the impact related failure rate of LTS is substantially below current SAC305 which is widely used in nowadays. Potential mechanical strengthening mechanism, such as corner or edge bonding material is attached along the BGA to observe the susceptibility of mechanical shock in experiment for two product emulators, tablet and automotive electronics who subject to frequent high shock loading environment.

THE CHALLENGE AND THE APPROACH

Since some of the BGA still in current SAC lead-free solder there is going to be a forward compatibility issue with LTS paste application to the component-SAC-LTS-circuit board interconnects system. The mixture of SAC and SnBiAg create a complicated mixed alloy system in which Bismuth tend to form a layer in bulk form in the mixture as well as along the IMC and solder interface as shown in Figure 2.

With brittle nature of the Bismuth phase in the β–Sn matrix of mixed alloy of SAC-SnBiAg, it is logic that the higher the Bi diffuse into SAC ball and the more the Bi-phase homogeneously distributed the reliable is the interconnect system. Although there are complications from other factor such as component corrected warpage with circuit board, CTE mismatch and pre-existing micro crack at fracture interface can contribute as bias to the reliability test performance.

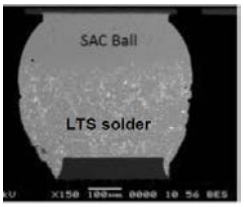
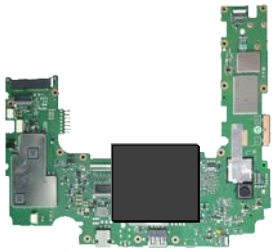


Figure 2. Mixed alloy of SnBiAg solder SAC ball under BGA interconnect

Solder paste printability and solder wetting so as interconnect reliability are two other major factors beyond other paste level qualifications for a smooth transition from SAC to LTS. It is also a concern about the creep aging behaviors of LTS as the melting point of SnBiAg 1.0 is in the 130~140 range is using as interconnect system for package such as CPU operated at high temperature or computer system running in harsh ambient environment after pre-existing stress from product shipping and material handling. It is a good question for system designer to judge whether a system design intent match with service warranty mission time. It is possible that BGA corner or edges bonding are option to protect against the impact load from transportation stress and material handling before user service cycle.

Three out of five product emulators as shown in Figure 3 are selected as test vehicles to represent the broad scope of various electronics products in our portfolio of interest. Due to the nature of brittleness of Bi contain in the LTS, the product e drop cycle to failure performance is much lower than current SAC305. Mechanical strengthening mechanism for BGA will be exploited to observe the susceptibility of mechanical shock in portable tablet and automotive electronics. Accelerated Thermal cycling test, ATC per IPC-9701 specification7 will be conducted to see the fatigue behavior of LTS in aging perspective of field service. In between ATC testing, the BFT, board functional test will be conducted on the whole active circuit daisy chain segment then TDR will be used to diagnosis segment of the circuit non-destructively to narrow down the specific location of failure before destructive test by x-section and SEM**.**



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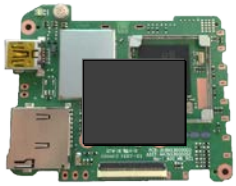
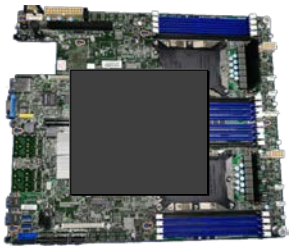


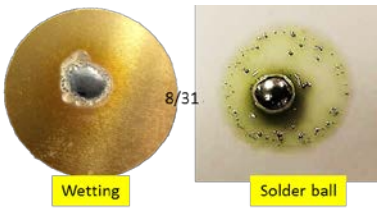


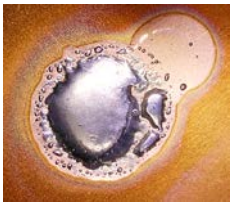
(b) (c)

Figure 3. Three of the five product emulators are shown here to represent potable, automotive electronics, and enterprise computer in LTS study

RESULT AND DISCUSSION

For LTS paste raw material level test, more than 17 items including viscosity, wetting, printing, solder ball test, SIR, EM etc. per TM-650 and JIS-Z standards were conducted on two suppliers, A and B. Inconsistent paste quality was found in one of the supplier during the course of LTS paste development. As shown in Figure 4, the massive solder ball residue and de-wetting were observed which failed IPC TM-650 2.4.43 and JIS-Z-3284.8 at one point and passed at another time. Similar inconsistent LTS solder quality was also found in one of the test board as shown in Figure 5. Although the exact composition of the paste is supplier's know-how, the most logical root cause for these LTS soldering quality problems are due to flux chemistry such as evaporation temperature so as the solder paste is not able to wet forward and pull back properly in paste wetting test and in actual test board reflow. Even though printability of the paste is fine but as the paste stay on the stencil longer through rolling back and forth, the flux chemistry will dictate how molten solder is behaved.





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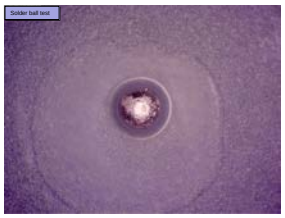


(c) (d)

Figure 4. Inconsistent paste quality found during the course of LTS paste development with massive solder ball residue and de-wetting problems at one point (a) and solder ball test and expansion test passed at another time (b)

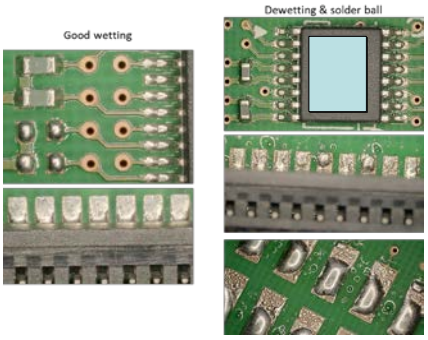


Figure 5. Inconsistent soldering quality, massive solder ball residue and de-wetting on one of the product test board

The paste printability is good with paste registration and paste volume and height maintain in acceptable level in both case of BGA and DDR4 as shown in Figure 6. This result matches with good result from viscosity and slump paste test. Voiding percentage after reflow in BGA and QFN are normal with percentage below 10% as shown in Figure 7, even though the profiling in modern mass production reflow oven is a challenge to match with an impractical profile from a low oven zone from a supplier lab for one case. For the fact that the LTS are still in early stage of development in the industry, a mature LTS solder performance so as to practically apply to low impact user environment and low power system design are a path to be exploited.

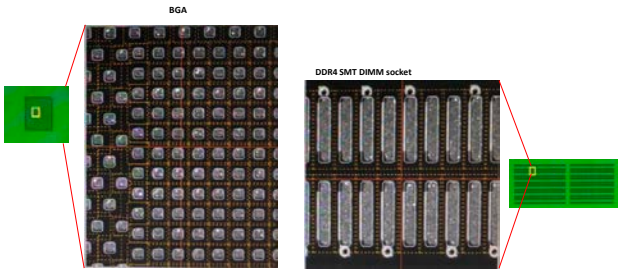


Figure 6. Paste printing inspection SPI of BGA and DDR4

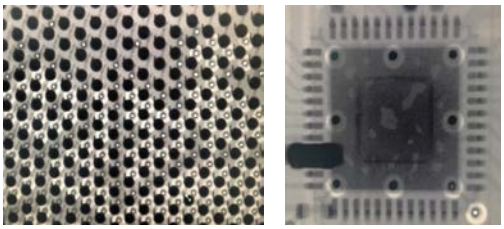


Figure 7. Normal voiding in BGA and QFN

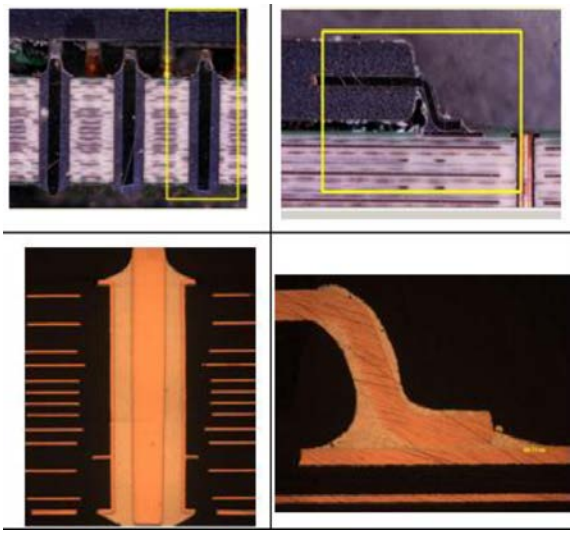
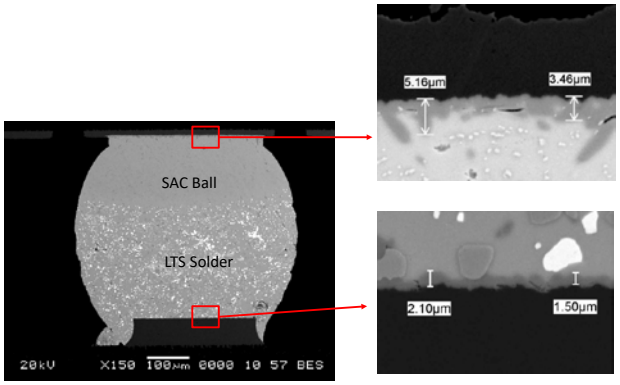


Figure 8. LTS solder configuration of pin PTH connector and surface mount gull wing IC

Optical and x-section views of an IC with gull wing and pin connector with PTH were inspected as shown in Figure 9. The solder hole fill reach 100% which is not a surprise for an test board with OSP finish and thickness in 2.2mm. Solder wetted height in toe and heel of gull wing and solder hole fill in PTH are normal which illustrate proper wetting can be achieved when the right flux chemistry and reflow profile are optimized as shown in Figure 8.

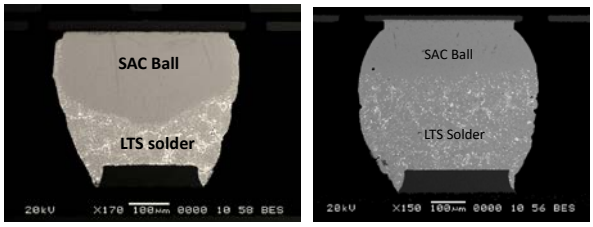
Because some of the BGA are in current SAC lead-free solder there is a forward compatibility issue with LTS paste application to the component-SAC-LTS-circuit board interconnects system. The mixture of SAC and SnBiAg create a mixed and complicated alloy system in which Bismuth tend to form a layer in bulk form in the mixture as well as along the IMC and solder interface as shown in Figure 9. Overall the IMC is in general acceptable range of thickness 1.5~3 µm with composition Cu_6Sn_5 as in pure SAC to SAC interconnect system, even though the bulk of Bismuth are much extensive.

With brittle nature of the Bismuth phase in the β–Sn matrix of mixed alloy of SAC-SnBiAg, it is logic to think that the higher the Bi diffuse into SAC ball and the more the Bi-phase homogeneously distributed in the mixed regions the reliable is the interconnect system as shown in Figure 10 (b). One reasonable rationale is that the peak reflow using in Paste B is reflowed at slight higher temperature so as to promote more molecule diffusion. The research teams are looking forward to see the cycle to failure performance difference of mixed alloy system from LTS of supplier A vs. supplier B through drop test and accelerated thermal cycling tests, although there are possible complications from other factor such as component corrected warpage with circuit board, CTE mismatch and pre-existing micro crack at fracture interface can contribute as bias to the reliability test performance. This type of loose correlation of interconnect reliability to Bi mixing in mixed alloy system probably will logically apply to the early study[7] that use Bismuth diffusion height in middle, left and right of the crescent shape of mixed SAC-LTS for Bi mixing percentage. Although quantitative relationship between paste volume ratio to SAC and Bi mixing percentage can be a good thing in term of establishing rationale of crack propagation though bulk form of Bi-phase in the matrix of β–Sn.



(a) (b) (c)

Figure 9. Microstructure of mixed alloy of SAC and LTS (a) with IMC thicker at package side (b) and Bismuth accumulate at LTS and IMC interface (c)



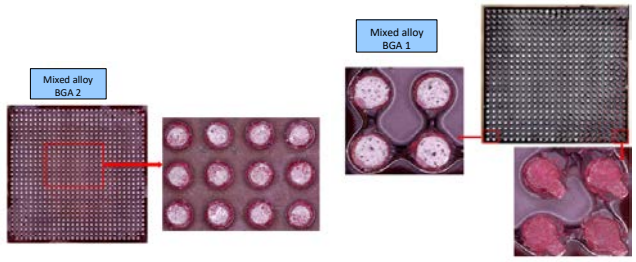
(a) (b)

Figure 10. Mixed alloy of SAC and SnBiAg solder ball in BGA using LTS from supplier A (a) and supplier B (b).

Accelerated Thermal cycling (ATC) with test condition -40~100^{0}C and 85^{0}C/85%RH aging test are conducted on one of the product emulator to see creep behavior of LTS-LTS and mixed alloy SAC-LTS system. Since the acceleration factor of SAC and mixed alloy of SAC-LTS are not known in the industry, the cycle to failure data of current test will be benchmarked to the ATC. As of July 2018, there are 3 mixed

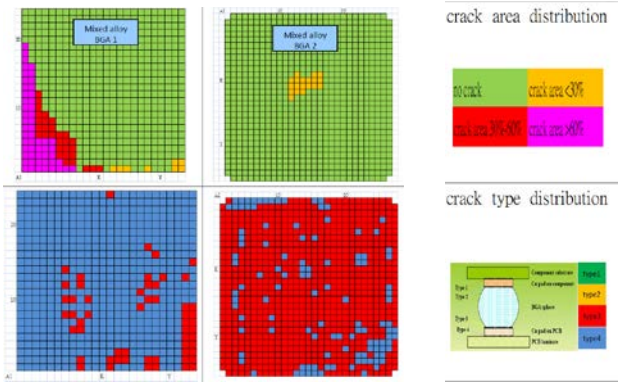
alloy BGA failed functional test out of 7 as compare to 0 failure of pure LTS-LTS BGA after 750 cycles of ATC.

Finally Dye penetration test was performed on the 3 failed mixed alloy BGAs and two of the representative site are shown in Figure 11. With crack location, area and type defined in Figure 12 (a), the conventional wisdom of crack at corner due to crack concentration is applied to two of the cases with the third BGA crack concentrated at center of the package of crack type 3. Ongoing study by dynamic Shadow Moiré will be performed to see the time/temperature base of package warpage and see the concave to convex of package shape inversion if any. In general overall concentrated area of crack can be compensated with extra paste volume but if the distribution is varied from board to board then paste volume and reflow profile are not likely can solve all the type than the component design and material selection in the perspective to enhance the mechanical robustness.



(a) (b)

Figure 11. Dye penetration of two mixed alloy BGA2 with preferential crack type 3 (a) and BGA 1 with crack type 3 and 4 (b)



(a) (b)

Figure 12. Solder crack area and crack type statistic (a) and Crack area crack type distribution definition (b)

CONCLUSION

Reduction in energy consumption so as to prevent excessive CO_2 emission into the atmosphere is a great benefit to the environment of planet earth. Reducing CO2 emission through alternative material application so as to reduce soldering temperature can be a potential major contribution from electronic industry. iNEMI Board Assembly Technical Roadmap[2] of 2017 predict that the low temperature soldering (LTS) usage will increase to 20 plus percent by 2027.

In part 1 of the study on new low temperature solder interconnects application and reliability on various products, the lesson learns from the study are:

- LTS paste raw material is early in the development process. Inconsistent paste qualities in paste level test and product emulator were observed in one case. Flux chemistry stability is likely the logical root cause to cause solder ball residue and de-wetting.
- Paste printability is good with registration and volume/height maintain in acceptable C_{pk} level. Solder wetting in PTH and leaded device are normal and voiding percentage after reflow for major packages are below 10%.
- Expecting backward compatibility issue in material sourcing. Mixed alloy in component-SAC-LTS-circuit board system to be interconnecting reliability concern with observed Bismuth tend to form a bulk phase in both the lower LTS region as well as along the IMC and solder interface. Overall the IMC show similar thickness and composition as in pure LTS-LTS system.
- With brittle nature of the Bismuth phase in the matrix of β–Sn, it is logic fact that the higher the Bi diffuse into SAC ball and the more the Bi-phase homogeneously distributed in the mixed regions the reliable is the interconnect system. The research teams are looking forward to see the cycle to failure performance difference of mixed alloy system from LTS of supplier A vs. supplier B through drop test and ATC. Expect further study on Bi-phase behavior in crack propagation to prove these effects.
- Initial ATC result as of July 2018 indicates that the mixed SAC-LTS alloys are at least 250 cycles less reliable than LTS-LTS interconnect system. Dye penetration test show the crack interfaces are at package to soldering as well as at solder to IMC interfaces.

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