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LOW-COST AND HIGH PERFORMANCE SILICON INTERPOSERS AND PACKAGES (LSIP) – A NEW GEORGIA TECH PRC INDUSTRY CONSORTIUM

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ABSTRACT

The Low-Cost Silicon Interposer (LSIP) industry consortium at Georgia Tech is proposed to address limitations of current organic packages as well as wafer-based silicon interposers that are being produced in wafer fabs. Organic substrates are seen as approaching limits in wiring, I/Os, warpage and acceptable cost. Silicon Interposers, on the other hand, suffer from high cost and low electrical performance. This paper addresses both these limitations.

Key words: Wafer silicon interposer, panel silicon interposer, polysilicon, through-package-via, polymer liner, insertion loss, low cost silicon interposer, dry film dielectric

INTRODUCTION

The Low-Cost Silicon Interposer (LSIP) industry consortium at Georgia Tech is proposed for eight reasons: 1) to replace organic substrates as they approach limits in wiring, I/Os, warpage and acceptable cost; 2) to act as 2.5D interposer in the short-term and BGA package in the longer-term for interconnecting ICs and 3D ICs with ultra-low k dielectrics; 3) to act as 3D Interposer, an alternative to 3D ICs for achieving high bandwidth at low power between logic on one side and memory or other devices on the other side, enabled by ultra-short through-package-via interconnections (TPVs) at same or similar pitch as TSVs in the 3D ICs; 4) to further miniaturize package and sub-systems as a result of double-side mounting of both actives and passives enabled by TPVs; 5) to extend wafer-level fan-out technologies in I/Os, miniaturization and cost; 6) to provide a technology platform for MEMS and Sensors with ultimate reliability, performance and cost compared to plastic packages that absorb moisture and transfer stress to the die as a result of large CTE mismatch between die of 3ppm/C and plastic package of 17ppm/C; 7) to achieve ultra-low warpage in ultra-thin packages as a result of high modulus of silicon and balanced double-side structure; and 8) to go beyond interposers and develop them into surface-mountable BGA packages.

A two-year program is focused, however, on 2.5D interposer with 2-5µm lithographic ground rules. This presentation will review goals and describe accomplishments in low-cost silicon raw material, low-cost through via and metallization, and low cost RDL.

OBJECTIVES

The objectives of low-cost silicon interposer technology being pioneered by Georgia Tech's industry consortium are to: 1) provide I/Os at 20-50µm pitch that cannot be achieved in area array with organic packages, 2) lower the cost of wafer-based silicon interposers by 2-10X and improve electrical performance over traditional lossy silicon.

General Requirements of Interposers

Table 1 lists general requirements of interposers:

Requirements
• Low Cost of Raw Substrate Material (Silicon) o Thin and large wafers or panels at low cost o None or minimal CMP cost
• Low Cost Processability of Through Vias and RDLs o Low cost through via hole formation and metallization o Low cost and high I/O multilayer redistribution layers
• Improved Properties o High electrical resistivity o Low electrical loss o High dimensional stability o High thermal conductivity o Appropriate CTE between IC, interposer or Package and board

Table 1. Primary Interposer Requirements

The critical characteristics include: availability in thin and large area raw substrates; processability to achieve high via and wiring density; good electrical and thermal properties such as CTE, thermal conductivity, electrical resistivity; and finally, relative overall cost that includes not only raw material cost but also the final processed cost with vias and wiring at 2-5µm technology, per square area. This comparison leads to low-cost wafer and large-area panel processing using non-traditional silicon as being the single most important factor in the final decision of interposer and package technology for low cost.

Table 2 compares and contrasts Georgia Tech's low-cost silicon interposer approach with the current wafer-based silicon interposers being pursued by industry.

Technology	Traditional Si Interposer		GT Low Cost Silicon Wafer and Panel Interposer
	BEOL	WLP	
Raw Material	CMOS Si		Polycrystal Si
Size	200-300mm wafer		300mm wafer to 700mm panel
Thickness	50-200µm with polish		100-200µm w/o polish
TPV Hole	DRIE		Laser
TPV Liner	Thin Oxide		Thick Polymer
TPV Metal	Barrier/Seed/Cu		Eless Seed/Cu
RDL	Single-side Process		Double-side Process
	Cu-Oxide	Cu-PI	Dry Film Build-up
Dielectric	Thin SiO_2	Spin on Polymer	Dry Film Polymer
Via	Dual Dam	Photo Via	Laser
Cost • Wafer • Panel	 High N/A	 Medium N/A	 2X 10X

Table 2. Comparison of Current Silicon Wafer-based Interposers with Georgia Tech's Polysilicon Interposer

Interposers, by definition, connect IC I/Os on the top side at 20-50µm pitch to organic packages on the bottom side at 100-150µm pitch for flip-chip assembly to organic BGA-like package substrates, which connect, at 300-500µm pitch for direct SMT-attach to board. Since the number of interposers coming from 200 or 300mm silicon wafers is low, particularly if the interposers are 50-60mm in size, serious cost concerns remain as the biggest barriers to silicon interposers. The second major concern with existing silicon interposer is the signal loss in vias and transmission lines as well as cross-talk between adjacent through vias at fine-pitch.

Georgia Tech's Packaging Research Center (PRC) proposes, therefore, a two-phase strategy as shown in Figures 1 and 2: 1) apply first, at largest wafer size by performing leading-edge R&D to demonstrate low loss silicon interposer with low cost TPV and RDL, and then commercialize using the improved and low cost materials and processes as described in Table 2, resulting in about 2X cost improvement; followed by 2) large panel processing of polycrystalline silicon for a broad set of applications.

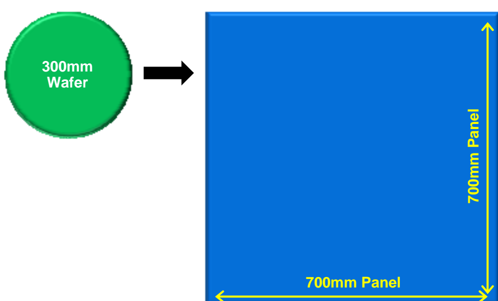

Figure 1. Georgia Tech PRC Strategy for Low-Cost Silicon Interposer – 2X Lower Cost at Wafer-Level First, Followed by Large Panel for potential 10X Cost Reduction

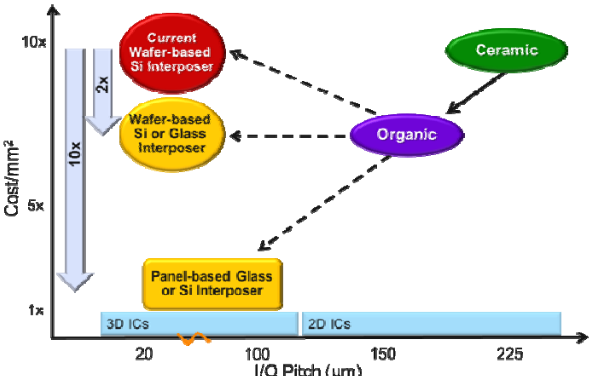

Figure 2. Georgia Tech PRC Low-Cost Strategy with Both Wafer and Panel Interposers

Such a strategy is expected to solve two major limitations of traditional silicon interposers: cost and electrical performance, thus leading to improved electrical, mechanical and thermal performances, as described below.

TECHNICAL BARRIERS

The barriers to the use of silicon are mainly its high signal loss and its high cost per mm^2, when processed with BEOL tools. Additional challenges include fine-pitch RDL with micron-size lines at high yield and low cost with minimum signal loss, and micro-bump assembly at fine-pitch.

The overall strategy is to address these barriers to enable commercialization of polysilicon interposers and packages. The Georgia Tech approach to low-cost silicon interposer is shown in Figure 3. It starts with polycrystalline silicon, which is a factor of 10 lower in cost than single-crystal silicon. The TPV hole is formed by laser at a cost lower than DRIE. The TPV liner is made of thick polymer by a low-cost process technology in contrast to thin SiO_2 liner. The RDLs are fabricated, not with liquid dielectrics, but with dry films. The initial program will focus on applying as many of the above low-cost technologies as possible at large wafer-level, which will then be applied at panel-level.

Figure 3. Georgia Tech's Non-traditional Silicon Interposer Materials and Process Flow

SILICON INTERPOSER TECHNOLOGIES

Low-Cost Silicon

The cost reduction focus starts with the use of upgraded metallurgical grade (UMG) polycrystalline silicon wafers, which are manufactured by directional solidification and wire-cut into 100-200µm finished thickness. This eliminates expensive steps including purification and ingot growth, as well as back-grind and CMP polish, required for CMOS-grade single crystal silicon wafers. The raw silicon wafer or panel used in this interposer research has been developed for photovoltaic applications, and can have varying electrical resistivity, ranging from 0.1 to 0.6 ohm-cm, based on the level of impurities in the silicon material. The polycrystalline silicon, not only is a factor of about 10X lower in cost than CMOS silicon, but is also scalable to large and thin 700mm x 700mm panels. Figure 4 shows a top view of a typical 156mm x 156mm wire-cut polycrystalline silicon panel at 200µm thickness. Novel thin silicon handling methods, for double-side processing, have been explored and demonstrated in this research [1].

Figure 4. Polycrystalline Silicon Panel at 200µm Thickness and 156mm x 156mm Panel Size

Via Formation

Bosch process is commonly used for via formation in traditional silicon interposers [2, 3]. However, such a process is not scalable to large-panel substrates. Therefore, low-cost and high throughput laser ablation process was developed in our study to form fine-pitch vias in polycrystalline silicon substrate. Three different laser technologies (UV, Excimer and Pico-second laser) were explored for via formation in polycrystalline silicon substrates. Table 3 compares the differences among the three laser technologies. The 355nm UV laser was able to achieve as small as 25µm vias at high throughput. While the excimer laser processing with a wavelength of 248nm was faster and resulted in small vias, this technology suffers from higher production cost. The 355nm pico-second lasers can further reduce the heat generated during the laser ablation process. Vias with 10-50µm diameter were formed by pico-second lasers. However, this method is currently limited by slow processing speed and serial via formation. Therefore the low cost 355nm UV laser was used as front-up method in our study. Figure 5 shows the top and bottom view of small and fine-pitch vias formed in polycrystalline silicon by UV laser.

Laser	Via Dimensions Achieved	Cost
UV (355nm)	25-150µm	Low
Eximer (248nm)	10-20µm	High
Pico-Second Laser (355nm)	10-50µm	High

Table 3. Via Formation in Polycrystalline Silicon Substrate by Three Laser Tools

Via diameter Via pitch	Top side (diameter)	Back side (diameter)
25um diameter 75um pitch	(25 um)	(14 um)
50um diameter 75um pitch	(50 um)	(37 um)

Figure 5. Via Formation in Polycrystalline Silicon by Low-Cost UV laser

Liner Formation

A SiO_2 layer with expensive barrier to prevent Cu diffusion is widely used as insulation liner in traditional silicon interposers [3]. Such a step always involves high-cost CVD or PVD processes. In addition, the traditional silicon interposer suffers from high signal loss due to the thin SiO_2 layer (0.1-0.2µm) that is typically and sparingly employed. The GT silicon interposer focuses on ultra-low-loss and thick polymer formation in fine-pitch vias to address the high signal loss in TPVs, while eliminating the diffusion barrier. Simulation results showed that the thick polymer helps to reduce the loss and resulting silicon interposer shows superior electrical performance than traditional silicon interposers, as shown in Figure 6. The technical approach for the liner formation is called double laser method, involving polymer filling of larger TPV, followed by laser ablation to form an “inner” via resulting in a via side wall liner of controlled thickness, as shown in Figure 7. The polymer was fully filled by a low-cost double-side vacuum lamination process. Such a lamination process can also form polymer layers on top and bottom sides of the silicon panel simultaneously, for insulation purposes. A low-cost UV laser process was then used to drill a smaller via in polymer. Alternative approaches to fabricate the liner, by conformal electrophoretic deposition and spray coating are also under study and will be presented in the future.

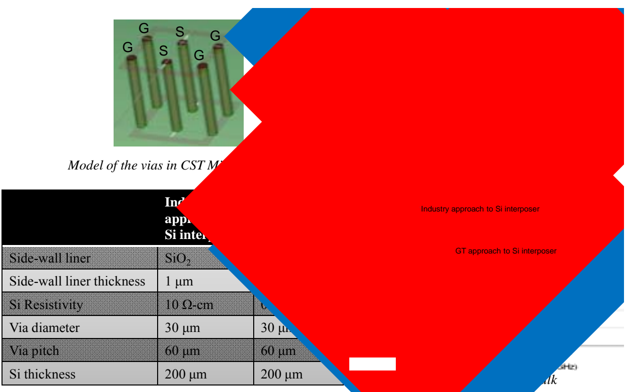

Figure 6. The GT Silicon Interposer Approach Shows Superior Electrical Performance Than Traditional Silicon Interposer

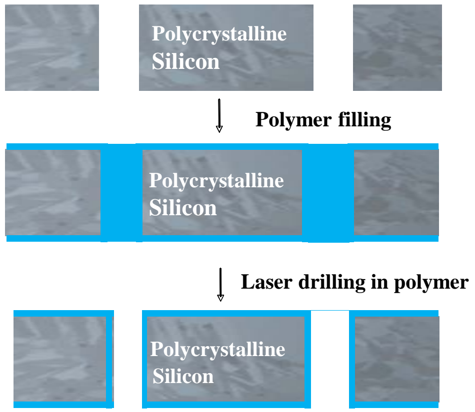

Figure 7. Double Laser Method to Form Thick Polymer Liner

Metalization

Comparing to the high-cost vapor deposition method for adhesion layer and electroplated Cu seed in traditional silicon interposers, the GT process involves a low-cost, all-wet metallization process, including electroless and electrolytic plating. The metallization process consisted of three steps: 1) Cu seed layer formation, 2) Cu electroplating and 3) pad formation. The polycrystalline silicon samples were first cleaned using plasma to remove any impurities on the surface. A fast, low-cost electroless plating process was then used to fabricate a 1µm thick Cu seed layer for further electroplating. The dry film was laminated on both surfaces of the sample followed by a lithography process. A void-free semi-additive Cu electroplating was then performed in the plating tank to fill the through vias. A final step, including Cu thinning, photoresist removal as well as seed layer etching, was conducted to form the Cu pad for connection. Figure 8 shows the cross-section of Cu-filled TPV with polymer liner.

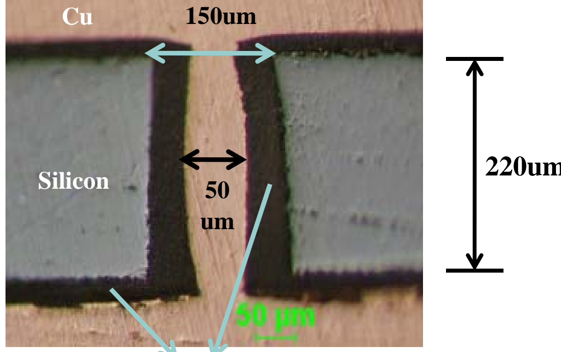

Figure 8. Cross-section of Polymer-lined and Metallized TPV

Ultra-fine line RDL wiring is essential for escape routing on silicon interposers, in as few layers as possible. Most of the published research on fine-pitch RDL fabrication is either expensive [4], or limited by relatively coarse wiring ground rules [5]. The GT target, in this project, is to realize fine-pitch RDL wiring on thin-panel silicon interposer at a lower cost than with wafer-based processes. In the 2.5D silicon interposer demonstration (Figure 9), 1000 interconnections between logic chips (10mm x 10mm) and memory chips were achieved with two metal layers of RDL. Bump pitch in these examples was 50µm, with 25µm landing pad diameter. Therefore, the wall-to-wall distance was 25µm. With 5µm wiring, three rows of I/Os can be routed in one metal layer (Figure 10).

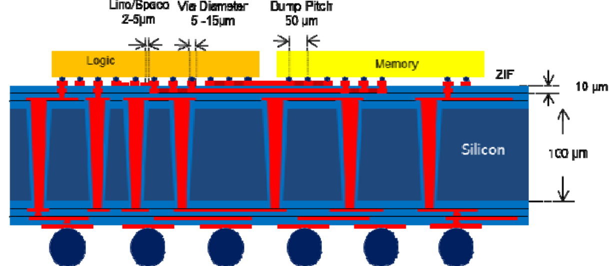

Figure 9. 2.5D Silicon Interposer Assembly

To achieve low-cost at ultra-fine-pitch RDL, the major challenges are transmission-line impedance match and the Cu-line formation processes. With 2µm line width and 4µm line height of microstrip transmission lines, the required dielectric thickness to achieve 50 ohm impedance is only 1.4µm. This is very hard to achieve. Thinner dielectric polymers and embedded lines are two ways to solve this problem. To achieve low-cost Cu wiring, semi-additive processes were applied. The semi-additive process involves Cu seed layer deposition, photolithography, and Cu-line metallization. In the GT approach, each step was controlled to achieve low cost. The GT approach uses electroless-plated Cu on ZIF polymer dry film dielectrics to form the RDLs.

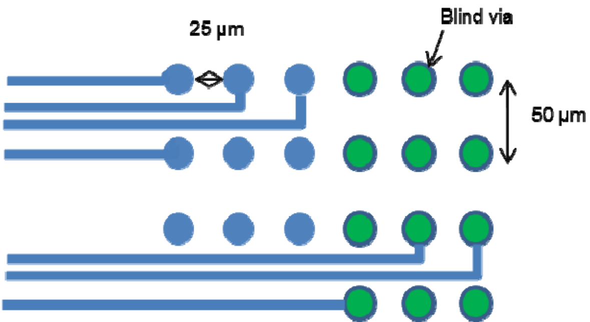

Figure 10. 2-Metal Layer Escape Routing Strategy

ELECTRICAL CHARACTERIZATION

Electrical design and characterization of TPVs and transmission lines were performed, as shown in Figure 11 to obtain S-parameter measurements. Four-metal layer test vehicles were designed and fabricated to form silicon interposers with coplanar wave guide (CPW) lines. The resistivity and thickness of the silicon used was 0.5 Ω-cm and 200μm, respectively, with a polymer-liner thickness of 40μm. The fabricated-CPW lines were 120μm wide. The gap between the signal and ground was 36.5μm. Frequency-domain simulations were carried out for TPVs using full wave EM solvers. The VNA measurement was performed with SOLT calibrations. Low signal loss is a key important parameter for longer RDL lines (4-8mm) that are routed between two dies in the 2.5D interposer. The 7mm signal lines fabricated were characterized to have less than -0.03dB of insertion loss, up to 10Ghz. This lower insertion loss is attributed to the thick polymer liner of very high resistivity. Thus, CPW lines in wafer or panel-silicon interposers are capable of handling high-speed digital signals with nominal distortion.

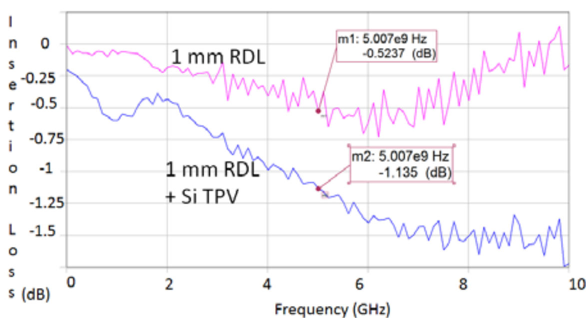

Figure 11. Insertion Loss of RDL Lines in GT's Silicon Interposers

SUMMARY

As organic packages reach their limits in I/Os, thermal and reliability performances, silicon interposers are being developed using BEOL processes in the wafer fabs. But such interposers have two main problems: high cost and low performance. The Georgia Tech approach addresses both these problems as described in this paper.

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