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Latent Short Circuit Failure in High-rel PCBS Caused by Lack of Cleanliness of PCB Processes and Base Materials

Stan Heltzel, European Space Agency
Components Technology and Space Materials Division
Noordwijk, Netherlands
Stan.Heltzel@esa.int

Brief Biography:
Stan Heltzel (1975) works at the Materials Technology Section of the European Space Agency since 2008 where he is responsible for qualification of Printed Circuit Board manufacturers and technology. Analysis of PCB samples and exposure to simulated space environment occurs in the materials and components laboratories. From 2001 to 2008 Stan worked on environmental testing facilities, exposing materials and solar cells to simulated solar radiation. Stan has a Bachelor degree in Applied Physics.

***Abstract*— Latent short circuit failures have been observed during testing of Printed Circuit Boards (PCB) for power distribution of spacecraft of the European Space Agency. Root cause analysis indicates that foreign fibers may have contaminated the PCB laminate. These fibers can provide a pathway for electromigration if they bridge the clearance between nets of different potential in the presence of humidity attracted by the hygroscopic laminate resin. PCB manufacturers report poor yield caused by contamination embedded in laminate. Inspections show that fiber contamination is present on prepreg and etched inner layers. Further fiber contamination may be attracted in the manufacturing environment due to static charging. The requirements for cleanliness that are specified for final PCBs are orders of magnitude more stringent than those specified for base materials. This paper describes inspections performed on base materials, manufacturing processes and final PCBs. It describes test methods that detect reduced insulation caused by contamination and Electromigration. Moreover, a proposal is presented specifying tightened requirements for a new class of base materials for the manufacture of high-rel PCBs.**

Keywords—PCB; cleanliness; contamination; quality; base materials; short circuit;

I. INTRODUCTION

Latent short circuit failures have been observed in Printed Circuit Boards (PCB) during testing of power distribution units of spacecraft for the European Space Agency (ESA). Root cause analysis has been conducted under review of Non-conformance Review Boards (NRB). PCB assemblies failed after prolonged functional testing in ambient laboratory environment or after thermal vacuum cycles. Due to the large amount of damage caused by the electrical overstress, it was not possible to obtain direct evidence of the failure. However, a working hypothesis has been developed indicating that fiber contamination may have caused a latent short circuit. This hypothesis was further substantiated by reports on contamination issues in base materials and by a test method that demonstrated the breach of insulation due to fiber contamination.

At the time of the observed failures at equipment level, PCB manufacturers reported poor cleanliness levels of base laminate materials causing poor yield. It is not possible to screen in an efficient manner for contamination in copper clad laminate, since visual inspection requires stripping of the copper. Several inspection methods show the lack of cleanliness of base materials, which is specified in IPC-4101 [8]. This paper identifies a major gap between the requirements specified on base materials and the requirements on manufactured PCBs and presents a proposal for a new class of cleaner base materials for the manufacture of high-rel PCBs.

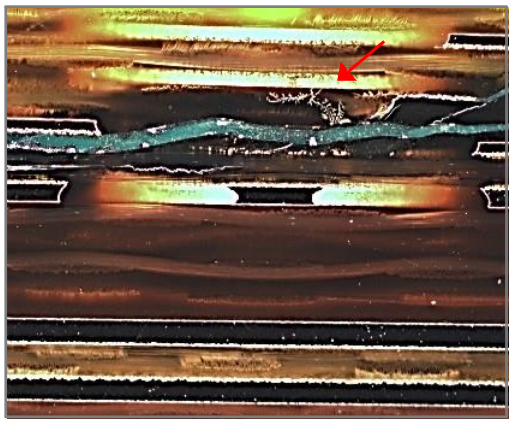

Fig. 1. Cross section of a failed PCB showing extensive damage due to electrical overstress and a dendritic structure.

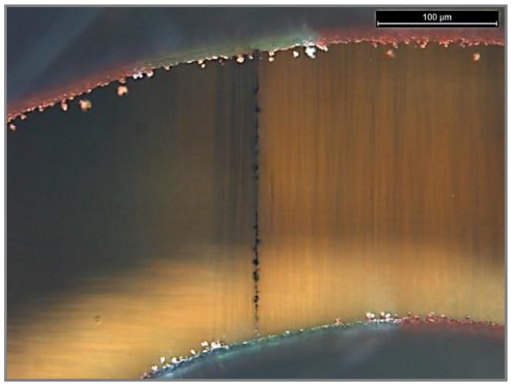

Fig. 2. In-plane section of a failed PCB showing a trace of electrical discharge along glass fibers in the clearance of a via through a plane.

The processes of PCB manufacturing are an additional contributing factor to possible contamination in the dielectric insulation. PCB manufacturers are audited for their cleaning methods on etched inner layers and on prepreg prior to stack-up for lamination. Recommendations have been issued [1] for a cleanliness control plan, for in-process inspections and for electrical testing on final PCBs [5].

Concerns with cleanliness of PCBs initiated the formation of a dedicated working group comprising of space agencies, original equipment manufacturers, satellite integrators and PCB manufacturers. The objectives of the working group are to inventorise the sources of contamination and to define risk mitigations, as described in the present paper.

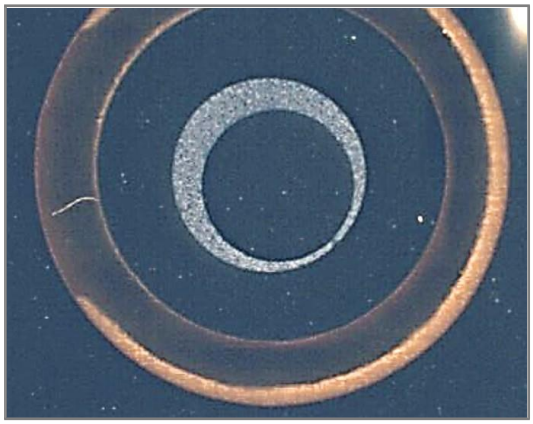

Fig. 3. In-plane section of a failed PCB showing fiber contamination in a clearance of a plated through-hole.

II. FAILURE MECHANISM

A. *Electrochemistry*

For electrochemistry to occur, the following factors need to be present: a pathway, an electrolyte (i.e. ions in a mobile substance) and a bias voltage [2].

Dendritic growth is a type of electromigration causing metallic deposition from the cathode. It is typically associated with surface migration. Use of flux in assembly can contaminate the surface and increase the probability of dendritic growth. Surface properties have been the main focus of specifications for PCB cleanliness and for Surface Insulation Resistance (SIR) tests.

Conductive Anodic Filament (CAF) growth is a specific type of electrochemistry causing copper salts to deposit from the anode along the glass-resin interface. CAF is typically associated with subsurface electrochemistry. Thermal stress deteriorates the glass-resin interface which increases the susceptibility to CAF. Hollow glass fibres provide another pathway for CAF.

B. *Discontinuities in laminate*

Any kind of inhomogeneity within the dielectric material can provide a pathway for electromigration. Bromine flame retardants have a limited solubility in polyimide resin and may separate during high-pressure lamination. Conglomerations can be formed by the flame retardant or, likewise, by ceramic fillers, as typically used in epoxy materials with high glass transition temperature. Manufacturing problems causing voids or delamination can degrade the insulating properties. A brittle resin system prone to cracking has previously been subject of ESA Alert EA-2010-MAT-12-B after critical short circuit failure in a power application during ground based testing.

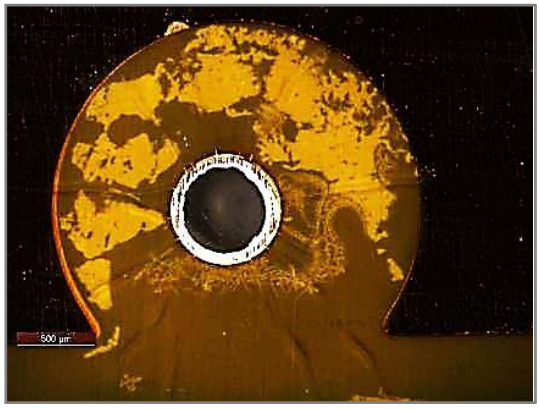

Fig. 4. In-plane section of a via showing radial resin cracks and a dendritic structure on a delaminated flex layer.

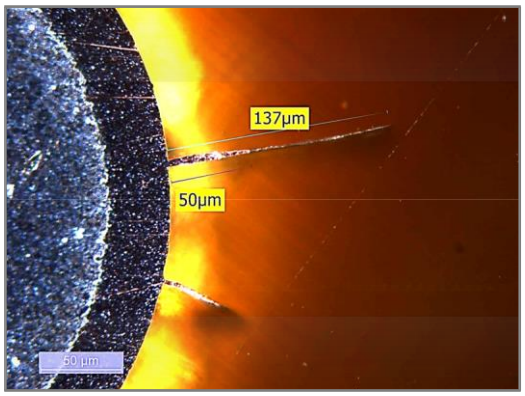

Fig. 5. In-plane section of a via without capture pad showing cracks and copper ingress caused by drilling in brittle resin.

In addition to the above, PCB laminate can be contaminated by foreign material, such as chemical residues from the production process, epoxy resin dust in polyimide laminate, metallic debris, dust or fibers. Contamination of PCB laminate by foreign fibers can provide a pathway for electromigration if fibers bridge the clearance between nets of different potential. Mobility within the PCB laminate can be provided by humidity. PCBs for space applications are typically made from polyimide laminates, which are thermally stable materials. However, polyimide resin is hygroscopic. Small amounts of chemicals can provide mobile ions creating a conductive electrolyte, even when cleanliness requirements for PCBs are met.

Another problem associated with contamination is loss of insulation caused by metallic particles or by carbonization of organic contaminants during lamination or during assembly. These failure mechanisms occur earlier and are easier to detect compared to the latent short circuit caused by electromigration.

C. Sources of contamination

Contamination of dielectric materials can occur in the PCB manufacturing process and in base material manufacturing. PCB manufacturers procure copper clad laminate and prepreg sheets from base material suppliers. The PCB manufacturer is in control of cleanliness in prepreg layers and on the surface of etched innerlayers. The base material supplier is in control of the cleanliness inside copper clad laminate and also of the cleanliness of prepreg.

PCB manufacturers report poor cleanliness levels in base materials and low yield as a result. In addition, audits of PCB manufacturers show that there is variation in cleanliness of the manufacturing environment and in the cleaning methods used on internal layers.

D. PCB design

IPC-2221 is a standard that is commonly used to specify insulation distance in a PCB as a function of voltage. Manufacturing tolerances are often overlooked when implementing design rules. In one failed PCB assembly, a 4 mil (100 µm) laminate was used to accommodate a voltage of 100 V between copper planes. This was intended to comply with 1 kV/mm as specified in IPC-2221. However, worst-case projected peak-to-peak insulation distance includes tolerances for laminate thickness as well as for copper surface profile. A thickness tolerance of 13 µm is specified in IPC-4101 for class C laminate with nominal thickness of 4 mil. A maximum copper foil profile of 10 µm is specified in IPC-4562 for a nominal foil thickness of 70 µm. Adding these tolerances can give a projected peak-to-peak insulation distance of about 68 µm for a nominal thickness of 4 mil.

Likewise, etching tolerances need to be included when specifying intralayer insulation distances between conductors in-plane of the PCB. Recently, PCB design specified in ECSS-Q-ST-70-12C [3] has been endorsed by the space industry. This standard takes worst-case manufacturing tolerances into account when specifying voltage rating.

Double insulation is a frequent requirement for critical high voltage signals in space applications. ECSS-Q-ST-70-12 specifies for the first time a set of PCB design rules that combines the use of two individually cured insulators as well as additional margin for voltage rating of critical signals.

Furthermore, the ECSS-Q-ST-70-12 specifies the presence of non-functional pads to mitigate the risk of drilling cracks in resin-rich areas and it specifies the use of two sheets of prepreg between copper layers as well as two layers of woven glass reinforcement in laminate, to mitigate the risk of contamination.

Evolutions in the capability of electronic industry have caused denser PCB designs, combining signal and power circuits with large ground planes, thick copper layers, thin dielectric insulation and dense component assembly. While PCB design may not have been taking full account of manufacturing tolerances, this cannot be considered the root cause of failures. The electrical strength of laminates provides an order of magnitude margin compared to the design rule for voltage rating. However, PCB materials are not perfect and requirements are specified for tolerable imperfections. Conservative PCB design is, therefore, an important risk mitigation.

III. INSULATION RESISTANCE TEST

Conventional SIR test equipment was used in a recent investigation [4] to measure insulation resistance (IR) on internal layers. The test was set-up in support of the working group on the ECSS-Q-ST-70-12 and had the objective to verify the voltage rating of 1 kV/mm for space applications. PCB coupons were manufactured using various base materials by two different PCB manufacturers. Coupons were submitted to thermal cycling representing end-of-life for space applications. Before and after thermal cycling, coupons were characterised by IR testing at 75% relative humidity (RH) and 85 ºC while a bias voltage of 100 VDC was applied across comb patters with intralayer insulation distances of 100, 150 and 200 µm.

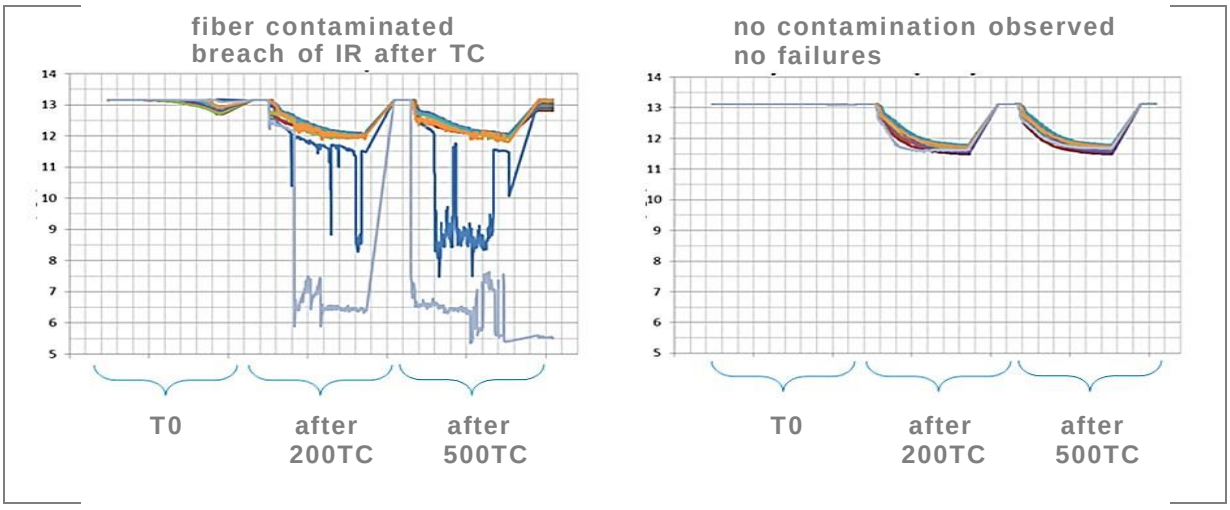

Fig. 6. Insulation resistance (log Ω) before and after thermal cycles (TC) from -65ºC to +135ºC, showing two failed innerlayers of a comb pattern that appeared to be fiber contaminated.

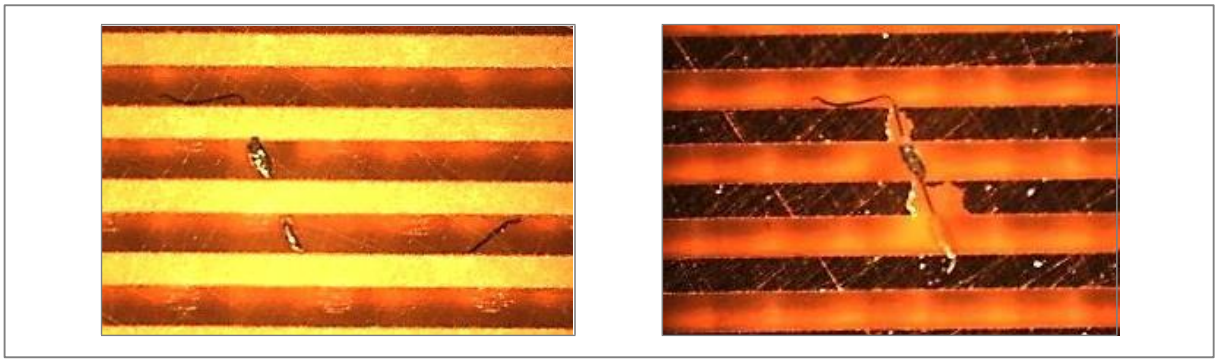

Fig. 7. In-plane sections of comb pattern after progressive polishing showing copper migration from the conductor along the fiber contamination.

An unexpected result of the test campaign was that one set of coupons appeared to be contaminated with fibers, which caused breach of insulation after thermal cycling. After the campaign, the short circuit was located using infrared thermography while applying a low current. Destructive Physical Analysis (DPA) was performed and progressive polishing finally revealed the fault location. In all cases for which the fault location could be identified in this manner, it was observed that the breach of insulation was associated with fiber contamination. In some cases it was evidenced that copper migrated from the comb pattern and re-deposited along the fiber. The fibers were observed in prepreg layers and therefore associated with the PCB manufacturing processes.

The main conclusion in support of the ECSS-Q-ST-70-12 was that the insulation at end-of-life was adequate for the field strength of 1 kV/mm, provided that no contamination was present. The other main conclusion was that fiber contamination in PCB laminate provides a pathway for electromigration to occur and can lead to latent short circuits in PCBs.

A similar test campaign has recently been performed on coupons that were manufactured by using different cleaning methods on innerlayers and prepreg sheets, prior to lay-up for lamination. It showed that the risk of breach of insulation could be significantly reduced by cleaning internal layers.

IV. RISK MITIGATIONS AT PCB MANUFACTURER

A. Sample inspection on base laminate

IPC-4101 [8] specifies sample frequency and criteria for acceptability of sub-surface imperfections. Some PCB manufacturers use this as a test method for incoming inspection of batches of base laminates. The method may be inefficient, since copper cladding needs to be etched from the laminate before inspection is possible, after which the laminate cannot be used anymore for PCB manufacture. Furthermore, the sample size needs to be significant to provide reliable statistics due to the probabilistic nature of contamination. Nevertheless, this method is a useful addition to the total package of risk mitigations, as it provides the PCB manufacturer with a simple quantification of cleanliness. In case of non-compliance to IPC-4101, the results can be used to return the batch and to file a claim with the base material supplier.

One PCB manufacturer gathered reliable statistics over a period from Jan 2012 until Feb 2014 and reported that about one third of incoming batches did not comply with requirements from IPC-4101 and another 8% did comply with IPC-4101 but did not comply with internal requirements. The base material supplier accepted all claims, also those that were strictly in compliance with requirements of IPC-4101.

Fig. 8. Top view of a laminate after etching of copper cladding, showing a plant seed embedded in the dielectric material, probably carried into the clean room on clothes of personnel. The scale is in mm.

Fig. 9. Top view of a prepreg showing an embedded insect.

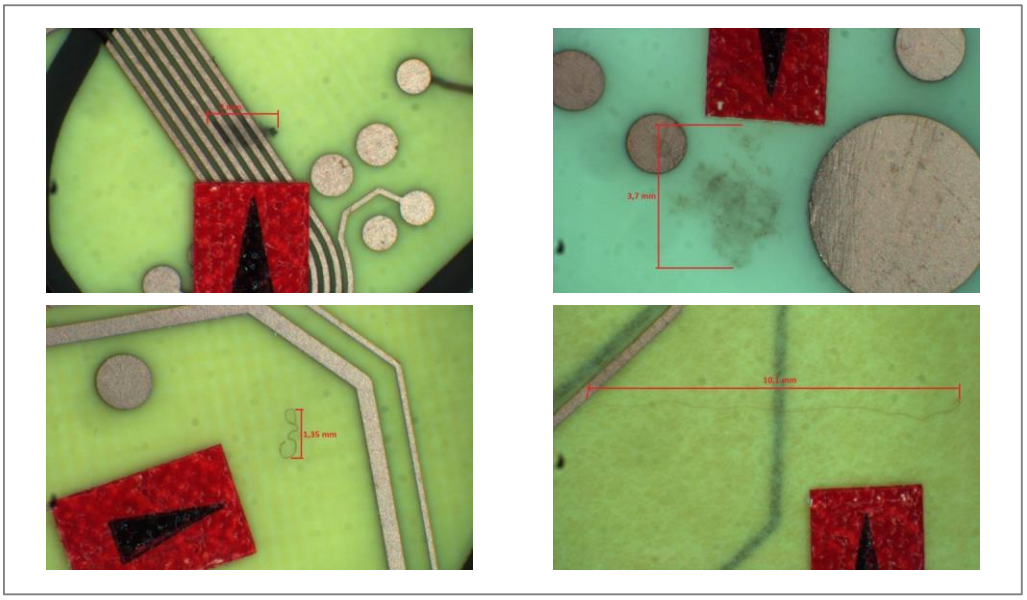

Fig. 10. Examples of etched innerlayers scrapped due to the presence of contamination.

B. Inspection on etched inner layers

To overcome the lack of statistical significance of sample inspections on base laminates, one PCB manufacturer implemented a 100% visual inspection of clearances on etched innerlayers using a light table. During manufacture of a critical batch of PCBs for a power unit, it was reported that 130 innerlayers were scrapped out of a total of about 10'000, due to the presence of embedded contamination as shown in figure 10. Not only is this a laborious inspection method; in addition low yield has a high cost impact that late in the manufacturing process flow.

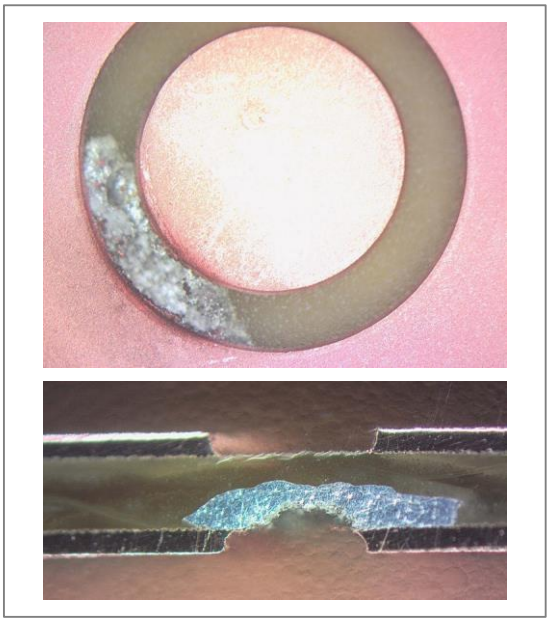

Fig. 11. In-plane view (top) of contamination embedded in clearance of etched innerlayer and cross section (bottom).

The visual inspection step is complementary to Automated Optical Inspection (AOI). This latter test equipment verifies the conductive circuit and discriminates the circuit from the dielectric by the specular or diffuse reflection. It is typically not considered to be an efficient method for determining discontinuities within clearances when these have similar optical properties. However, recently one PCB manufacturer provided contaminated etched inner layers to an AOI supplier for their assessment by new software using grey scales to successfully detect contamination.

Both visual inspection and AOI can only be performed in clearances and do not provide information of the quality of dielectrics below surface copper. This is a problem on plane layers when only a small amount of copper is etched away. A breach of insulation between layers is possible in case of particulate contamination when it penetrates the layers of woven glass reinforcement. This has been seen for chlorine bearing particles and metallic debris. This failure mechanism has been the reason to require a minimum of two layers of glass reinforcement between copper layers. Contamination caused by fibers or chemical residue is considered to be more of risk for in-plane insulation and this can be mitigated by the visual inspection and an efficient AOI method.

C. Cleanliness in the PCB production area

The PCB manufacturing processes take place in an industrial environment, which add to the risk of contaminating innerlayers with dust particles or fibers, for instance. Copper surface treatment of innerlayers includes a drying process as a last step. Air filtration needs to be verified for this process. Furthermore, this process is prone to static charging of inner layers. This is also the case for polymeric interleavers that are used to separate and protect innerlayers. Prepreg sheets also show a large amount of static charging.

Interleavers, transport trolleys, trays and work benches that are in contact with interlayers and prepreg should be inspected and cleaned regularly. The lay-up area in which etched innerlayers and prepreg are stacked up prior to lamination, should be under control by clean room practices such as air filtration, humidity control, overpressure, regular cleaning, protective clothing, restricted access, smooth unpainted surfaces, etc. Furthermore it is recommended to implement laminar flow benches for lay-up and the use of de-ionisation equipment. These recommendations are specified in [1] and have become subject to audit of PCB manufacturers.

D. Cleaning and inspection of innerlayers and prepreg at lay-up

Due to the fact that the environment of PCB manufacturing is relatively uncontrolled with respect to cleanliness and PCB materials and consumables are prone to static charging, it is essential that a cleaning step is implemented prior to lamination. The best process for last-minute cleaning is the lay-up. The use of so-called tacky rollers, based on Van der Waals attraction of particles without risking to contaminate the rolled surface with an adhesive residue, is widely endorsed. Cleaning of prepreg sheets, however, is not so widely performed.

Verification of the efficiency of the cleaning can be done by visual inspection under bright light and ultraviolet (UV) light. UV flash lights as well as bright lights are readily available in various wavelength ranges. Using UV light inspection it was shown that sealed bags of polyimide prepreg are occasionally contaminated as delivered from the base material supplier. Polyimide resin dust was shown not to be fluorescent, whereas epoxy resin as well as dust fibers do show UV fluorescence. Either source of contamination is unacceptable in polyimide production processes at high temperature.

Fig. 12. Inspection of a sealed bag of polyimide prepreg showing UV fluorescence of particulate contamination.

One PCB manufacturer performs vacuum cleaning on etched inner layers as well as on sheets of prepreg. Special non-contaminating brushes are used and the motor and air exhaust of the vacuum system is placed outside the clean room.

Another PCB manufacturer recently demonstrated the efficiency of different cleaning methods using rollers and vacuuming. Sample coupons were manufactured using different cleaning methods and were submitted to IR testing, as previously described.

E. Inspection on external layers of final PCB

As part of the release procedure for the final PCB, a visual inspection is performed on external layers to detect defects in the surface finish, circuit or clearances. It is common for PCBs for space applications to be designed with laminate on outer layers, rather than copper foil and prepreg. Contamination embedded in laminate remains covered by copper cladding throughout the production process, until the final tin-lead pattern plating and etching process on the outer layer. Rejecting a final PCB often affects on-time delivery.

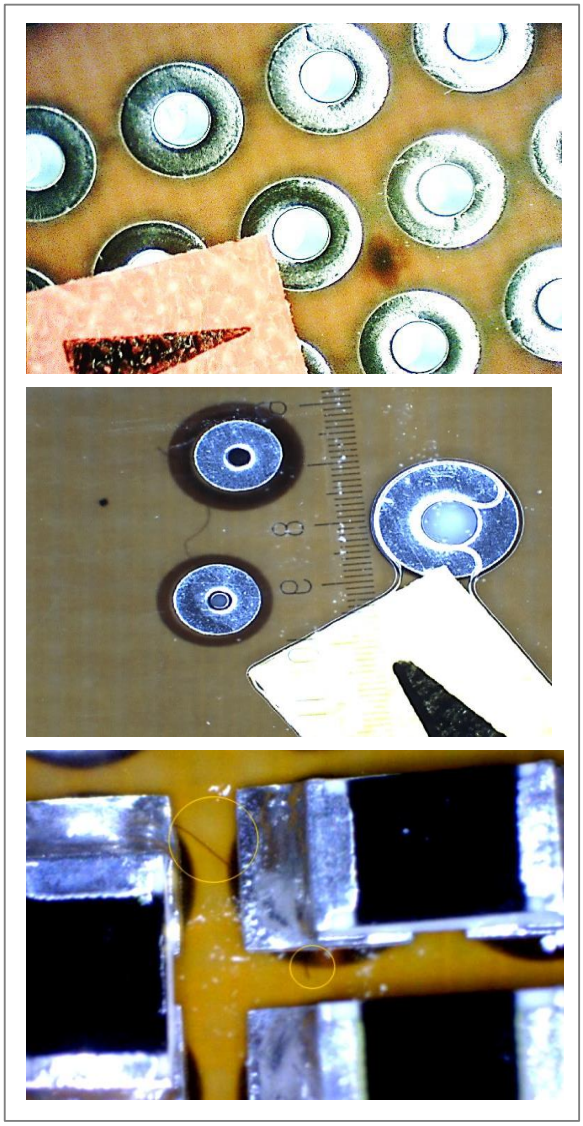

Fig. 13. Contamination embedded in base laminate on external layers bridging the insulation between pads, at outgoing inspection and after assembly.

In some recent cases, small but critical fiber contamination remained undetected at outgoing inspection as well as incoming inspection at the customer, which is described as NC#1 as part of ESA Alert EA-2014-EEE-3-A. Only after assembly and conformal coating, it was discovered that fiber

contamination was embedded within the outer layer laminate and bridging the gap between pads. Waiving such non-conformance by repair and testing under careful assessment by NRB was performed but requires high effort and cost, in particular when the delivery of the PCB assembly is on the critical path of satellite integration.

F. Electrical testing

Typical electrical testing applied on PCBs by flying probe equipment, is specified in IPC-9252 and is based on an insulation threshold of 10 MΩ, corresponding to level C for IPC class 3. The objective of this test method is to verify electrical design, i.e. the absence of unintended connections in the circuit. For IPC class 3/A this test method is amended in IPC-6012 to 100 MΩ under 250 V bias.

The working group specified a new high resistance electrical test method [5] with a 1 GΩ threshold and monitoring of Voltage during ramp-up, to determine the quality of the insulation and to detect possible imperfections in the dielectric material. The rationale is that contamination between nets can provide a high-Ohmic path that can be detected under high voltage bias and therefore fails this test. The requirement for GΩ insulation resistance is specified in ECSS-Q-ST-70-10C [6] and is substantiated by the typical volume resistivity of 10^8 MΩ-cm, determined on dielectric materials at humid conditions of 90% RH in accordance with IPC-TM-650 2.5.17.1.

During recent use of this test method, one PCB manufacturer reported failure of a PCB at 160 MΩ insulation. When the PCB was submitted to 250 V sustained for a longer period of 1 minute, the net eventually failed in short circuit. Subsequent analysis and DPA showed particulate contamination in a 4 mil base laminate. Scanning Electron Microscopy (SEM/EDX) identified the presence of Titanium and Iron, among others. The high-Ohmic path would have remained undetected with other test methods.

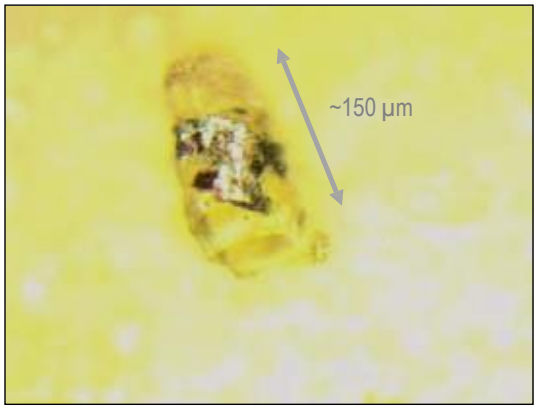

Fig. 14. In-plane section of particulate contamination with metallic constituents embedded in base laminate causing high-Ohmic short.

V. RISK MITIGATIONS AT BASE MATERIAL SUPPLIERS

A. Observations on base materials

It has been identified that various production processes may contribute to the cleanliness level of dielectric insulation of a PCB. PCB manufacturers that are qualified in accordance with ECSS-Q-ST-70-10C [6] are subject to an audit process that assesses the implemented risk mitigations. This is however not the case for base material suppliers.

PCB manufacturers perform sample screening on laminates, they perform in-process screening on etched inner layers and on prepreg sheets during lay-up and they perform root cause investigation when a final PCB fails electrical testing. The results obtained from these inspections are presented in the previous chapter and show varying level of quality of base materials. In some cases, contamination is identified that exceeds the requirements of IPC-4101 [8]. In other cases, contamination is identified that is within the requirements of IPC-4101 but is still proven to be unsuitable for PCB manufacture in high-rel applications.

B. IPC-4101 Specification for base materials

The concerns regarding lack of cleanliness on base materials have been addressed to the IPC subcommittee 3-11, which is responsible of updating the IPC-4101 [8] to revision D. This standard currently has non-stringent requirements for the sample size of screening and for acceptance criteria of subsurface imperfections. Although the sample screening on a batch of laminate may be statistically inefficient, it does provide a simple method to quantify cleanliness level, against which base material suppliers can be held accountable. One remarkably weak requirement of IPC-4101 is to permit fiber contamination up to 13 mm length. This is in contrast with IPC-6012 that does not allow foreign inclusions that reduce dielectric spacing to below the minimum requirement for class 3/A PCBs for space application. As a comparison, common PCB design for space may use in-plane insulation in the order of 0.5 mm, with a minimum as-manufactured of 0.15 mm for 100 V, as specified in ECSS-Q-ST-70-12.

A proposal with tightened requirements for a new class of cleaner base materials has been drafted [7] and presented to the IPC subcommittee. This proposal requires 100% visual inspection on prepreg prior to copper cladding for the manufacture of laminate as well as on prepreg to be provided as b-stage cured sheets to PCB manufacturers. Furthermore, the proposal requires fibers to be evaluated as opaque foreign matter limiting its size to 0.5 mm. A sample inspection of 2% is required for batch acceptance of laminates. Some base material suppliers report good experience with high-pot testing on thin laminates. This is specified as an optional test method to be agreed between supplier and customer.

C. Procurement specification to base material suppliers

The proposal described above cannot be seen separate from the other risk mitigations. The proposed requirements can still cause latent short circuits when contaminants are situated in a critical area with minimum spacing. It has been seen, however, that base material suppliers on occasion struggle to achieve the

current requirements on IPC-4101. Implementing a more stringent specification is, therefore, expected to necessitate better cleanliness control. Moreover, the required inspections for batch release provide accountability.

The proposed specification does not describe an ideal material. It is rather deemed to be a compromise that is realistically achievable in an attempt to define a new class of cleaner base materials. It is not the intention to specify requirements on a unilateral basis that cannot be achieved by base material suppliers. This is for instance the case for the copper foil class D surface roughness specified in IPC-4101, which appears to be unavailable from most suppliers.

Therefore, the proposed specification has recently been provided to key suppliers of base materials for review and for their Statements of Compliance. The cost of investments may be difficult to carry by the base material suppliers since the European space industry is a niche market. This may have a commercial impact that remains to be assessed by the entire supply chain. However, the recent feedback from key suppliers has been positive.

VI. CONCLUSIONS

Latent short circuit failure of power PCBs has been associated with fiber contamination of the dielectric material. Tests and inspections have shown various sources of contamination in laminate, prepreg and on etched innerlayers. It has been demonstrated by IR tests that contamination can cause breach of insulation due to electromigration.

Risk mitigations have been specified in PCB design, PCB manufacture and base material supply. These include conservative design of insulation, inspection on base laminates and prepreg, in-process inspections on etched innerlayers, clean room practices in manufacture, cleaning of innerlayers and electrical testing on final PCBs.

IPC-4101 specifies a cleanliness level for base materials that is in conflict with high-rel PCB manufacture and requirements for insulation specified for IPC class 3/A. A specification for a new class of cleaner base materials is being issued to key base material suppliers and is proposed to be included in a revision of IPC-4101.

ACKNOWLEDGEMENT

This paper summarises collected results obtained within the PCB-SMT working group of the Component Technology Board, a supporting unit of the European Space Component Coordination. This working group includes representatives of the space agencies CNES and ESA, satellite integrators Airbus, Thales Alenia Space and RUAG and qualified PCB manufacturers TESAT Spacecom, PrinctaGRAPHIC, Systronic, and Invotec. Moreover, improvements in PCB design have been the subject of the working group on the ECSS-Q-ST-70-12. Working group members contributed extensively to the common know-how presented in this paper. Moreover, key base material suppliers have supported the working group in the understanding of cleanliness issues in critical processes and in defining risk mitigations. Without their commitment to the high-rel space market it would not be possible to improve on quality.

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