THE LAST WILL AND TESTAMENT OF THE BGA VOID

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ABSTRACT
The impact of voiding on the solder joint integrity of ball grid arrays (BGAs)/chip scale packages (CSPs) can be a topic of lengthy and energetic discussion. Detailed industry investigations have shown that voids have little effect on solder joint integrity unless they fall into specific location/geometry configurations. These investigations have focused on thermal cycle testing at 0°C-100°C, which is typically used to evaluate commercial electronic products. This paper documents an investigation to determine the impact of voids in BGA and CSP components using thermal cycle testing (-55°C to +125°C) in accordance with the IPC-9701 specification for tin/lead solder alloys. This temperature range is more typical of military and other high performance product use environments. A proposed BGA void requirement revision for the IPC-JSTD-001 specification will be extracted from the results analysis.

BACKGROUND
The subject of voids in BGA solder joints in the electronics industry was highly controversial in the late 1990s and early 2000s. One school of industry thought held that a void in a solder joint would be a stress riser that initiated cracks, leading to solder joint failure. An opposing school of thought was that voids act as crack arrestors, which improve solder joint life. The root cause of voids in BGA solder joints is well understood by the electronics industry with a number of papers published on the topic [1, 2, 3]. R. Aspandiar characterized and classified BGA solder joint voids into several categories with assigned root causes that are widely utilized as 'the' industry void definition standard [4]. Macro voids have been the focus of the electronics industry for influencing solder joint integrity. These voids are the result of assembly process issues and do not have material or design root causes. Macro voids are due to assembly variation that can be eliminated with matched material and consistent process parameter selection/control. Other solder joint void types are primarily influenced by product/process design selection in the printed wiring assembly design phase. Figure 1 illustrates Aspandiar's solder joint void classifications.

Figure 1. Solder Joint Void Classifications [4]

The following sections summarize published literature on the impact of voids in BGA solder joints found during the authors' literature review.

Study #1:
D. Banks et al "The Effects of Solder Joint Voiding on Plastic Ball Grid Array Reliability" [5]

Investigation Specifics:
- 225 I/O Plastic BGA, daisy chained, 0.762mm (30 mil) diameter solderball
- Sn63 solder paste
- Test vehicle: 1.57mm thick (62 mil), FR-4, 2 internal planes
- Thermal cycling: 0°C-100°C, 5 minute dwells, 10 minute ramps, 8000+ cycles

Investigation Conclusion:
- Typical void size was 2-3% diameter, overall range was 0-24% diameter
- Voids were typically found at solder joint / BGA package interface
- Voids did not appear to alter crack propagation path

- Voids had no effect on solder joint integrity (Figure 2)
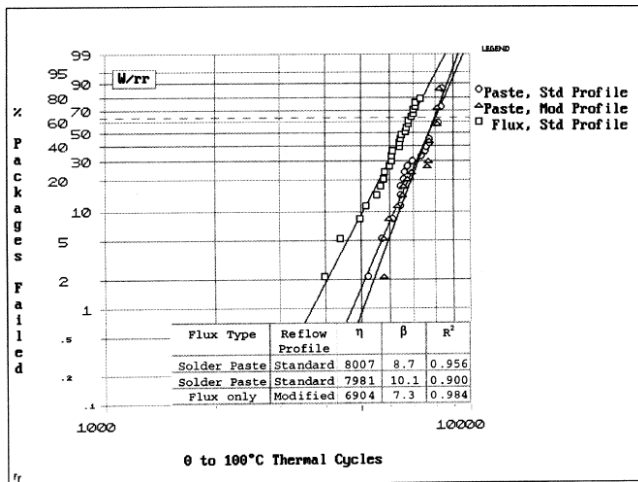
Figure 2. Failure Data Weibull Plot from Banks [5]

Figure 2 illustrates Weibull plots that show that BGAs with voids (i.e. Mod Profile) and BGAs without voids (i.e. Standard Profile) did not have distinguishable solder joint failure populations. Banks' work was one of the earliest published tin/lead solder alloy investigations to demonstrate that macro voids did not interact with the solder joint failure cracks and their presence did not cause solder joint failure.

Study #2:
IPC Solder Products Value Council (SPVC), "The Effect of Voiding in Solder Interconnections Formed from Lead-free Solder Pastes with Alloys of Tin, Silver and Copper" [6]

Investigation Specifics:
- Variety of BGAs and CSPs, daisy chained, various solder ball diameters
- SnPb and SAC solder pastes
- Test vehicle one: 2.36mm thick (93 mil), FR-4, 6 internal planes
- Test vehicle two: No data provided
- Thermal cycling: 0°C-100°C, 10 minute dwells, 20 minute ramps, 6000+ cycles

Investigation Conclusion:
- Both test vehicles had voiding greater than 25% of the X-ray image area in multiple components
- SAC solder had more voids than SnPb solder
- No correlation was found between void size and solder joint integrity (Figure 3)
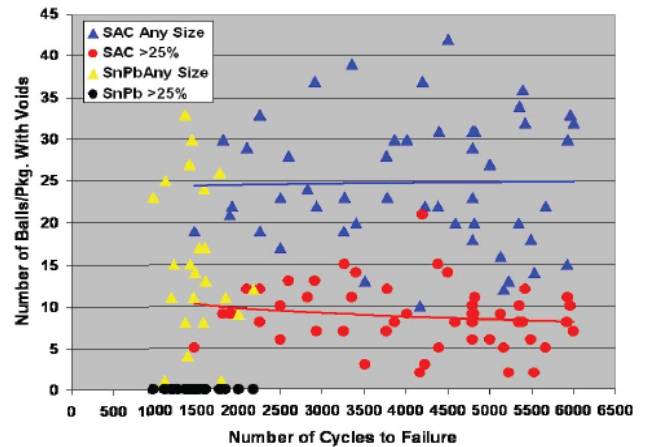
Figure 3. Solder Joint Voiding Versus Cycles to Failure for CSP84 Component [6]

The SPVC investigation demonstrated that the number of cycles to failure did not correlate with void size. If there was a negative influence of voids the solder joint integrity, Figure 3 would show a cluster of early low cycle failures for larger voids and a cluster of late cycle failures for the small voids. This was not the case; the results show a uniform data spread for the number of cycles to failure for both void size populations, with no distinctly different groups for either the tin/lead or lead-free solder alloys.

Study #3:
D. Kim et al, "Effect of Voiding on Solder Joint Shock and Thermal Cycle Reliability" [7]

Investigation Specifics:
- Variety of BGAs, daisy chained, 1.0mm pitch, various solder ball diameters
- SnPb solder paste
- Test vehicle one: 2.36mm thick (93 mil), FR-4, 8 internal planes, OSP finish
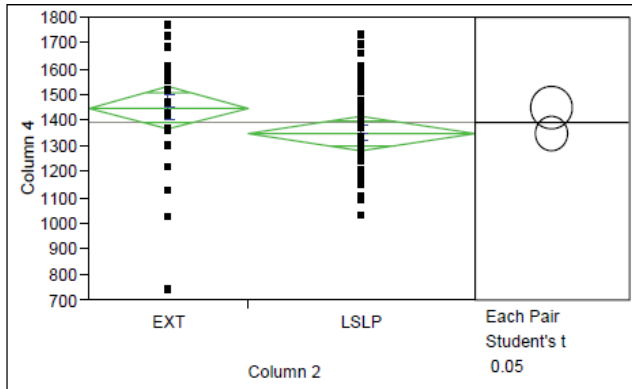- Thermal cycling: 0°C-100°C, 5 minute dwells, 10 minute ramps, 3500 cycles

Investigation Conclusion:
- Typical void size range was 0-60% of solderball diameter
- Solder crack path typically found at solder joint / BGA package interface
- BGAs with 50% of their solder joints containing voids in the 35-60% solderball diameter range had no negative effects on solder joint integrity (Table 1)

Table 1. D. Kim Characteristic Failure Cycles at 0°C-100°C Temperature Range [7]

Solder ball	Eutectic				2%Ag			
Reflow profile	LSLP		Extreme		LSLP		Extreme	
Preconditioning	Precon	No precon	Precon	No precon	Precon	No precon	Precon	No precon
144 I/O BGA	1443 β=8.8	1406 β=7.3	1520 β=6.9	1233 β=6.7	1374 β=7.7	1475 β=9.6	1452 β=5	1637 β=11.5
165 I/O BGA	Only few failures occurred, and thermal cycling stopped at 3500cycles							
1657 I/O FCBGA	NA				Only few failures occurred, and thermal cycling stopped at 3500cycles			

Kim's investigation utilized two different reflow profiles – typical (aka LSLP) and non-typical (aka Extreme) – to generate voids in the BGA solder joints. The LSLP reflow profile produced minimal voiding whereas the Extreme reflow profile resulted in voiding as large as 60% of the solderball diameter. Preconditioning of the BGAs prior to reflow (10 days of 60°C/60%RH) was included in the test as an additional technique for generating voids. Analysis of the thermal cycle results revealed that there was no statistically significant difference between the void and void-less solder joint populations for the 144 I/O BGA components (Figure 4).

Figure 4. Statistical T-Test for Solder Joint Voiding Showing Indistinguishable Failure Populations [7]

Study #4:
S. Sethuraman et al, "The Effect of Process Voiding on BGA Solder Joint Fatigue Life Measured in Accelerated Temperature Cycling" [8]
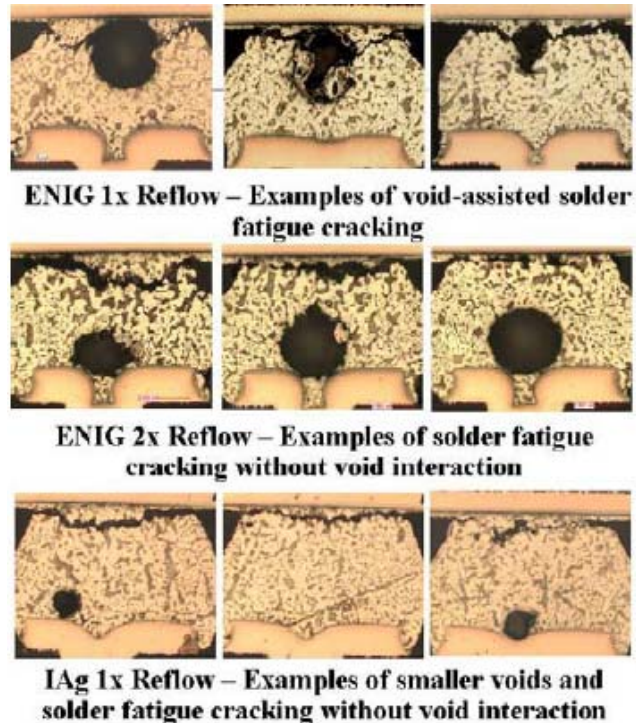
Investigation Specifics:
- 84 I/O Plastic CSP, daisy chained, 0.3mm (12 mil) diameter solderballs
- Sn63 solder paste
- Test vehicle: Characteristics not available, Immersion Silver (IAg) and ENIG finishes
- Thermal cycling: 0°C-100°C, 10 minute dwells, 10 minute ramps, 1000+ cycles

Investigation Conclusion:
- Typical void size was range was 0-65% of X-ray image area
- Solder crack path typically found at the solder joint / BGA package interface

- Void size alone was insufficient to define acceptance for solder joint reliability
- Solder voiding only reduced the reliability when the voids were located in the crack path (Figure 5)

ENIG 1x Reflow – Examples of void-assisted solder fatigue cracking

ENIG 2x Reflow – Examples of solder fatigue cracking without void interaction

IAg 1x Reflow – Examples of smaller voids and solder fatigue cracking without void interaction

Figure 5. Solder Joint Void Versus Crack Path Interaction, S. Sethuraman et al [8]

The Sethuraman investigation demonstrated that the solder void location, rather than the solder void size, is the primary mechanism by which voids can reduce solder joint integrity. Only voids in the solder joint crack propagation path reduced the solder joint thermal cycle life.

Study #5:
R. Coyle, et al, "The Influence of Solder Void Location on BGA Thermal Fatigue Life", SMTAI Conference Proceedings [9]

Investigation Specifics:
- 680 I/O Plastic BGA, daisy chained, 35x35mm package, 1.0mm pitch, 0.635 (25 mil) diameter solderball
- SAC305 solder paste
- Test vehicle: 2.36mm (93 mil) thick, Isola 370HR laminate, 8 internal planes, OSP finish
- Thermal cycling: 0°C-100°C, 10 minute dwells, 10 minute ramps, 2900+ cycles

Investigation Conclusion:
- Overall void density on BGA component was not high
- Solder crack path typically found at solder joint / BGA package interface

- Planar (flat) metallographic cross-sectioning thru package/solder joint interface showed a high incidence of voiding not observed in orthogonal cross-section
- Solder voiding had a negative impact on solder joint reliability only when void density was high and void location was in the crack path (Figure 6)
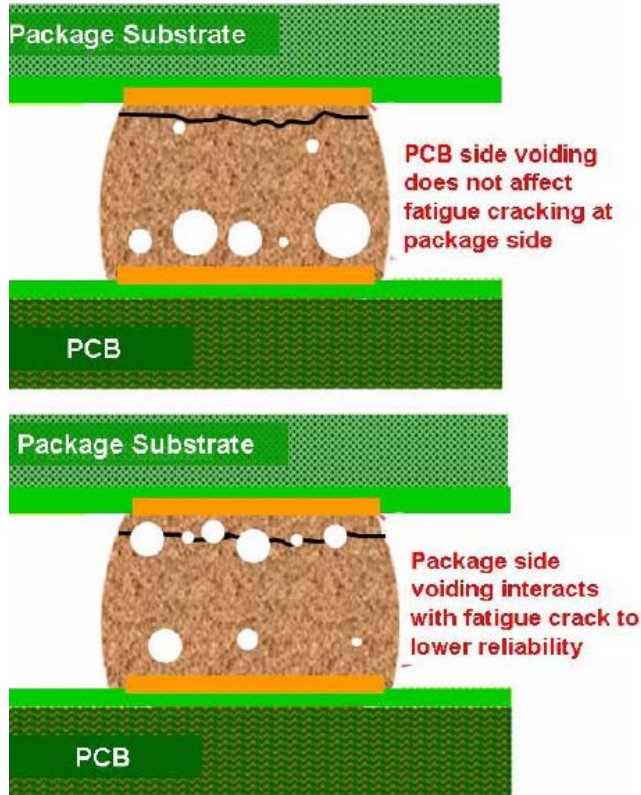
Figure 6. Impact of Voids on Solder Joint Integrity, D. Coyle et al [9]

The Coyle investigation found that macro voids reduce solder joint reliability by reducing the effective attachment area and that this geometric effect was independent of solder alloy composition. The study concluded that the dominant factor that impacts solder joint integrity was void location and not the void size or density of voids.

Study #6:
J. Smetana, et al, "The Effects of Non-filled Microvia in Pad on Pbfree Solder Joint Reliability of BGA and QFN Packages in Accelerated Thermal Cycling" [10]

Investigation Specifics:
- Various Ceramic and Plastic BGAs/CSPs, daisy chained, 0.3mm – 0.889mm (12 mil – 35 mil) diameter solder balls
- SAC305 solder paste
- Test vehicle: 3.17mm thick (125 mil), High Tg Phenolic FR-4, 6 internal planes, Immersion Silver finish
- Thermal cycling: 0°C-100°C, 10 minute dwells, 10 minute ramps, 4279 cycles

Investigation Conclusion:
- A total of 21 of 40 test vehicles had a void greater than 45% of solder ball diameter or 20% of ball area
- Solder crack path typically found at solder joint / BGA package interface
- Via in Pad (VIP) resulted in significantly more voids in BGA/CSP solder joints than no Via in Pad design
- The voiding percentage in area or diameter of the BGA solder joints did not correlate to the failure cycle in thermal cycling (Figure 7)
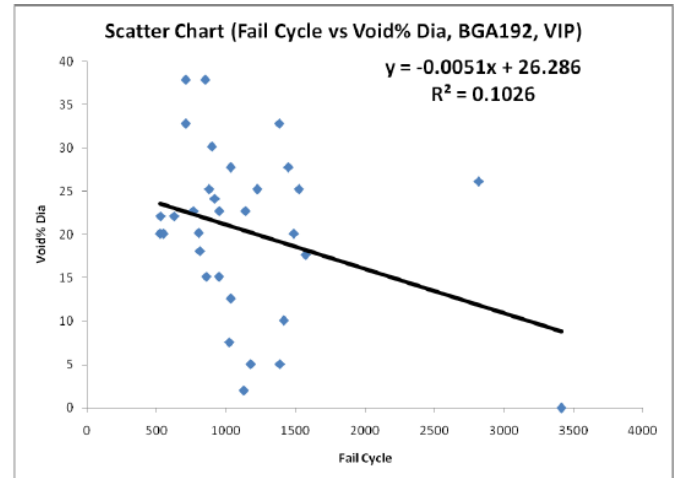
Figure 7. Scatter Chart Showing No Correlation between Solder Joint Void and Thermal Cycle Integrity, J. Smetana et al [10]

The Smetana investigation documented that for both a ceramic BGA component and a plastic CSP component, the void diameter or area percentage had no correlation to solder joint thermal cycle integrity. Cross-sectional analysis revealed numerous examples of thermal cycle fatigue cracking having no interaction with the solder joint void.

OBJECTIVES
The objectives of the investigation were: (1) determine if a correlation between solder joint void size/location and solder joint thermal cycle integrity existed for the thermal cycle range of -55°C to +125°C; (2) derive a BGA/CSP solder joint void criteria for submission to the IPC-JSTD-001 committee.

PROCEDURES
Test Components
Three different sizes of Ball Grid Arrays (BGAs) were selected for the test. The components, which were procured from Practical Components, were daisy chained to allow for electrical continuity monitoring during thermal cycle testing. The component sizes and pitches are listed in Table 2 together with the Practical Components part numbers.

Table 2. Components Characteristics

Part	Size	Pitch	Part Number
BGA56	6x6 mm	0.5 mm	A-CABGA56-.5mm-6mm-DC
BGA256	17x17 mm	0.8 mm	A-CABGA256-1.0mm-17mm-DC
BGA288	19x19 mm	1.0 mm	A-CABGA288-.8mm-19mm-DC

Test Vehicle

The test board was 2.18mm (86 mil) thick with 14 dummy inner layers. The board was constructed using FR-4 material in accordance with IPC-4101/126 with an electroless nickel/immersion gold (ENIG) surface finish. Figure 8 illustrates a completely assembled test vehicle without the ribbon cable used for monitoring current continuity. Micro-vias in accordance with IPC-6012 Class 3, Type 4 and IPC 2315 Type II were placed in the component pads to facilitate void generation in the solder joints. Table 3 lists the specific micro-via design data for each component on the test vehicle. Through-holes were arranged along one side of the test vehicle for ease of organizing cabling to the PWB. Instead of using a connector, ribbon cable leads were manually soldered to the through holes corresponding to each component I/O pair.
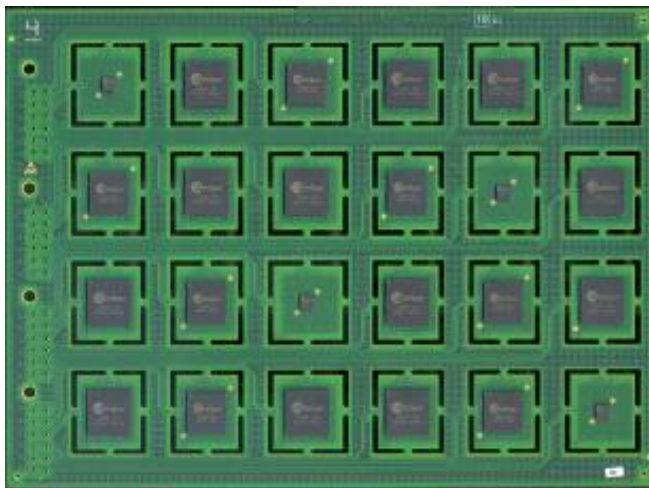
Figure 8. As-Assembled Test Vehicle

Table 3. Test Component Micro-via Design Data

	Package	Ball Pad	Pitch (mm)	Microvia	Concentric (Microvia and Pad)	Routing layer
U1	A_CABGA56__.5	0.010"	0.5	10_5	yes	2
U2	A_CABGA288_.8	0.012"	0.8	10_5	OFFSET	2
U3	A_CABGA256_1.0	0.015"	1.0	15_5	yes	2
U4	A_CABGA288_.8	0.014"	0.8	14_4 (5)	yes	2
U5	A_CABGA288_.8	0.012"	0.8	12_5	yes	2
U6	A_CABGA256_1.0	0.015"	1.0	none	N/A	1
U7	A_CABGA256_1.0	0.015"	1.0	15_5	yes	2
U8	A_CABGA288_.8	0.014"	0.8	14_4 (5)	yes	2
U9	A_CABGA288_.8	0.012"	0.8	12_5	yes	2
U10	A_CABGA256_1.0	0.015"	1.0	none	N/A	1
U11	A_CABGA56__.5	0.010"	0.5	10_5	yes	2
U12	A_CABGA288_.8	0.012"	0.8	10_5	OFFSET	2
U13	A_CABGA288_.8	0.012"	0.8	12_5	yes	2
U14	A_CABGA256_1.0	0.015"	1.0	none	N/A	1
U15	A_CABGA56__.5	0.010"	0.5	10_5	yes	2
U16	A_CABGA288_.8	0.012"	0.8	10_5	OFFSET	2
U17	A_CABGA256_1.0	0.015"	1.0	15_5	yes	2
U18	A_CABGA288_.8	0.014"	0.8	14_4 (5)	yes	2
U20	A_CABGA256_1.0	0.015"	1.0	15_5	yes	2
U19	A_CABGA288_.8	0.012"	0.8	10_5	OFFSET	2
U21	A_CABGA288_.8	0.014"	0.8	14_4 (5)	yes	2
U22	A_CABGA288_.8	0.012"	0.8	12_5	yes	2
U24	A_CABGA56__.5	0.010"	0.5	10_5	yes	2
U23	A_CABGA256_1.0	0.015"	1.0	none	N/A	1

Test Vehicle Assembly

The test vehicles were assembled at the Rockwell Collins Coralville production facility. An MPM Ultra Print 2000 automated stencil printer using a 0.005 inch thick stainless steel stencil applied solder paste to the test vehicles (Figure 9). The solder paste was Alpha tin/lead solder alloy WS-609. The components were placed using the Universal Advantis machine.

Figure 9. MPM Stencil Printer

The test vehicle was reflowed in a Heller 1912EXL Convection Reflow Oven. This oven had 14 temperature zones. The conveyor speed was 102 cm per minute with a standard air atmosphere environment. The oven used the high convection setting, and the boards were placed on the rails.

The test vehicles were allowed to air cool after reflow and then placed in the Electrovert Aquastorm 200 in-line cleaning system for removal of solder flux residues and other contaminants from the assembly. The in-line cleaner utilized 13.5% (by volume) Kyzen Aquanox 4625 saponifier in deionized water. The in-line cleaner is shown in Figure 10.


Figure 10. Electrovert Aquastorm In-line Cleaning System

X-ray Inspection of Test Vehicles

A critical element of the investigation was the assessment of the solder joint void size and location in the test components. The investigation used a significantly larger than normal test component population (85,920 individual solder joints) due to the random nature of void formation. The test vehicles were X-ray inspected for void size and location by Dr. David Bernard and Dr. Evstatin Krastev of Nordson Dage on the Nordson Dage XD7600NT100 X-ray inspection system before and after thermal cycling. Only those voids found in the BGAs that were above 25% of X-ray image area were chosen for further X-ray analysis. Once a void exceeded this threshold, the specific BGA containing the void was shown on the inspection system screen. The system software provides automatic definition of the gray scale level in the image to define the outline of all the BGA solder balls shown on the screen. The software also provides a measurement of the ball diameter by indicating the diameter of the longest axis of the defined ball area. This is achieved by automatically counting the number of pixels in the long axis. This measurement is calibrated against the primary system sample movement and is adjusted for the depth of the BGA in the sample (e.g. is it on side one or side two). In this regard, a suitable magnification must be selected for the imaging such that each BGA ball occupies a reasonable number of pixels in order to have a fair measurement. Once a ball diameter has been defined, the system can automatically determine the level of voiding within each defined BGA ball. A second gray level threshold is applied against which all pixels within each defined ball area are compared. If a pixel within the BGA ball is brighter than the threshold, it is defined to be a void pixel. The sum of the void pixels within the defined ball

area is then compared to the total ball area to determine the percentage level of voiding within each solder ball.

The range of solder voids recorded was from 0% - 35% of X-ray image area, with the majority of the population in the 1% - 10% range. A larger population of solder voids in the 25%-35% range would have been desirable but sufficient solder voids greater than the IPC-JSTD-001 specification of 25% were observed to make the investigation valid. Figure 11 (top) illustrates voids of 32% and 29% area on the inner rows of a test component. Additionally, the low voiding % of the other solder joints is visible. Figure 11 (bottom) shows an oblique view X-ray image of a BGA ball with 30% void. It also shows the interfaces of the solder joint as ellipses above and below the ball.
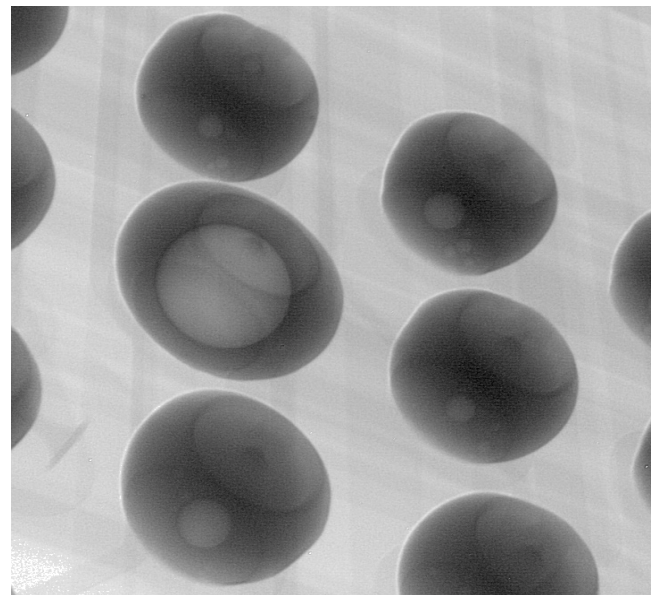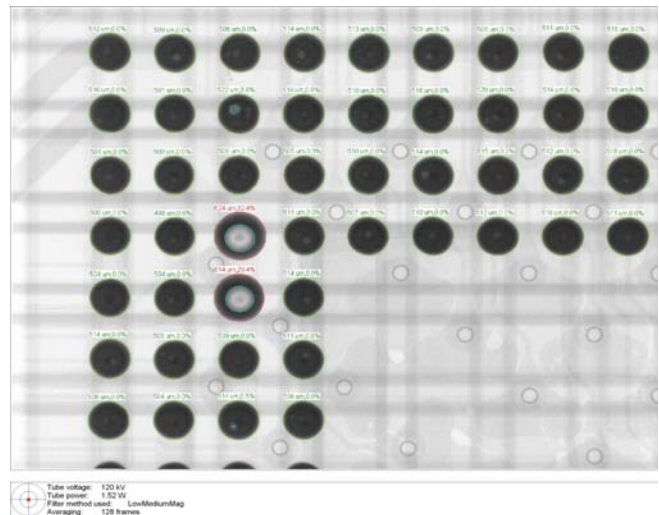
Figure 11. X-ray Examination of Test Vehicle Revealing: Top - Voids of 32% and 29% Area, Bottom - Oblique Angle X-ray View of 30% Void in BGA

THERMAL CYCLE TESTING

The temperature cycle range used in this study was -55°C to +125°C with a minimum 15 minute dwell at each temperature extreme and a maximum temperature ramp of 10°C/minute. Figure 12 shows the thermal cycling chamber along with the Anatech Event Detection system.

Figure 12. Thermal Cycling Chamber and Anatech

Figure 13 illustrates the thermal profile recorded using the Graphtec Midi Logger GL220 temperature acquisition unit.

Figure 13. Thermal Profile

The continuity of the components was continuously monitored throughout thermal cycle testing by an event detector in accordance with the IPC-9701 specification. Each component was treated as a single resistance channel. An "event" was recorded if the resistance of a channel exceeded 300 Ω for longer than 0.2 μsec within a 30-second period.

A failure was defined for a component when it:

- Exceeded the maximum resistance for 15 consecutive events; or

- Had five consecutive detection events and proceeded to record at least 15 events; or

- Became electrically open.

The Anatech keeps track of events in two ways. One format records individual events chronologically, giving the cycle number and temperature of the chamber at the time of the event. Once a solder joint recorded 15 events in this format the component was considered to be failed and the event detection system software excluded it from the remainder of the test (i.e. event data were not recorded for that component for the remainder of the test). The second data log format keeps track of the frequency of events after the first is recorded until the end of the test. This data can be used to determine whether a channel may have had 15 events in an isolated timeframe and then reconnected. In general, however, once a channel has met the criteria for a failure, even a low frequency of events afterwards will not redeem the solder joint and the failure remains on record. A total of 1150 thermal cycles were completed in the testing.

TEST RESULTS

Statistical Analysis

The solder joint thermal cycle integrity was statistically analyzed using regression analysis to determine the Weibull shape factor (β) and characteristic life (θ) for the failure data. The Weibull function relates the cumulative failure distribution, F(n), to the number of thermal cycles at which a failure occurred, n, as:

$$F(n) = 1 - \exp\left(-\frac{n}{\theta}\right)^{\beta}$$

The characteristic life in a Weibull distribution, θ, corresponds to the number of cycles at which 63.2% of the population is expected to have failed. This parameter is often referred to as "N63" and may be thought of as an indication of the approximate average life of the population. The shape factor (β) is often referred to as the Weibull slope and is a measure of how tightly grouped the failures are. The higher the shape factor, the more uniform the reliability across the population is; if all components fail at exactly the same point the shape factor would be infinity. A shape factor of less than 1.0 is generally considered to be indicative of infant mortality. Electronic components in thermal cycling that are undergoing 'post infant mortality' failures typically exhibit shape factors in the range of 4-8, depending on the particular packaging style.

The initial analysis of the data showed that the BGA56 data exhibited characteristics that would be typical of a failure population that contained two distinct failure modes. Figure 14 shows this behavior, in which a number of samples failed prior to 200 cycles, followed by the majority of the population surviving past 600 cycles. A mixed mode Weibull fit was calculated using the equation below. This

adds two separate Weibull functions, with one multiplied by p (the portion of the total population that fails due to the first failure mode) with the other multiplied by 1-p, i.e. the portion of the population that fails by the second failure mode. An iterative approach was used to calculate the Weibull coefficients and values of p that gave the best fit to the equation.

$$F(n) = p * \left[1 - \exp\left(-\frac{n}{\theta_1} \right)^{\beta_1} \right] + (1-p) * \left[1 - \exp\left(-\frac{n}{\theta_2} \right)^{\beta_2} \right]$$
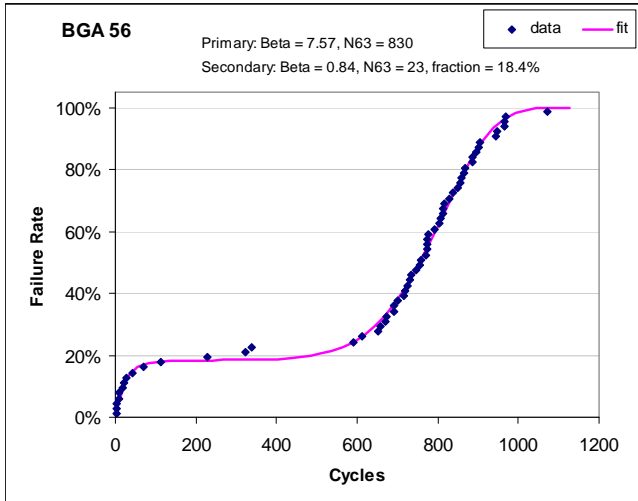
Figure 14. Mixed Mode Weibull Fit for BGA56 Data with Voids

The data for the assembly with typical voids (i.e. a void range of 1-10% of X-ray image area) similarly exhibited mixed-mode reliability characteristics. Upon further investigation, it was determined that in both data sets virtually all of the early failures occurred in the same component location on the test board (reference designator U1).

Figure 15 and Figure 16 clearly shows the significant difference in the reliability of the U1 components, which were located in one corner of the test board, compared to the other BGA56 components. This indicated that the secondary failure mechanism was due to an assembly process root cause and not related to the absence or presence of voids in the solder joints. Therefore, subsequent data analysis did not include the data for component reference designator U1.
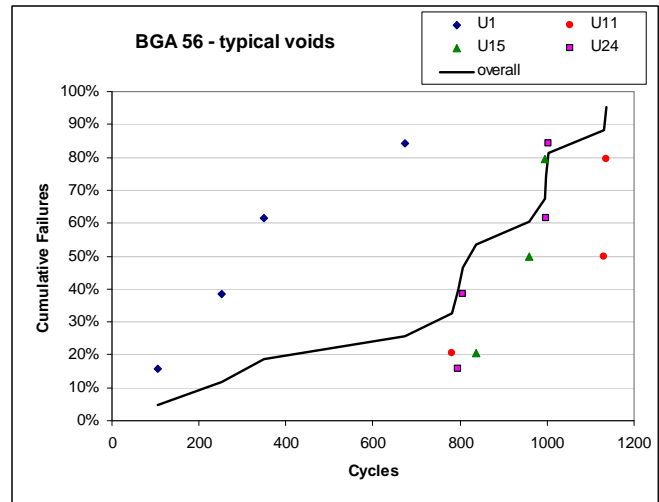
Figure 15: Failure Distributions for BGA56, by Reference Designator, With Typical Voids
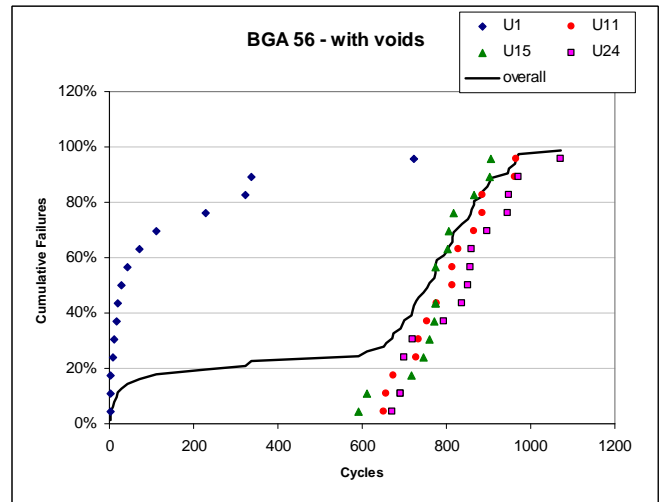
Figure 16. Failure Distributions for BGA56, by Reference Designator, With Voids

A similar reference designator level analysis was conducted for the BGA256 and BGA288 devices. The results of this analysis, for the samples with voids, are shown in Figure 17 and Figure 18. While these results do show that there was some variation among the individual reliability characteristics depending on the particular reference designator, other than U1 in the BGA56 data set, these differences do not appear to be statistically significant.
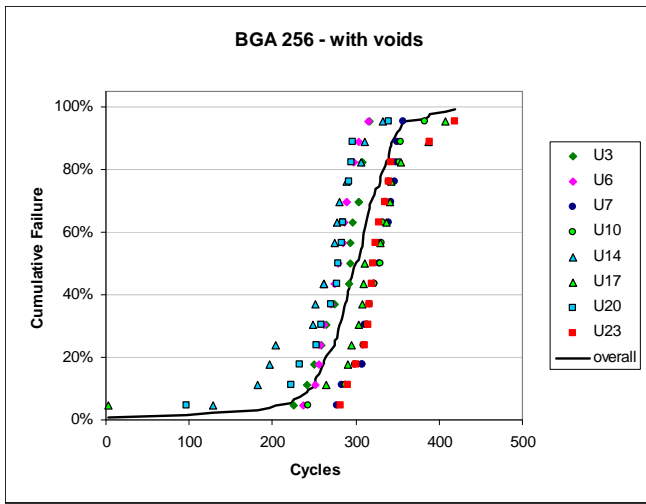
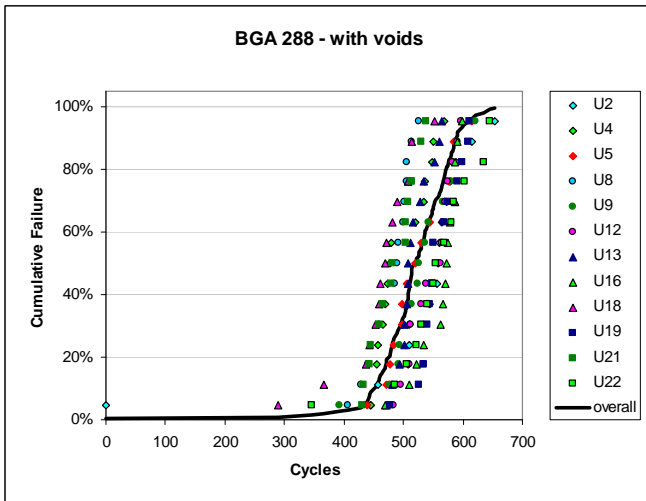**Figure 17.** Failure Distributions by Reference Designator

Figure 18. Failure Distributions by Reference Designator

For reference, the symbols and colors used in Figure 15 through Figure 18 were defined to help to identify any trends related to the location of a reference designator on the board. Symbols indicate which of the four horizontal rows on the test board that a particular reference designator occupied while the colors correspond to a column. The color/symbol combinations for the reference designator locations are shown Figure 19. There does not appear to be any distinct correlation between the reliability of the components and their location on the test board.

Figure 19. Reference Designator Location Key

The overall reliability data for the study, not including the data for U1, is shown in Figure 20. This clearly shows that the additional voids have relatively little impact to the overall reliability of the components. The Weibull coefficients calculated for all three components and for typical and voided conditions are shown in Table 4. This table also indicates the impact of the voids on the characteristic life calculated for each data set.
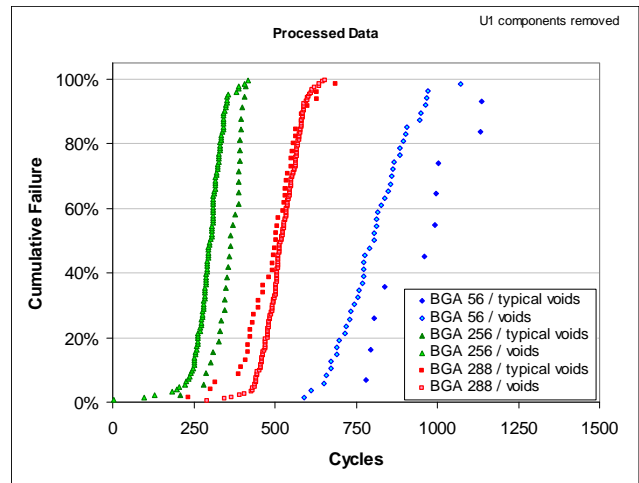

Figure 20. Component Reliability Results

Table 4. Calculated Weibull Coefficients

	BGA 56		BGA 256		BGA 288	
	typical	voids	typical	voids	typical	voids
ξ	6.68	8.39	10.66	8.71	7.08	10.57
N63	1002	840	378	314	527	544
ξ N63	16%		-16%		+3%	

Figure 21 compares the reliability curves for all samples of BGA 256 and BGA 288 components with voids greater than 20% to the rest of the samples tested. The similarity between the trend lines, and the calculated Weibull coefficients shown in Table 5, indicate that the samples with and without voids had the same reliability.
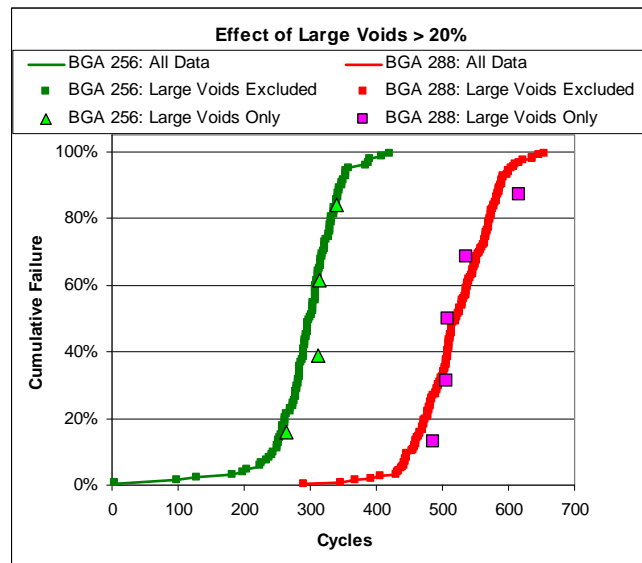


Figure 21. Effect of Large Voids Reliability Results

Table 5. Large Voids Calculated Weibull Coefficients

|	BGA256			BGA288		
	all data	w/o large voids	large voids only	all data	w/o large voids	large voids only
samples	120	116	4	179	174	5
Weibull slope	8.7	8.6	10.4	10.6	10.5	18.3
characteristic life	314	313	322	544	544	528

Physical Failure Analysis

Metallurgical cross-sectional analysis was conducted using the X-ray analysis as a guide. One of the goals of the cross-sectional analysis was to characterize void locations, sizes, failures and any indications of cracking/degradation.

Figure 22 (top image) illustrates two BGA corner/outer row solder joints that failed in the typical location at the component/solder joint interface. One of these solder joints (magnified lower image) has a void less than the 25% maximum requirement but did undergo a loss of solder joint integrity. Figure 23 (top image) illustrates two BGA corner/outer row solder joints that failed in the typical mode but with no voiding present.
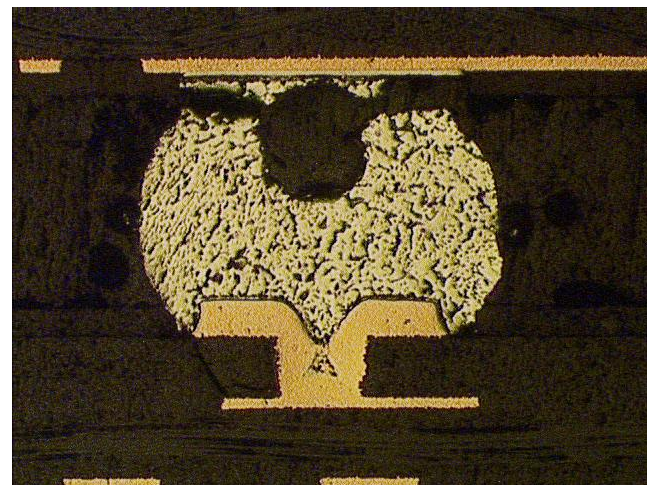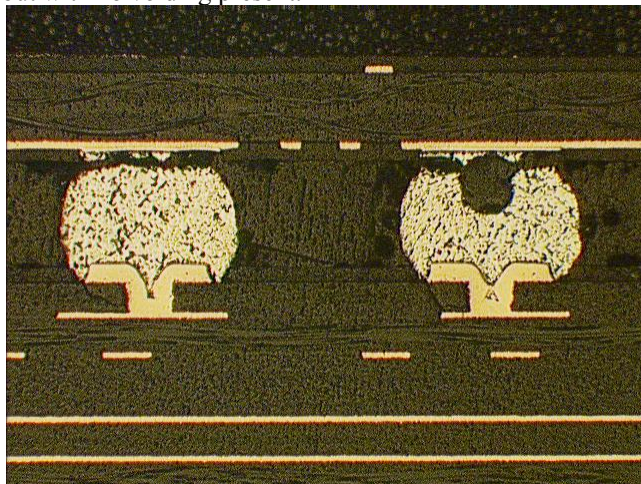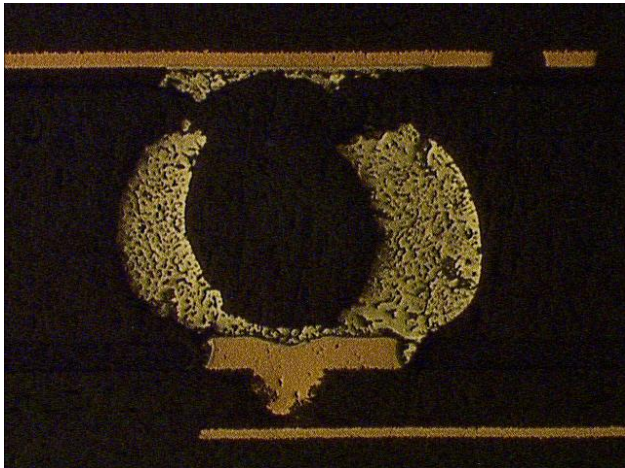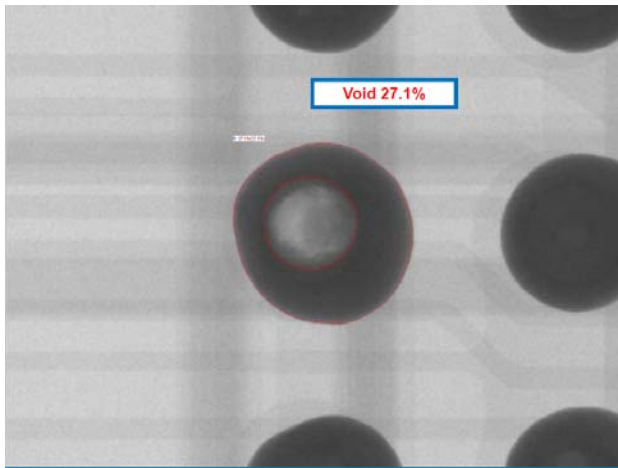

Figure 22. Macro (Top) and Magnified (Bottom) Views, BGA Void Assessment: 18% Void, Outer Row, 264 Cycles, BGA256
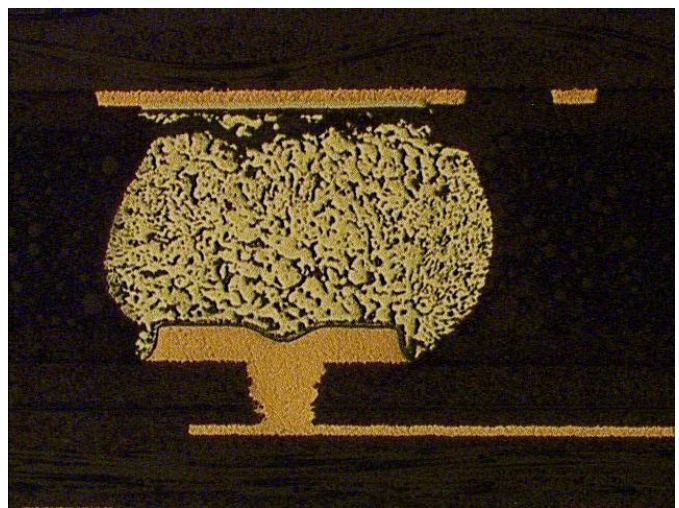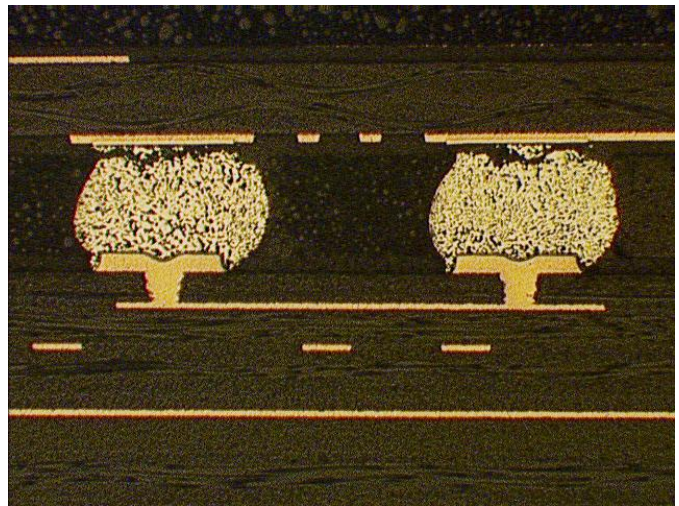

Figure 23. Macro (Top) and Magnified (Bottom) Views BGA Void Assessment: No Void, Outer Row, 311 Cycles, BGA256

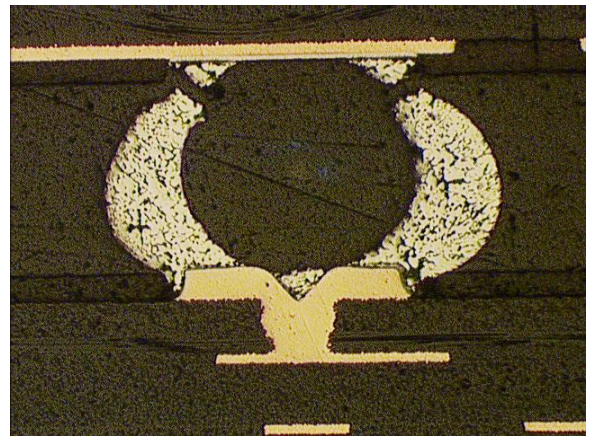Figure 24 illustrates a solder joint failure due to a 27.1% void that reduced the crack path length and resulted in a loss of solder joint integrity. This BGA solder joint was located on the outer row but not a corner location. Figure 25 and Figure 26 illustrate a solder joint failure due to a 31.3% void reducing the crack path length. This BGA solder joint was located on an inner row/ near package corner location.

Figure 24. X-ray (Top) and Cross Sectional (Bottom) Views BGA Void Assessment: 27.1%, Outer Row, 505 Cycles, BGA 288
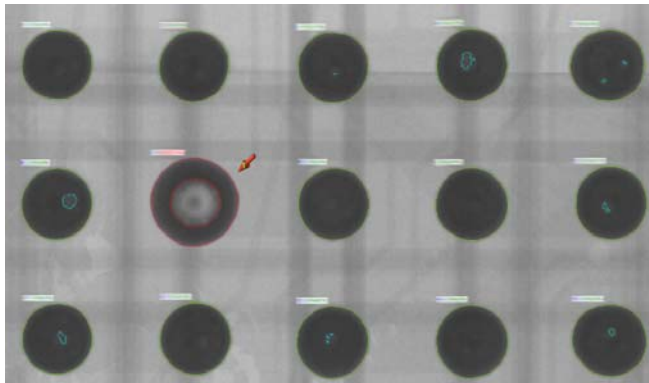

Figure 25. X-ray View, BGA Void Assessment: 31.3%, Inner Row/Corner, 311 Cycles, BGA256

Figure 26. Cross Sectional View, BGA Void Assessment: 31.3%, Inner Row/Corner, 311 Cycles, BGA256

Figure 27 illustrates a typical solder joint containing a 12% void in a BGA solder joint that did not fail the thermal cycling test. This BGA solder joint was located on the outer row but not a corner location. Figure 28 illustrates a typical solder joint containing a 17% void in a BGA inner row that did not fail.
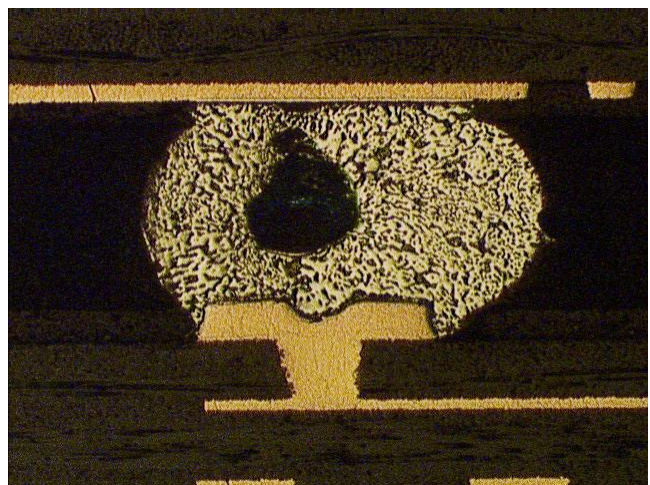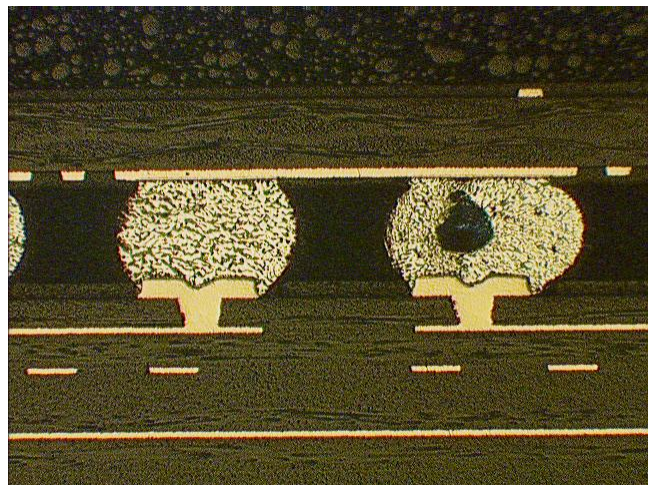
Figure 27. Macro (Top) and Magnified (Bottom) Views, BGA Void Assessment: 12%, Outer Row, No fail, BGA288
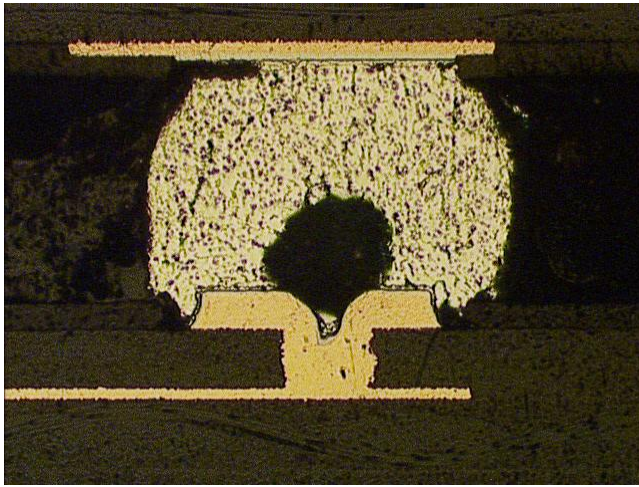
**Figure 28**. BGA Void Assessment: 17%, Inner Row, No fail, BGA256

Figure 14 showed that the Weibull analysis indicated the existence of two failure modes impacting the BGA56 component solder joint integrity results. Cross-sectional analysis was conducted on the U1 BGA56 component based on the analysis illustrated in Figure 16. The cross-sectional analysis revealed that insufficient solder paste transfer occurred at the U1 component location. The lack of solder paste resulted in the U1 component making an electrical connection with no solder joint structural integrity. The U1 component condition is not a valid solder joint configuration, which justifies its removal from the investigation data set for assignable cause. Figure 29 and Figure 30 illustrate the defective U1 component pad location. The solder joint has a pad impression where it made electrical contact before the thermal cycle induced stresses caused failure.
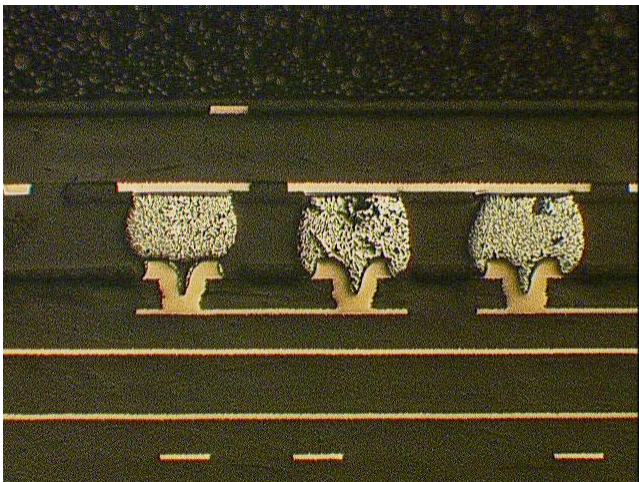
Figure 29. Macro View, BGA56 U1 Component Cross-section Showing Assembly Induced Solder Joint Defect, Failed @ 18 Cycles, BGA 56
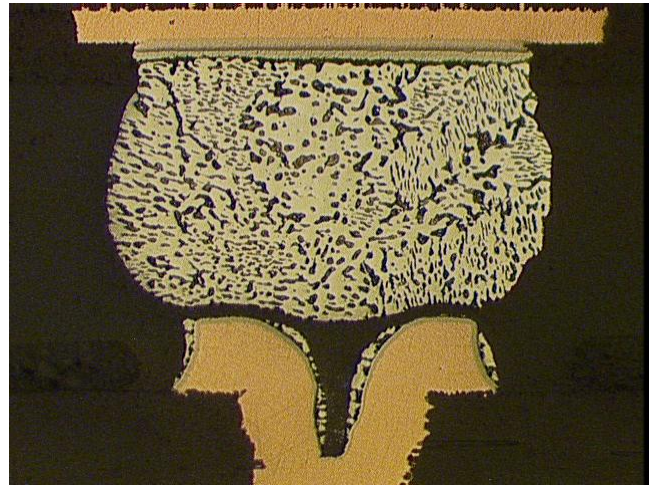
Figure 30. Magnified View, BGA56 U1 Component Cross-section Showing Assembly Induced Solder Joint Defect, Failed @ 18 Cycles, Defect Due to Stencil Paste Deposit Issue, BGA56

Computerized Tomography
The investigation utilized Computerized Tomography (CT) as an additional BGA failure analysis tool. CT or 'CAT scanning' is best known from the medical sphere for its diagnostic analysis capabilities by being able to image any 2D slice view through a volume. The same technique can be applied to the inspection of electronics. For electronic applications, it provides the ability to make continuous cross-sections through any plane within an object – all with the added advantage of not destroying the volume, as would be the case with a traditional cross-section. Of course, the resolution of the CT is not at the same level as that found in a scanning electron microscope (SEM) but the speed of making the CT model is measured in minutes compared with the hours that are usually necessary for traditional micro-section preparation.

For CT, a series of 2D X-ray images, or projections as they are known in the CT world, are taken of an object as it is rotated perpendicular to the X-ray beam axis (see Figure 31). The density variation data contained within each image is processed using software to create a three-dimensional density model of the object. This 3D model can then be viewed, manipulated and sectioned as required. In addition, reconstructed 2D X-ray slices ('virtual cross-sections') through any plane in the CT model can be produced.

There are three stages to producing and using a CT model. These are:
1. Image Acquisition
2. CT Model Reconstruction
3. Visualization / Analysis

The image acquisition stage of CT may well be the most time consuming phase of the process. It depends on the number of images taken during the sample rotation, as well as the averaging of each image that may be required to improve the signal to noise ratio. The more images that are

taken, the more information there is for the CT reconstruction.
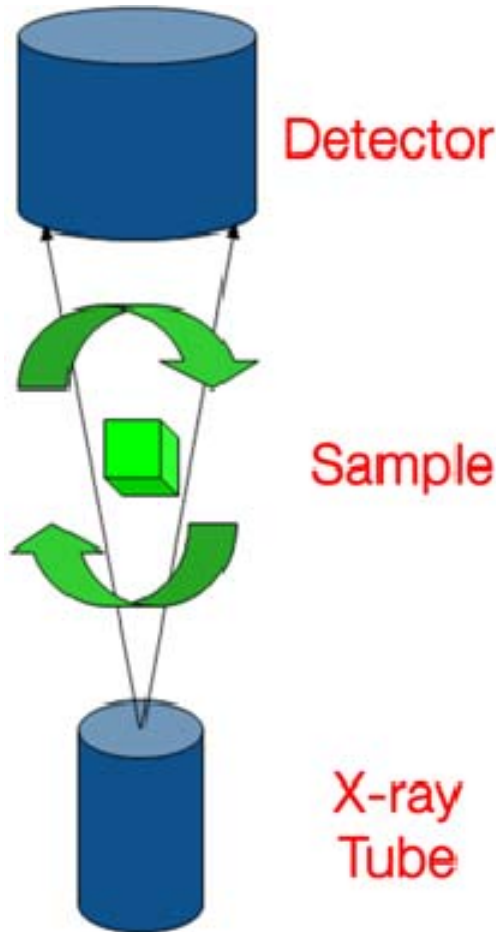
Figure 31. Schematic representation of the image acquisition phase of CT inspection

The need for more or less image averaging will depend on the type of detector that is being used. For example, an image intensifier has more noise in the image than would be seen with a flat panel detector, so a better CT model from an image intensifier will require more averaging than when using a flat panel detector.

Once the 2D images have been obtained, the reconstruction phase to produce the CT model can be undertaken. The most commonly used CT algorithm is called the Feldkamp cone beam reconstruction method. This is a filtered rear-projection technique. Whatever algorithm is chosen, the end result is a digital model that is a three-dimensional density map of the original object. The model is contained within a virtual cube that is made up of volume pixels, or voxels. The more voxels the model has, the better the detail that will be in the model. For example, a model made from 512 x 512 x 512 (or 512^3) voxels would have less detail than one made from 1024 x 1024 x 1024 (1024^3) voxels. However, a 1024^3 model has 8X the data within it compared to a 512^3 model and this fact impacts the calculation times required for the

reconstruction. Until very recently, the high cost and limited availability of major computational power to do these CT calculations made it necessary to limit the CT models to smaller values such that reconstruction times were manageable, or it was necessary to have custom hardware available to do the massive amount of processing required to generate the CT model from the many 2D images. However, the rapid development of PC gaming and its need for fast graphic processing now means high powered graphic processor unit (GPU) boards are readily, and cheaply available and these lend themselves directly to the mathematical processing required by the CT. As a result, larger CT models can now be processed in minutes compared to the hours that it would have taken only a few years ago. For the future, GPU technology will further improve CT, as different, possibly better, CT algorithms become computationally viable. Upon completion of the reconstruction, sample analysis can be conducted.

Dr. Evstatin Krastev conducted 3D CT assessment of the BGA voids using the Nordson Dage XD7600NT100 X-ray inspection system after the completion of the thermal cycle testing. The CT assessment allowed for a better understanding of the void location within the solder joints and the interaction of the failure crack path/void interface. The CT assessment results were in agreement with the cross-sectional analysis results indicating that the outer row of the BGA/CSP was most influenced by the void size and location. Figure 32 and Figure 33 illustrate a typical example of the CT assessment of a 26.1% BGA Void on an outer row that failed at 616 thermal cycles.

Figure 32 is a 2D X-ray image of the area of interest incorporating void calculations. The location of the voids within the joint is much better assessed using 3D CT virtual cross sectioning. Figure 33 (top) provides a 3D overview of the examined area and Figure 33 (bottom) represents a virtual cross section through the particular BGA row. Black areas represent voids/cracks. The location, size and shape of the voids can be precisely examined. The cracks resulting from the thermal cycling are also clearly visible. Once the CT model is compiled the failure analysis engineer uses dedicated software viewer to pan through each ball in slices as a continuous 'virtual cross-section' through the whole sample in order to evaluate the void size and location. The advantages here compared to mechanical cross-sectioning is that there are no limitations in the position of the virtual section plane, virtual sectioning is fully reversible (as it is done on a software model), and no additional mechanical defects are introduced.
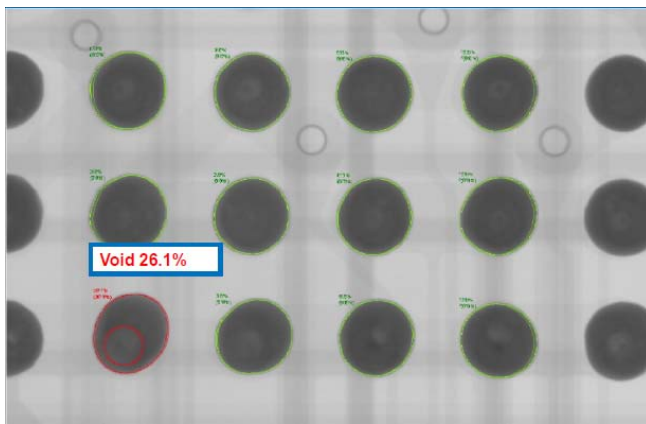
Figure 32. 26.1% BGA Voids Selected for CT Assessment
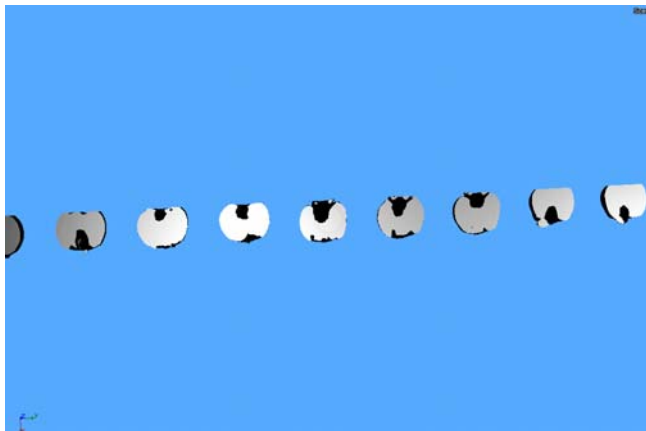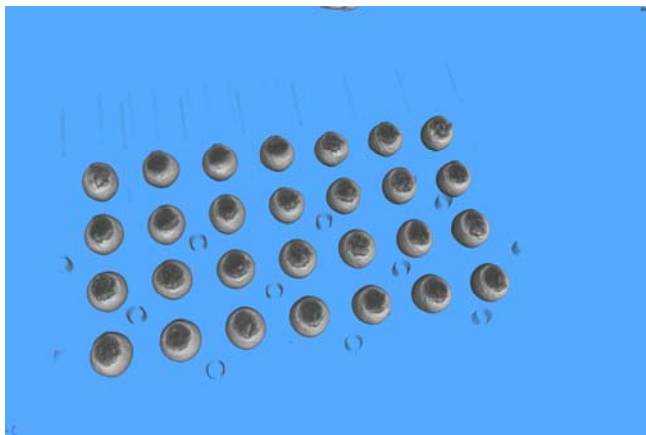
Figure 33. CT Assessment Image of 26.1% BGA Void. Top - CT overview of examined area, Bottom - CT Virtual cross section revealing voids and cracks represented by black areas.

DISCUSSION

The metallographic cross-sectional analysis results revealed that the BGA/CSP component was influenced by the void size and location. It is industry general knowledge [11, 12] that the outer row/corner solder ball locations of a BGA/CSP package are the maximum stress/strain locations (excluding component silicon die CTE effects). The metallographic analysis showed that when solder joints containing voids greater than 25% failed earlier than solder joints with voids less than 25%, it was primarily due to the location of voids in the crack path. This reduced the overall crack path length necessary for joint failure. Figure 22 and Figure 23 illustrate this observation with the void containing solder joint failing slightly earlier (i.e. within 50 cycles) than the non-void containing solder joint. Other examples found during the cross-sectional examination demonstrated that the simple existence of a void was not the controlling factor for the loss of solder joint integrity. The location of void relative to the solder joint failure crack path had a much larger impact than the presence of the void alone. This result is in agreement with both the Sethuraman [8] and Coyle [9] investigations. The results did indicate a more significant effect of large void size on the solder joint thermal cycle integrity than found in the Smetana [10], Sethuraman [8], SPVC [6] and Coyle [9] investigations. It is presumed that the more pronounced effects of large voids observed in this study were the result of the larger temperature excursion (-55°C to +125°C) used for cycling. This wider temperature range imposed larger stress/strain forces on the test components than the forces imposed by the small temperature ranges used in the other investigations and exacerbated the stress concentrations.

The investigation results are the statistical data basis from which real world "practical" solder joint requirements can be derived. These investigation results and the cited published literature results clearly demonstrate that voids have limited impact on the overall reliability of BGA and CSP components over a wide range of components tested and temperature cycle ranges. However, sound engineering practice and utilization of robust soldering processes to insure repeatability and reproducibility, will inherently lead to BGA/CSP solder joints with minimal voiding. Several industry studies [4, 13, 14] have shown that soldering processes using qualified solder paste materials and consistent process controls produce BGA/CSP solder joints that are nearly void free. When significant BGA/CSP voiding does occur, it is due to a pad design feature (i.e. via in pad) [4, 10] or an improper soldering process [2, 14]. It is a reasonable expectation that the electronics industry have a set of BGA/CSP void criteria. It should be noted however that the primary objective of the void criteria is not to verify component integrity, but rather to establish soldering process control.

PROPOSED BGA/CSP SOLDER JOINT VOID REQUIREMENTS

The following BGA/CSP solder joint void requirements are proposed for the IPC-JSTD-001 specification:

- BGA/CSP voids in the 0%-20% of the ball X-ray image area require no action

- BGA/CSP voids in the 20%-25% of the ball X-ray image area should be treated as a process indicator initiating a process root cause analysis

- BGA/CSP voids greater than 25% of the ball X-ray image area in the outer row of the component are not acceptable

- BGA/CSP voids greater than 35% of the ball X-ray image area are not acceptable

- Continue to utilize the following Notes listed in IPC-JSTD-001:

  (1) Design induced voids, e.g. microvia in land, are excluded from this criteria. In such cases acceptance criteria will need to be established between the manufacturer and user.

  (2) Manufacturers may use test or analysis to develop alternative acceptance criteria for voiding that considers the end use environment.

CONCLUSION

The investigation results show:
- The location of the void within the solder joint was the primary root cause for the loss of solder joint integrity.

ACKNOWLEDGEMENTS

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