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Influence of Plating Quality on Reliability of Microvias

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Abstract
Advances in miniaturized electronic devices have led to the evolution of microvias in high density interconnect (HDI) circuit boards from single-level to stacked structures that intersect multiple HDI layers. Stacked microvias are usually filled with electroplated copper. Challenges for fabricating reliable microvias include creating strong interface between the base of the microvia and the target pad, and generating no voids in the electrodeposited copper structures. Interface delamination is the most common microvia failure due to inferior quality of electroless copper, while microvia fatigue life can be reduced by over 90% as a result of large voids, according to the authors' finite element analysis and fatigue life prediction. This paper addresses the influence of voids on reliability of microvias, as well as the interface delamination issue.

In a prior study, the authors investigated stress levels of copper-filled microvias with spherical voids of different sizes. Besides void size, void shape and microvia aspect ratio also affect the stress levels, and hence reliability of voided microvias. In this paper, stacked microvias with different void shapes and aspect ratios were modeled using finite element method. Stress distributions of these microvia models under cyclic thermal loading were examined to determine the effects of the voids on the reliability of microvias at different circumstances. The finite element modeling results demonstrated that conical voids resulted in higher stress levels in microvias than spherical voids of the same size. For the same void shape, larger voids increased the stress level, except for very small spherical voids which reduced the maximum stress in the microvias.

To study the delamination issue, the very thin layer of electroless copper was simulated between the base of the microvia and the target pad. It is assumed that the delamination was due to fracture within the electroless copper layer. The fracture toughness parameter in terms of stress intensity factor was calculated under different initial crack length and thermal loading conditions to characterize the likelihood of the delamination.

1. Introduction

High density interconnects (HDIs) have been widely used, due to increases in component performance and lead density, as well as reductions in package size. HDI circuit boards experienced the highest growth rate among all PCB product types in North American in 2013 [1]. Microvias are used as interconnects between conductor layers to accommodate the high I/O density in HDI boards. According to the IPC standards [2][3], microvias are blind or buried vias with a diameter equal to or less than 150 μm. Figure 1 is a schematic diagram of a single level microvia.

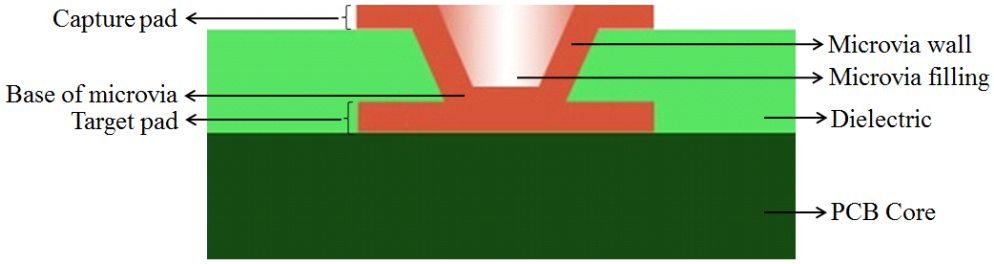

Figure 1 Diagram of a single level microvia

Advances of miniaturized electronic devices have led to the evolution of microvias from single-level to stacked structures that intersect multiple HDI layers. Stacked multi-level microvias are usually filled with electroplated copper to make electrical interconnections and support the outer level(s) of the microvia or components mounted to the upper capture pad. Figure 2 shows a schematic diagram of a [2+4+2]-layer HDI board (2 HDI layers on each side of the board, and 4 layers of traditional PCB core board in the middle) with stacked and staggered microvias.

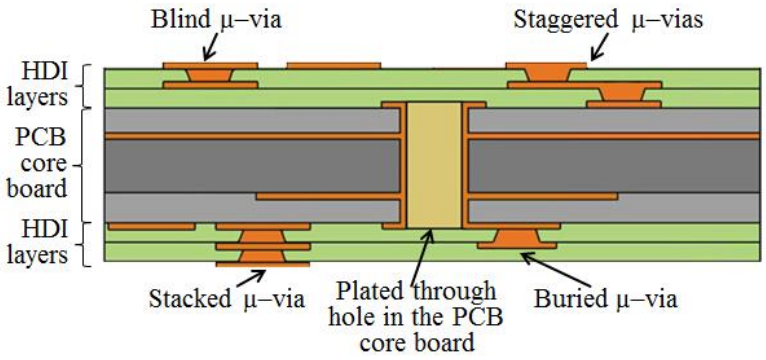

Figure 2 Illustration of an HDI Board with Various Microvias [4]

Reliability of Microvia has been a concern since microvias were first introduced to the electronics industry. During the assembly process and field usage, thermo-mechanical stresses are exerted on microvias due to coefficient of thermal expansion (CTE) mismatch between the dielectric material and the copper deposition in the microvia structure. The most commonly observed microvia failure is delamination between the base of the microvia and the capture pad [5][6]. There is a very thin layer of electroless copper (about 1-2 µm thickness) between the microvia base and the capture pad from the plating process. Incomplete cleaning of residues from laser drilling, surface roughness of the capture pad, and the brittleness of the electroless copper are blamed to be causes of the delamination [5]-[7]. Another reliability challenge in copper-filled microvias is that voids can be generated from the plating process. Figure 3 shows examples of microvias with voids of different shapes. Voids potentially degrade the reliability of microvias.

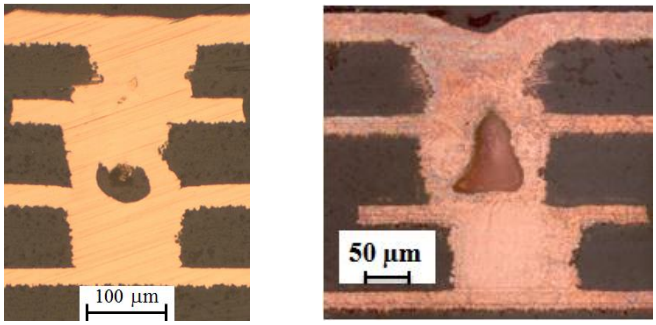

Figure 3 Examples of Microvia with Voids (Cross-Section) [4]

Microvia reliability research has focused on go / no-go type of experimental testing. Researchers tested single-level unfilled or epoxy-filled microvias [5],[8]-[13], as well as stacked multi-level microvia filled with copper [14] using thermal shock, interconnect stress test (IST), as well as reflow oven testing. However, they usually only recorded if the test coupons passed or failed at a specific testing cycle, and there was lack of statistical results about cycles to failure of the microvia structures. Birch **Error! Reference source not found.**[6] tested stacked microvias using IST, and conducted Weibull analysis on the test data. His results showed that single- and 2-level stacked microvias last longer than 3- and 4-level microvias (e. g. 2-level stacked microvias experienced about 20 times more cycles to failure than 4-level stacked microvias). However, none of the previous research on reliability testing addressed how microvias fail in the delamination process, or the effect of voids on the reliability of microvias.

Researchers have also developed numerical models using finite element method (FEM) to obtain local stress/strain states in the microvia structure, and employed analytical models to estimate the microvia fatigue life [11][12][15][16]. Prabhu *et al*. [15] investigated the effect of accelerated temperature cycling and thermal shock on the fatigue life of microvias. Ogunjimi *et al*. [16] found that the strain concentration factor, copper ductility, and microvia wall thickness had more significant effects on microvia reliability than the wall angle and epoxy height. Authors of [11][12] investigated the effects of geometry and material properties on microvia reliability using FEA. Wang and Lai [17] investigated the potential failure sites of microvias using submodeling technique in FEA. They found that copper filled microvias usually had a lower stress level than unfilled microvias. These FEA studies focused on single-level flaw-free microvias – none of the papers modeled stacked microvias, nor did they address the effect of voiding on reliability of copper-filled microvias.

Wang et al. [18] estimated the fatigue life of single-level unfilled microvias with a component assembled to it. In their work, the originally unfilled microvia barrel was either fully filled with solder or remained completely hollow after assembling the component. They found that the hollow microvias had a shorter fatigue life than the fully solder filled microvias by up to

35%. Wang et al. again focused on single-level defect-free microvias. Their model of hollow microvias after assembly is similar to a microvia with a void, but the authors did not consider effects of different voiding conditions (e.g. different void shapes, sizes, and voided microvias with different microvia aspect ratios).

Moreover, none of the researches modeled the electroless copper layer between the base of the microvia and the target pad, but considered all the copper were electrodeposited in the microvia structure for simplification. The microvia delamination issue was never studied with numerical modeling in the literature.

In a prior study [4], the authors investigated stress levels of copper-filled microvias with spherical voids of different sizes. In this study, the authors compared the maximum von Mises stress of microvias with spherical and conical voids of the same sizes, as well as voided microvias of different aspect ratios. The effect of electrolytic copper plating quality was investigated in terms of the maximum stress in microvias under cyclic thermal loading. Moreover, to study the effect of electroless copper plating, the authors modeled the very thin electroless copper layer to investigate the delamination issue between the base of the microvia and the target pad. The likelihood of the delamination was characterized by the stress intensity factor of the electroless copper.

Section 2 of the paper describes the FEA modeling process for voiding effects. Section 3 discusses the simulation results of effects of voids on microvia reliability. Section 4 addresses the delamination modeling and results. Section 5 concludes the papers and presents future work for the delamination study.

2. Finite Element Modeling for Voiding Effects

To investigate the effects of voids on reliability of microvias, FEA was conducted to examine the maximum von Mises stress of microvias with different voiding conditions under cyclic thermal loading. The accumulation of the stress / strain from each loading cycle will finally result in fatigue failure of the microvia structure. The finite element modeling process is discussed in this section.

The in-plane dimensions of a PCB are many orders of magnitude larger than the height of a microvia. Therefore, an acceptable approximate model is to isolate an appropriate "unit cell" containing only one microvia structure [19]-[21]. Assuming microvias are periodically arranged in a PCB with equal distance between two neighboring microvias in a row or column, suitable "periodic" boundary conditions [19]-[21] can be imposed on the unit cell to simulate the presence of the surrounding microvias and board materials. The unit cell extends half-way to the neighboring microvias in the same row or column in the periodic arrangement (Figure 4). The periodic boundary conditions were applied to the unit cell model to simulate the effect of neighboring microvias on it [4].

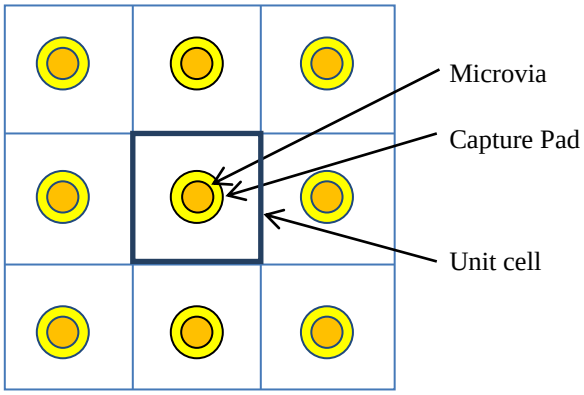

Figure 4 - Illustration of a Unit Cell [4]

The geometric dimensions of the microvia models are listed in

Table 1. Firstly, microvias of aspect ratio (dielectric thickness / microvia diameter) of 0.5 were modeled with spherical and conical voids of different sizes. The effects of void size and shape were examined. Then, microvias of different aspect ratios, 0.25, 0.5, and 0.75, with the same void volume ratio was compared to investigate the effects of aspect ratio on reliability of voided microvias. The models simulated a [2+4+2]-layer HDI board. The stacked two-level microvia was located in the most outside dielectric layers of the board. The top half of the HDI board was modeled due to symmetry about the board mid-plane. A 3D model was created for the unit cell, and a quarter model was used due to symmetry. Figure 5 shows the stacked microvia models with no void.

Table 1 - Geometric Dimensions of the Microvia Models

	Location	Dimension (μm)		
		AR = 0.5	AR = 0.25	AR = 0.75
Thickness	1st copper layer	28	28	28
	1st dielectric layer	75	37.5	112.5
	2nd copper layer	18	18	18
	2nd dielectric layer	75	37.5	112.5
	3rd copper layer	18	18	18
	3rd dielectric layer	75	75	75
	4th copper layer	12	12	12
	middle dielectric layer	100	100	100
Microvia diameter	top	150	150	150
	bottom	120	135	105
Microvia capture/target pad diameter		300	300	300
Distance between two neighboring microvias		800	800	800

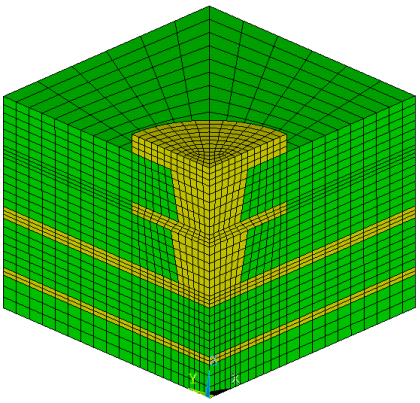

Figure 5 Finite Element Model of the Microvia

Table 2 lists the material properties used for the FEA models. The fabric reinforced composite, which most PCBs are constructed from, is used for the dielectric materials in the core board and the HDI layers. The woven-fabric reinforced resin is an orthotropic material with two principal material directions running along the board plane and orthogonal to each other, and a third direction along the out-of-plane normal. The reinforced resin was modeled as an elastic material [22]. Copper is used for the conductor layers and fills the microvias. The electroplated copper of the microvias was modeled as an elastic-plastic material having a bilinear kinematic hardening relationship [12]. For simplification, the very thin electroless copper layer was not simulated in the FEA models for the fatigue analysis; all the copper material in the microvia structures was considered as electroplated copper.

Table 2 - Material Properties

Material		CTE (ppm/°C)	Young's Modulus (GPa)	Poisson's Ratio	Shear Modulus (GPa)
FR4 (Transverse isotropic)	X-axis/YZ plane	16	17	0. 42	2. 4
	Y-axis/XZ plane	16	17	0. 42	2. 4
	Z-axis/XY plane	50	7. 45	0. 13	3
Copper (Isotropic)		17	103. 42	0. 34	
		Yield strength (MPa)		**Hardening Modulus (MPa)**	

	172. 3	1034. 2

Note: the PCB plane is the XY plane and the PCB thickness direction is the Z-axis

The thermal load simulated on the finite element models was temperature cycling from -55ºC to +125ºC, with 5-minute ramp times between the extreme temperatures and 10-minute dwell times at the high or low temperatures. Under the thermal loading, the microvia experiences cyclic tensile and compressive stresses. These stresses and corresponding strains are due to CTE mismatch between the dielectric material and copper, and the geometry of the microvia (including voiding geometry). At +125ºC, the CTE mismatch reaches the maximum and consequently, the thermos-mechanical stress in the microvias is the maximum. In this study, von Mises stresses at the highest temperature were monitored to examine the effects of voiding.

3. Simulation Results – Effects of Voids on Microvia Reliability

To investigate the influence of electrolytic plating quality on reliability of microvias, conical and spherical voids of different sizes were compared to understand the void shape effect; voided microvia of different aspect ratios were simulated, and the stress levels were correlated with the aspect ratio.

3.1 Void size and shape effects

Volume ratio was used to measure the void size in this study. Volume ratio was defined as the ratio of the void volume to the microvia volume. Both spherical and conical voids were observed from commercial HDI boards. Spherical voids of different size were simulated in [4]. The von Mises stress first declined and then rose as the void size increased. The existence of the minimum stress level around 12% void indicated the possibility of a beneficial void size with respect to the stress level, and potentially the reliability, of the microvia.

Conical voids of different sizes were modeled in this study. As shown in Figure 6, all the microvias with a conical void had higher maximum stress than the non-voided microvia. The stress increased as the conical void size increased. The stress of the microvia with 20% void was about 60% higher than the non-voided microvias. By comparing the conical voids and spherical voids, it was observed that a conical void always led to a higher stress level than the spherical void of the same size. For example, the microvia with 20% conical void had a 37% higher stress than the microvia with 20% spherical void.

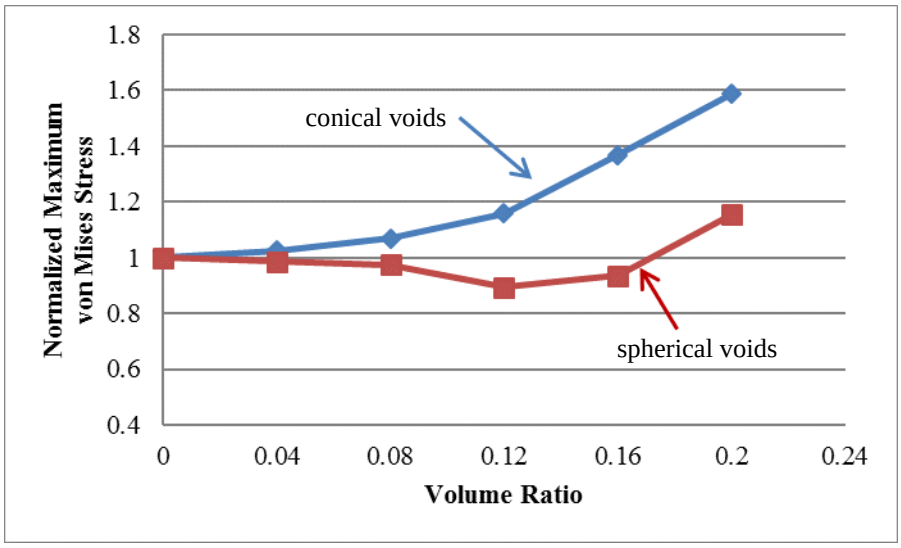

Figure 6 Effects of Voiding Shape on von Mises Stress

3.2 Microvia aspect ratio effects

For the same void shape (conical) and volume ratio (16%), microvias of different aspect ratios were simulated. The diameters of the microvias were unchanged, and different aspect ratios were achieved by altering the dielectric thickness (the height of the microvias).

As shown in Figure 7, the larger the aspect ratio, the higher the stress level in the voided microvia. The microvia of aspect ratio of 0.5 had 107% higher stress level than that of the microvia of aspect ratio of 0.25; the microvia of aspect ratio of 0.75 had 17% higher stress level than that of the microvia of aspect ratio of 0.5. Interestingly, the voided microvia (16% volume ratio) of aspect ratio of 0.25 had a lower stress level than the non-voided microvia of aspect ratio of 0.5 (34% lower). Therefore, it is not proper to simply provide a void size criterion for voided microvias acceptance / rejection without considering the microvia aspect ratio and void shape.

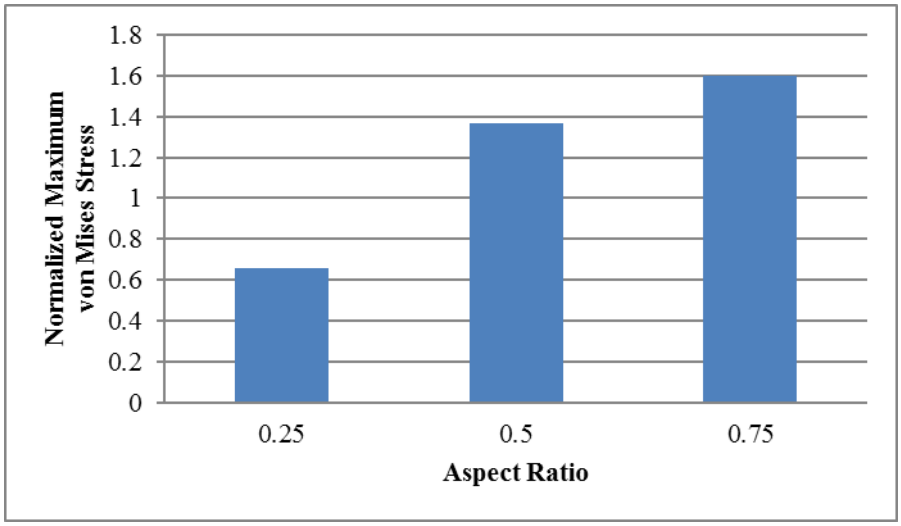

Figure 7 Voided Microvias with Different Aspect Ratio

4. Finite Element Modeling for Delamination

In the delamination between the base of the microvia and the target pad, the separation may occur between the interface of the microvia base (electrolytic copper) and the electroless copper, the interface of the electroless copper and the target pad (electrolytic copper), or within the electroless copper. Lesniewski [23] observed that the separation was within the electroless copper layer from the testing samples. As the first study to numerically investigate the microvia delamination issue, this paper assumes that the delamination is due to fracture within the electroless copper layer. Fracture analysis using FEA was conducted to calculate the fracture mechanics parameter in the electroless copper layer.

In the fracture analysis, an initial crack is present, simulating a material defect. The fracture mechanics parameters, such as stress intensity factor or energy release rate are usually used to characterize fracture. In this study, the authors calculated the stress intensity factor, K at the crack tip using 2D FEA. The crack growth occurs when the stress intensity factor reaches a critical value, that is,

$$K = K_C \tag{1}$$

where K_C is called fracture toughness, a material constant [24].

4.1 2D finite element modeling

To model the microvia structure using a 2D geometry, a cylindrical unit cell was isolated from the HDI board (Figure 8). In this case, the 2D axial section can be used for the microvia model due to axisymmetry. Periodical boundary conditions were applied on the outer cylindrical boundary of the unit cell.

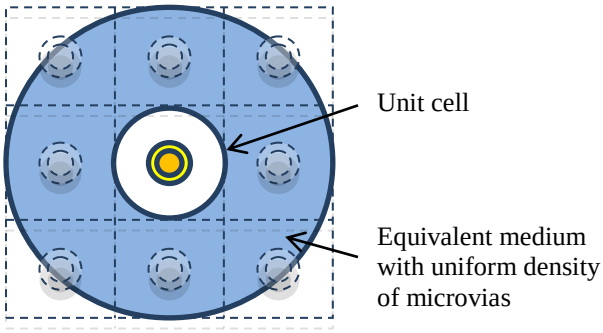

Figure 8 Cylindrical Unit Cell

Half of the axial section of the unit cell was modeled due to symmetry. The 2D model is shown in Figure 9. According to the fatigue modeling from Section 3 and 4, the stress concentration in the microvia structure occurred at the corner of the microvia base and the target pad in the lower microvia level. Therefore, the electroless copper in the lower microvia level was the potential site for microvia delamination. Consequently, only the electroless copper layer in the lower microvia level was simulated in the finite element model, and the other part of the microvia was simplified as electrolytic copper.

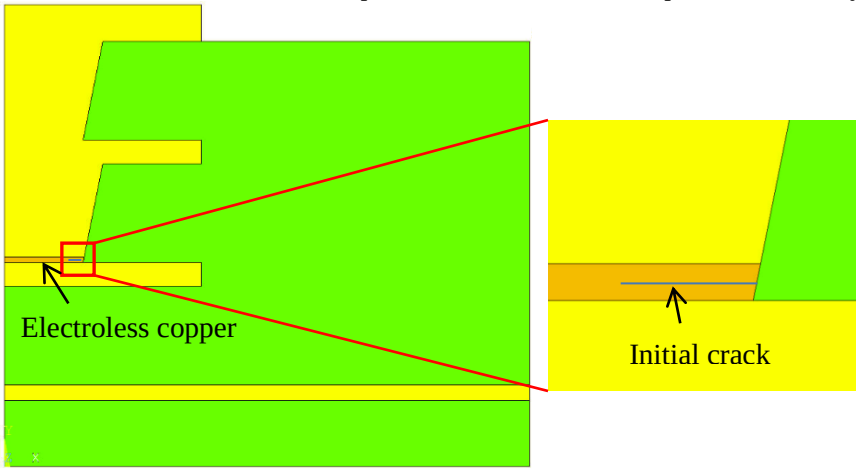

Figure 9 2D Axisymmetric Model

The same material properties for the electrolytic copper and dielectric material were used in the delamination modeling as in the fatigue modeling for voiding effects. The properties of the electroless copper are listed in Table 3.

Table 3 Material Properties of Electroless Copper

Material	CTE (ppm/^{o}C)	Young's Modulus (GPa)	Poisson's Ratio
Copper (Isotropic)	17	119	0. 34

Figure 10 shows the meshing result of the axisymmetric model. The meshing on the electroless copper is much finer than that on the other part of the model.

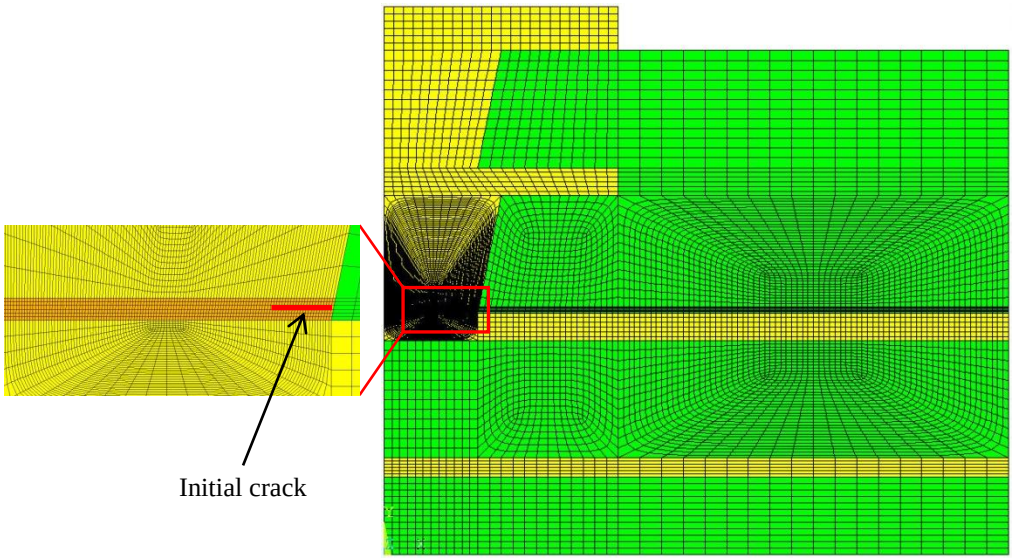

Figure 10 Meshing Result of the Axisymmetric Model

To understand the likelihood of fracture, different loading conditions and initial crack lengths were simulated. The loading conditions were monotonic thermal loading, 25ºC – 125ºC and 25ºC – 260ºC, which simulated the accelerated testing and solder reflow conditions, respectively. The initial crack length was also varied in the simulation to examine its effect to the stress intensity factor.

4.2 Results of stress intensity factor

The stress intensity factor predicts the likelihood of fracture. When the value of the stress intensity factor, K exceeds the critical stress intensity factor, K_C , the initial crack will grow and the fracture / separation will finally occur. Depending on the relative movement of the two surfaces of the crack, there are three fracture models – Mode I, opening or tensile mode; Mode II, shearing or sliding mode; Mode III, tearing or out of plane mode. The 2D axisymmetric model is used for plane strain cases, and therefore, the Mode III stress intensity factor was assumed to be zero in this study. The other two intensity factors were calculated using FEA. The Mode I stress intensity factor is shown in Figure 11, and the Mode II stress intensity factor in Figure 12 for different loading temperatures and initial crack lengths.

For both Mode I and Mode II stress intensity factors, the higher the loading temperature, the larger the stress intensity factor for the same initial crack length. This means that a higher temperature results in a higher likelihood of fracture in the electroless copper layer. Therefore, the solder reflow is a more severe condition for microvia delamination. The Mode I stress intensity factor decreased with the increase of the initial crack length for both thermal loading conditions. This result revealed that the shorter the initial crack, the more difficult for the crack to grow. However, the Mode II stress intensity factor was much less sensitive to the initial crack length. Moreover, there was no monotonic trend for the Mode II stress intensity factor with the change of the initial crack length, which was probably due to the complex geometry of the microvia structure and material constitution. Further, in the case that the critical stress intensity factor is known for the electroless copper in the microvias, the crack growth can be predicted.

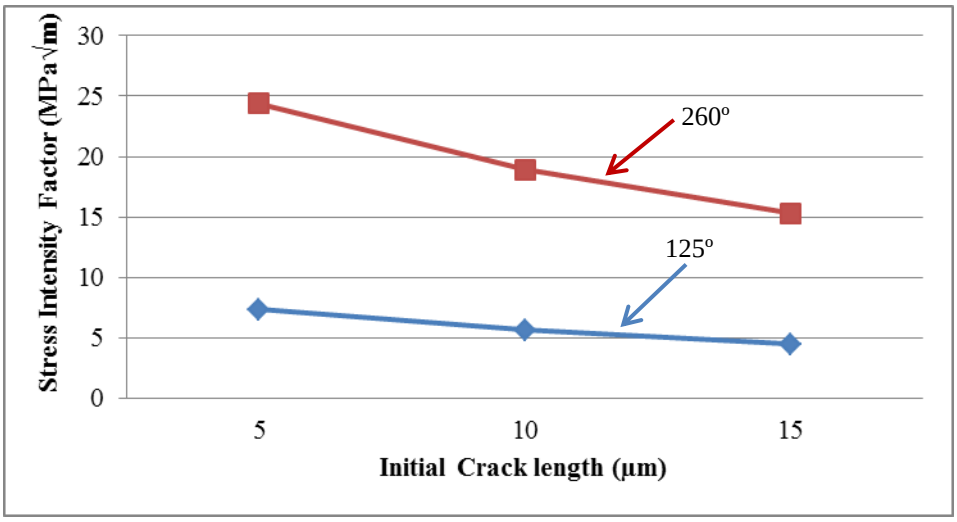

Figure 11 Mode I Stress Intensity Factor

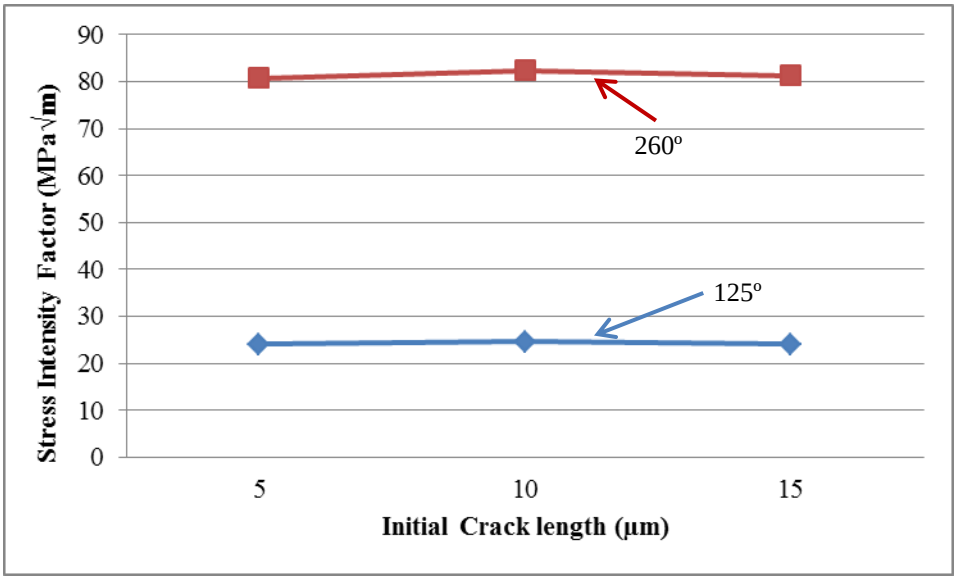

Figure 12 Mode II Stress Intensity Factor

5. Discussions and Conclusions

The effects of electrolytic plating and electroless copper quality on microvia reliability were investigated using finite element simulation in this paper. FEA studies addressed two failure mechanisms in HDI circuit boards – fatigue failure at the microvia barrel and delamination between the microvia base and target pad.

Considering the fatigue analysis for voiding effects, FEA studies were conducted to assess the influence of void shape and microvia aspect ratio on the stress distribution of voided microvias. All the microvias with a conical void had a higher stress then the non-voided microvia, and the stress level increased monotonically with the void size. The void boundary of the conical voids was non-uniform, and there was local stress concentration when the radius of curvature changed. As a result, the stress of the microvia with a conical void was always higher than the microvia with a spherical void of the same size.

Different void shapes and sizes also resulted in different locations of maximum stress, which are the potential failure sites. For the non-voided microvia, the site of maximum von Mises stress was at the corner of the target pad and the microvia base. For microvias with conical voids, the maximum von Mises stress was located at the void boundary due to local stress concentration. For microvias with spherical voids, when the voids was 16% volume ratio or smaller, the site of maximum damage was the same as the non-voided microvia; the major effect of the void was the change of the compliance of the microvia structure, which resulted in a decrease in the maximum von Mises stress. When the void reached 20%, the thin microvia well between the void boundary and the outside edge of the microvia generated local stress concentration, and the maximum von Mises stress (higher than the non-voided microvia) was located on the void boundary.

Microvia aspect ratio had a great impact on reliability of voided microvias. The larger the aspect ratio, the higher the stress level. Particularly, the stress of a voided microvia (16% void ratio) of aspect ratio of 0.25 had a lower stress level than the non-voided microvia of aspect ratio of 0.5. Therefore, it is not a proper way to provide a single criterion (e.g. void size) for accepting or rejecting HDI boards with microvias without considering the geometry of the microvias and the void shape.

This paper provides the first study on delamination between microvia base and target pad using fracture analysis. A higher load level always resulted in a larger stress intensity factor – more likely to cause fracture and delamination. For Mode I fracture, a smaller initial crack length resulted in a larger stress intensity factor, and therefore was easier for the crack to grow. The Mode II stress intensity factor was less sensitive to the initial crack length.

As the most common failure mode, the delamination issue is worthy of more attention and future studies. The authors are interested in designing proper experiments to measure the critical fracture mechanics parameters (e.g. critical stress intensity factor or critical energy release rate) of the electroless copper, and simulate the crack growth process. Temperature, copper grain size, and cyclic loading all can affect the critical fracture mechanic parameters and the crack growth process. These variables will be considered in future research. Additionally, it is interesting to study the delamination on the interface between electroless copper and electrolytic copper (on microvia base or target pad), as well as estimate the competing failure mechanisms of the interface delamination and fracture in electroless copper.

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