# **IMPROVED SMT AND BLR OF 0.35MM PITCH WAFER LEVEL PACKAGES**

Brian Roggeman and Beth Keser Qualcomm Technologies, Inc. San Diego, CA, USA roggeman@qti.qualcomm.com

## ABSTRACT

The surface mount process to successfully mount 0.35mm pitch Wafer level packages (WLP) was studied. Processes including solder paste printing and flux dipping were examined and optimized. The paste print process was optimized in terms of printer setup to use standard materials. Flux dipping was used as an alternative to paste printing to address situations where print challenges cannot be overcome. Flux dipping often results in a decrease in board level due to the decrease in solder joint standoff, so a novel dip encapsulant was also included. The dip encapsulant is a polymer adhesive which encapsulates the BGA joints after reflow, providing some gain in reliability over standard flux dipping. For board level reliability, temperature cycling was performed using -40 to 125 C temperature swings. The lifetime and failure modes of the package were analyzed. This study shows optimized print process can be achieved using standard materials, yet alternative SMT processes can also be adopted to successfully assemble fine pitch WLP packages, while also considering board level reliability.

Key words: wafer level package, printing, SMT, BGA

#### **INTRODUCTION**

Wafer level packages (WLP) are rapidly being adopted in the mobile consumer space. The cumulative annual growth rate of WLP from 2014 to 2019 is predicted to be 8.7%, growing from 29.5B units to 44.6B. [1] WLP is used throughout the mobile application space including power management, RFIC, Bluetooth, Wi-Fi, WLAN, switches and tuners. Image sensors, microcontrollers, memory, discretes, and integrated passive devices also use WLP. WLP's small size and low cost make them widespread in consumer mobile wireless devices.

Internal package interconnects, such as flip chip bumps or wirebonds are eliminated in WLP, as well as the need for a substrate or leadframe for BGA level redistribution. The limitation of a WLP is its small package area due to its increased sensitivity to reliability as it gets larger.

Additionally, all the pins must fit within the die area at the pitch of a BGA. 0.5mm and 0.4mm BGA pitch wafer level packages are the most common in the industry. [2-5] Larger WLP's (i.e. >5mm) may experience solder joint failures during board level temperature cycle test due to a combination of the CTE mismatch between the WLP and PCB and the increased distance to neutral point (DNP) of the periphery pins. Therefore, in order to increase the number of BGA per WLP without increasing the WLP size,

the pitch must shrink. Alternatively, this saves cost by adding more pins without growing the silicon area.

Although finer pitches can shrink the die, save packaging costs and increase the number of pins for increased functionality, there are potential drawbacks. The ability to surface mount these finer pitches needs to be studied with the goal to use existing equipment and processes at the assembly sites. The PCB board design rules and features to support finer pitches also need to be evaluated to ensure finer pitches are not driving up board costs. The board level reliability of 0.35mm and 0.3 mm pitch WLP with fully populated ball arrays for 4mm x 4mm, 5mm x 5mm, and 6mm x 6mm test vehicle sizes has been reported previously [6]. This paper describes SMT process details of 0.35mm pitch WLP, including the use of a novel solder joint encapsulant as an alternative to paste printing.

#### EXPERIMENTAL

#### **Test Vehicle Description**

The wafer level packages created for this study use a Cu RDL metal structure to connect the die pad to the solder ball (Figure 1) rather than a ball on pad or ball on repassivation structure where the solder ball sits directly on the die pad or a polymer passivation opening over the die pad, respectively. Packages used a 0.35mm ball pitch and SAC405 solder balls. Packages were daisy chained through the top Al metal of the device for open/short monitoring after SMT.



Figure 1. RDL Type Wafer Level Package

PCBs were designed to the JEDEC drop test standard (JESD22-B111). The boards used a 1-6-1, eight layer stack-up, and 1mm final thickness. Non-solder mask defined copper pads were used with a 0.22mm diameter.

#### **SMT Assembly Process**

SMT assembly improvements focused on solder paste printer setup, paste material and alternate dipping process. Paste printing was performed on a high-volume SMT printer, using active force feedback squeegees. Dedicated vacuum tooling and over-the-top snugger clamps (side clamping) were used to support the PCB during printing. Other important printer parameters included on-contact printing and zero-separation distance, effectively releasing the PCB at the maximum speed after printing. Other parameters are described in the next section. A tandard leadfree reflow profile was used with a peak temperature of 245°C, as shown in Figure 2.



Figure 2. Standard lead-free reflow profile with 245°C peak.

# RESULTS

## **Paste Printing**

A key enabler to fine pitch WLP packaging is the SMT process, and specifically paste printing. This area has received much focus in recent years, with advances in stencils, squeegees and paste materials to achieve acceptable print deposits, particularly for challenging aperture area ratios. This portion of the study focused on printer setup to maximize transfer efficiency and minimize variation, while using standard material sets such as laser cut SS stencil and type 4 paste. Four factors were studied, including squeegee angle, squeegee overhang, print speed and print pressure. Factors are listed in Table 1, along with the values that were tested. A diagram of the squeegee angle and blade overhang is included in Figure 3, for reference.

Table 1. Factors and Le	els for Print l	Experiment
-------------------------	-----------------	------------

Factor	Levels
Squeegee angle (°)	45, 60
Squeegee blade overhang (mm)	6, 15
Print Pressure (KgF)	5, 7.4, 10
Print Speed (mm/s)	20, 30, 40



**Figure 3.** Illustration of squeegee blade for angle and overhang reference.

A partial factorial experiment was conducted to determine the effects of the factors shown in Table 1, and to select the optimal print parameters for the follow-on assembly portion of this study. Efforts were made to minimize other variables outside of the factors studied. The same stencil and solder paste were used for each leg. A new board was used for every print to prevent influence of PCB cleaning and residual solder particles. Multiple boards were printed for each factor to include both forward and backward strokes of the print head. Finally, the stencil was thoroughly cleaned in between each leg to reset the starting condition.

Solder deposits were analyzed using a 3D solder paste inspection (SPI) system. Because the paste and stencil remained the same throughout the experiment, transfer efficiency and standard deviation were used as a direct comparison between different printer setups. The data is plotted in Figure 4 for approximately 28,000 individual print deposits per condition. Several observations were made:

- 1. The 15mm overhang blade is not suitable for use with a 45° squeegee angle. Because of the longer overhang, the actual contact angle with the stencil due to downward pressure is very low and not conducive to good aperture fill.
- 2. Aside from the above condition, average transfer efficiency is approximately the same for all conditions. Average transfer efficiency is just a single indicator of print performance. Variability is also a critical parameter.
- 3. The 45° squeegee with 6mm blade overhang is generally less sensitive to speed and/or pressure settings when primarily considering the lower end of print deposits.
- 4. The 60° squeegee with 15mm blade overhang appears to have a wide range of tuning available. This means that the performance can be optimized with careful printer setup and monitoring.

The remainder of the experiment used a 60° squeegee angle and 15mm blade overhang for SMT assembly. Type 4 and Type 5 pastes were investigated, both using a SAC305 alloy. The print performance comparison, holding all other variables constant, is shown as a histogram in Figure 5 as measured by SPI. The stencil used for assembly was  $100\mu$ m thick and had 220 $\mu$ m aperture size for an area ratio of 0.55. Given a specified printer setup, the Type 5 paste achieves higher transfer efficiency and lower variability, as expected. Lower and upper spec limits on transfer efficiency were set to 50% and 150%, respectively. This results in Cpk 1.22 for Type 4 paste and 2.52 for Type 5 paste. An example of the print quality for Type 5 solder paste is shown in Figure 6. The consistency of the print volume is illustrated, and visibly corresponds to the SPI data.



**Figure 4.** Print results as a function of Pressure, Speed, Blade Length and Squeegee Angle. Top: transfer efficiency; Bottom: standard deviation.



**Figure 5.** Transfer Efficiency histogram for Type 4 and Type 5 solder paste on a 100 $\mu$ m thick stencil with 220 $\mu$ m aperture (0.55 AR). Type 4 Cpk = 1.22; Type 5 Cpk = 2.52.



Figure 6. Print quality using Type 5 solder paste

SMT results achieved 100% for both paste types. Time zero cross-sections were prepared to analyze the solder joint formation with both paste types. Figure 7 shows representative cross-sections for Type 4 and Type 5 paste assembly. No differences in solder joint standoff, voiding levels, IMC formation or grain structures was observed.



**Figure 7.** Cross-section images for assemblies built different solder paste. (a) Type 4 paste; (b) Type 5 paste.

## Alternate SMT: Flux dip and Joint Encapsulant

When challenges in solder paste printing for fine pitch WLP packages cannot be overcome, flux dipping may be a solution for SMT assembly. Traditional tacky fluxes have been developed for use in package-on-package assembly, and are also well suited for assembly of fine pitch packages. Because no extra solder material is introduced through flux dipping, the final solder joint standoff will be reduced versus a standard printing process. In turn, the reliability could be negatively affected. New encapsulant flux materials, which act as a solder joint encapsulant after reflow, have been developed specifically to enhance reliability.

The encapsulant flux is a polymer adhesive which encapsulates the BGA joints after reflow. During the reflow process, this polymer adhesive removes metal oxide and allows the solder joint to be formed, similar to a traditional tacky flux. A 3-D polymer network forms and encapsulates the joints, providing mechanical reinforcement not unlike underfill.

This study investigated the use of traditional tacky flux dipping, as well as the use of a dippable encapsulant flux. Both materials were transferred to the solder joint through a

linear flux transfer unit attached to the placement machine. Flux depth will vary based on the viscosity and thixotropic properties of the material, even for a fixed reservoir depth, so best practice is to use a thin film gauge with fine increments to get an accurate measurement of the depth. The targeted thickness was minimum 70% of the solder ball height. Several machine settings can be adjusted which affect the final material transfer, including dip speed, dwell time, extraction speed, and milling frequency and speed [7]. Basic machine settings were optimized for standard tacky flux and then adjusted for the encapsulant flux.

Due to the increased tackiness of the encapsulant flux, several process adjustments were required to transfer adequate material while also successfully removing packages from the encapsulant film. The pickup nozzle was increased in size so that the inner diameter roughly matched the package body size, effectively maximizing vacuum suction on the package. The extraction speed after dipping was also reduced by half versus traditional tacky flux to ensure packages remained on the pickup nozzle after dipping. After these process adjustments, 100% of packages were successfully dipped and placed onto PCBs.

Figure 8 shows examples of the material transfer after dipping in the encapsulant flux. Ball coverage is approximately 75% based on the wetted height measurement of the encapsulant. Post-SMT coverage is shown in Figure 9. The encapsulant only covers the bottom half of the solder joint, with no reinforcement at the top side near the underbump metallurgy (UBM). Ideally the encapsulant should reinforce both the top and bottom of the solder joint for maximum reliability improvement.



**Figure 8.** Encapsulant coverage on solder balls after dipping. (a) Single solder ball showing approximately 75% coverage by wetted height; (b) Array of balls showing consistency in coverage.



**Figure 9.** Post-SMT coverage is limited to the bottom of the solder joint with no reinforcement near the package UBM

Additional efforts were made to increase encapsulant volume, so that the post-SMT solder joint would have reinforcement at both top and bottom side of the joint. The typical process adjustment would be to increase the thickness of the film by changing the reservoir depth. However, control of reservoir depth was too coarse for the small solder ball height. Instead, volume increase was achieved by encouraging capillary flow of the encapsulant onto the solder ball. Increasing the dwell time in the encapsulant and further reducing the extraction speed resulted in better coverage. Figure 10 shows the result, with full wetting observed on solder balls near the edge and corners of the package. Balls near the center of the package are only covered approximately 90%, as measured by wetted height onto the ball. As WLP packages are typically quite flat, warpage was not suspected to be the cause of the inconsistent coverage. Rather, it is assumed that the material is displaced laterally when the package is dipped, and the edge-most solder joints receive the most benefit of capillary flow due to the surrounding material in the reservoir. The post-SMT coverage at the edge of the package is shown in Figure 11, with material coverage at both the top and bottom of the solder joint, as desired.







**Figure 10.** Encapsulant coverage on solder balls after dipping. (a) Fully covered solder ball on the edge of the package; (b) solder balls towards the center are approximately 90% covered, but no material has wet to the WLP package.



**Figure 11.** Post-SMT coverage of edge solder joints after further optimization of dip process

Dipping in encapsulant flux proved to be challenging due to the small solder ball height and requirement of material coverage, so printing the encapsulant material was also investigated. Initial evaluations used the same settings as were used as for paste printing. Additional optmization was not performed for this material. SPI could not be used to inspect print quality due to the optically clear condition of the encapsulant flux, so visual inspection was used. An example of the print result is shown in Figure 12. Unlike the solder paste shown in Figure 6, the encapsulant does not remain where printed and flows out across multiple pads. Because the material has no metal, the risk of shorting during reflow was considered low, and in fact no shorting was observed after SMT. Similar to the initial dip trials, reinforcement of just the bottom of the solder joint was achieved post-SMT (Figure 13). Additional printing optimization is expected to improve the coverage, but that was outside the scope of this effort.

All processes resulted in 100% SMT yield, and the summary is shown in Table 2.



**Figure 12.** Print result of the encapsulant flux. The material flows across multiple pads.



**Figure 13.** Post-SMT encapsulant coverage after printing the material using paste-print parameters. Only the bottom of the solder joint is reinforced.

Table 2. SMT yield re	esults across	all processes,	inspected
for opens and shorts			

SMT Process	Quantity
Print, Type 4 Paste	60/60 = 100%
Print, Type 5 Paste	30/30 = 100%
Dip, Tacky Flux	30/30 = 100%
Dip, Encapsulant Flux	75/75 = 100%
Print, Encapsulant Flux	30/30 = 100%

#### **Board Level Reliability**

Temperature cycling reliability was used a verification of the SMT process parameters. Temperature cycling is a main driver of WLP packaging due to the CTE mismatch between the Si and the PCB. Two daisy chain nets were monitored for failure, including corner solder joints that are considered non-critical to function (NCTF), and non-corner solder joints that are critical to function (CTF). Packages were cycled from -40°C to 125°C, with 10 minute dwells at the extremes. Figure 14 shows an illustration of the temperature cycle used in this analysis.



Figure 14. -40/125°C temperature cycle profile

Failures were fit to a 2-parameter Weibull distribution for analysis. For comparison purposes, the 5% cumulative failure rate (CFR) was calculated from the distribution. This was used instead of mean or characteristic life because it better captures the behavior of early failures, which are assumed to be more critical to the success of a process. The summary of relative differences is presented in Table 3, with the Type 4 paste print process used as the control. The reliability using printed encapsulant is not considered because the process was not fully optimized.

Table 3.	Summary	of tem	perature	cycle	results
----------	---------	--------	----------	-------	---------

	Relative Result (5% CF		
SMT Process	Corner	Non-Corner	
	Joints	Joints	
Print, Type 4 Paste	Control	Control	
Dip, Tacky Flux	↓ 19%	↓ 5%	
Dip, Encapsulant Flux	↑ 10%	↓ 14%	

The tacky flux shows a consistent reduction in reliability compared to the paste print process, on both corner and noncorner solder joints. This result is consistent with previously reported data on non-WLP packages [8]. The reduction in reliability is related to the reduced standoff when using flux instead of paste.

The encapsulant flux results in a 10% *improvement* in the reliability (at 5% CFR) of the corner solder joints over a paste print process and a 36% improvement over tacky flux. This improvement can be related to maximum reinforcement of the joint by full coverage of the material, as shown in Figures 10 and 11. An example of the weibull failure distribution is shown in Figure 14 for the corner

solder joints. Solder joints not near the edge of the package were not fully encapsulated, which in turn lowers the reliability of the non-coner joints.



**Figure 15.** Example Weibull plot illustrating improvement in corner joint reliability with encapsulant flux, but reduction in reliability with tacky flux.

# CONCLUSIONS

This study examined improvements in the SMT process for successfully integrating 0.35mm pitch wafer level packages. The solder paste print result was shown to be sensitive to printer parameters, including pressure, speed and squeegee type. It was shown that an optimized setup could be achieved on a challenging stencil aperture area ratio of 0.55. More importantly, the results were achieved using a standard Type 4 paste, and otherwise standard equipment sets and stencil type. Type 5 paste further improved the print result in terms of maximizing transfer efficiency and minimizing variability, however it was determined that the finer powder size was not required if print setup was optimized.

As an alternative to printing, a novel solder joint encapsulant was investigated. Full solder joint coverage was only achieved after significant adjustments to the dip process. When full coverage could be achieved, such as on edge/corner solder joints, the reliability was improved over a standard paste print process and tacky flux. Ultimately paste printing with well controlled print process can achieve excellent SMT results and high reliability of 0.35mm WLP packages.

## ACKNOWLEDGEMENTS

The authors would like to thank Nick Leonardi and Dr. Wusheng Yin from Yincae for supplying the encapsulant material, and Steven Lehtonen and Donato Esteban of Qualcomm's packaging lab for assembly and failure analysis support.

## REFERENCES

[1] Vardaman, E. Jan, Yancey, T. "2015 Flip Chip and WLP: Emerging Trends and Forecasts," p7, 2015.

[2] Tee, T.Y, Tan, L.B., Anderson, R., Ng, H.S., Low, J.H., Khoo, C.P., Moody, R., Rogers, B., "Advanced Analysis of WLCSP Copper Interconnect Reliability under Board Level Drop Test," Proc. IEEE Electronics Packaging Technology Conference, 2008, pp. 1086-1095.

[3] Fan, X., and Han, Q., "Design and Reliability in Wafer Level Packaging," Proc. IEEE Electronics Packaging Technology Conference, 2008, pp. 834-841.

[4] Cergel, L., Wetz, L., Keser, B., White, J., "Chip Size Packages with Wafer Level Ball Attach and their Reliability," Proc. of 4th International Conference on Advanced Semiconductor Devices and Microsystems, 2002, pp. 27-30.

[5] Yang, D., Ye, X., Xiao, F., Chen, D., Zhang, L., "Reliability of Fine Pitch Wafer Level Packages," International Conference on Electronic Packaging Technology and High Density Packaging, 2012, pp. 1097-1101.

[6] Keser, B., Alvarado, R., Choi, A., Schwarz, M., Bezuk, S., "Board Level Reliability and Surface Mount Assembly of 0.35mm and 0.3mm Pitch Wafer Level Packages," Proc. IEEE Electronics Packaging Technology Conference, 2014, pp. 925-930.

[7] Roggeman, B., Vicari, D., Smith, L., Syed, A., "Material Selection and Parameter Optimization for Reliable TMV PoP Assembly", Proceedings of SMTA International, Ft. Worth TX, October, 2011.

[8] Choi, A., Roggeman, B., Schwarz, M., "Demonstrated Process And Reliability Of 0.35 mm Pitch BGA Devices For Mobile Environment", Proceedings of SMTA International, Orlando FL, October 2013