

Improve SMT Assembly Yields Using Root Cause Analysis in Stencil Design

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Abstract

Reduction of first pass defects in the SMT assembly process minimizes cost, assembly time and improves reliability. These three areas, cost, delivery and reliability determine manufacturing yields and are key in maintaining a successful and profitable assembly process. It is commonly accepted that the solder paste printing process causes the highest percentage of yield challenges in the SMT assembly process. As form factor continues to get smaller, the challenge to obtain 100% yield becomes more difficult. This paper will identify defects affecting SMT yields in the printing process and discuss their Root Cause. Outer layer copper weight and surface treatment will also be addressed as to their effect on printability. Experiments using leadless and emerging components will be studied and root cause analysis will be presented on the following common SMT defects:

- Poor Solder Paste Release: Focus will be placed on small components
- Solder-balls (Mid Chip Solder Beads): Stencil design to minimize solderballs
- Tombstoning: Improving tombstoning with stencil design
- Bridging at Print: Simple guidelines to eliminate bridging
- Bridging at SMT Reflow: What causes bridging after reflow when it is not present after print
- Insufficient Solder Volume at SMT Reflow: Look at the correlation of stencil design to solder volume after reflow
- Voiding: Design ideas to reduce voiding through stencil design

Root causes of these challenges will be identified and practical stencil design recommendations will be made with the intent of eliminating defects and improving yields during the printing process.

Introduction

Component miniaturization is a way of life in the SMT assembly industry and as smaller components continue to become mainstream, larger, established components continue to be used in the same assemblies. In addition to requiring these challenging mixes of technology, end users are also pushing for improved yields and improved product reliability. The ability of the assembly operation to reduce defects in the SMT assembly process can minimize cost, reduce assembly time and ultimately improve product reliability.

By identifying the most common types of SMT defects in the process, focus can be placed on specific ways to eliminate those defects. The common SMT defects addressed in this paper are poor solder paste release, bridging at print, insufficient solder volume at reflow and bridging at reflow, mid-chip solder balls, tombstoning, and voiding. Causes of these defects will be addressed along with stencil design solutions that have been utilized in production situations to reduce and in many cases eliminate the defects altogether. These common SMT defects can be referred to as “universal” defects in that their presence can be seen across multiple companies, in multiple product builds over many years. In previous work [1], R. Dervaes states, “Determining the root cause of a “universal” SMT defect, that is more assembly independent, involves testing a very wide array of assemblies over a much longer period than can be fit into one experiment.” This paper is a continuation of the Dervaes’ work and utilizes both experimental data and customer feedback.

Root Cause Analysis to Improve Poor Solder Paste Release

Historically the best method of predicting solder paste release is to calculate the aperture Area Ratio (Figure 1). It can be used on any stencil aperture, regardless of the shape, and compares the surface area of the stencil opening to the surface area of the stencil aperture walls. IPC recommends a minimum area ratio of 0.66 for acceptable solder paste release [2].

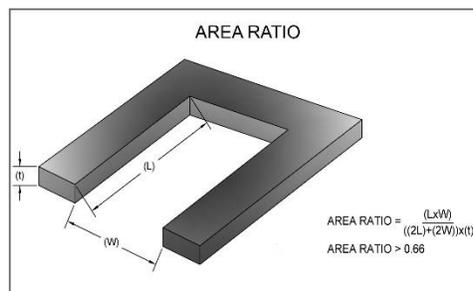


Figure 1 - Stencil Area Ratio

The current stencil area ratio only considers the stencil thickness and stencil aperture size when predicting solder paste release and the printed circuit board (PCB) is not considered. The question becomes, “Is the adhesion of the solder paste to the PWB SMT pad what pulls the solder paste out of the stencil?” If so, the adhesion strength of the solder paste to the PWB SMT pad is determined by the size of the SMT pad, and the corresponding surface area. In addition, differences in copper weight and surface finishes would produce differences in PWB pad sizes at the surface of the PWB and these differences could become critical to improve solder paste release.

The PCB manufacturing process consists of etching the copper to produce the circuitry (traces, SMT pads, via pads, etc.) and the copper etching process produces a SMT pad cross section (Figure 2) where the top of the SMT pad is smaller than the bottom.

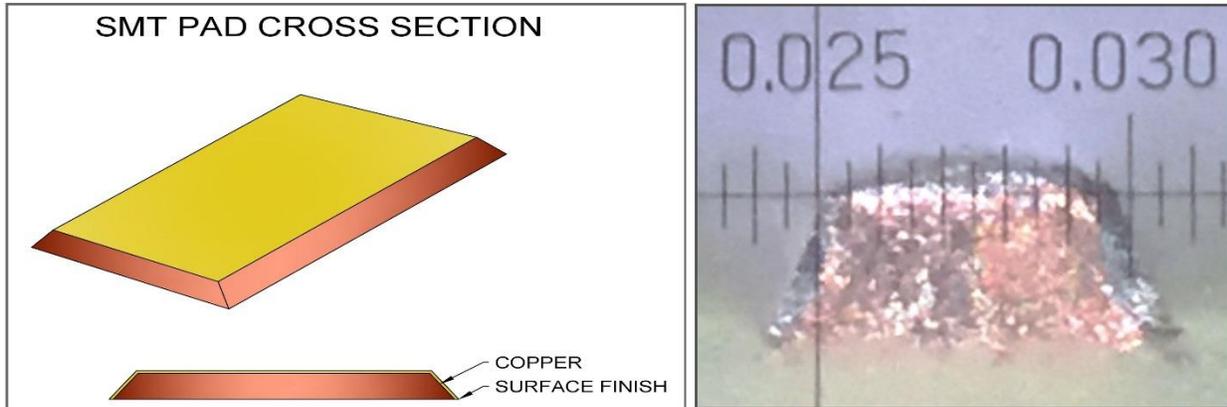


Figure 2 - SMT Pad Cross Section

During the design stage of the PWB, lines, traces and pads are “modified” to allow for etch back during its fabrication process. The results typically show the top of the SMT pad will be smaller than the base and as copper weights increase, the pad dimensions at the surface can be smaller than the nominal Gerber SMT pad size. The smaller pad size on the top surface of the PWB could potentially affect the release of paste. If this is true, a new modified Surface Area Ratio should be used to predict sufficient transfer efficiency of the solder paste for small component printing. A test vehicle (Figure 4) with 5 mil lines and 7 mil spaces in the upper left and bottom of the board was used in this experiment. Cross sections were taken from the boards after fabrication and an optical measuring device was used to measure the tops of the 5 mil traces to determine etch back as compared to nominal from the Gerber file. The measurements are recorded in Table 1.

Table 1 - PWB Measurements

| Cu Weight | Surface Finish | Surface Measurement(mils) | Difference-Surface versus Nominal(mils) | Foot Measurement(mils) |
|-----------|----------------|---------------------------|---|------------------------|
| 2 oz | HASL | 0.004173 | -0.0008 | 0.005906 |
| 2 oz | HASL | 0.004016 | -0.0010 | 0.005492 |
| 2 oz | ENIG | 0.004874 | -.00012 | 0.005911 |
| 1 oz | HASL | 0.004252 | -0.0007 | 0.005236 |
| 1 oz | HASL | 0.003937 | -0.0011 | 0.005807 |
| 1 oz | ENIG | 0.004823 | -0.0002 | 0.005906 |
| 1 oz | ENIG | 0.004991 | -0.0000 | 0.006063 |

To accurately determine if the PWB configuration affects paste transfer efficiency at print, a modified Surface Area Ratio formula was determined (Figure 3).

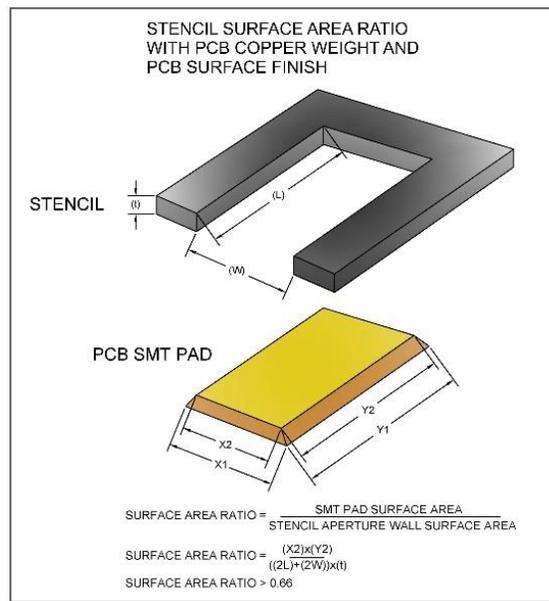


Figure 3 - Modified Surface Area Ratio

The modified comparison takes into account changes in PCB SMT pad sizes due to variations in copper weights and surface finishes. Heavier copper weights will produce larger reductions at the surface of the SMT pad as compared to the actual board Gerber data. Flat surface finishes, like ENIG, OSP, immersion Ag, and immersion Sn, allow the solder paste to stick to the entire top surface of the SMT pad (assuming PCB-to-stencil alignment is accurate) for maximum adhesion strength. When these flat surface finishes are used no size reductions is used when calculating Surface Area Ratio for the surface finish. Non-flat surface finishes, like HASL, have a more domed/irregular surface and the semi-rounded surface makes it more difficult for the solder paste to stick to the entire surface. When HASL and HAL surface finishes are used, an additional reduction is made to calculate the Surface Area Ratio. To calculate this modified Surface Area Ratio, the following table has been created based on measurement of finished board data (Table 2).

Table 2 - SMT Pad Reductions to Calculate Modified Surface Area Ratio

| Copper Weight (oz) | Copper Thickness (µm) | Size Reduction mm(inches) | Size Reduction mm(inches) with ENIG, OSP, Ag, Sn | Size Reduction mm(inches) with HASL & HAL |
|--------------------|-----------------------|---------------------------|--|---|
| 0.5 | 17.5 | 0 | 0 | 0.001 |
| 1 | 35 | 0.0005 | 0 | .0005 |
| 2 | 70 | .001 | 0 | 0.001 |

Utilizing the SMT pad size reductions in Table 3 will provide a much more realistic representation of what SMT pad sizes to expect on physical PCBs, and the modified Surface Area Ratio will be used to test this theory.

Table 3 - Example of Modified Area Ratio

| Component | Copper Weight | Surface Finish | PWB Pad Size | Stencil Aperture Size | Area Ratio | Surface Area Ratio |
|-----------|---------------|----------------|--------------|-------------------------|------------|--------------------|
| .4 BGA | 2 oz | HASL | 9 mil Round | 7 mil Sq, 2 mil Radius | 0.44 | 0.44 |
| .4 BGA | 2 oz | HASL | 9 mil Round | 9 mil Round | 0.56 | 0.34 |
| .4 BGA | 2 oz | HASL | 9 mil Round | 11 mil Sq, 2 mil Radius | 0.69 | 0.28 |
| uBGA | 2 oz | HASL | 11 mil Round | 9 mil Sq, 2 mil Radius | 0.56 | 0.56 |
| uBGA | 2 oz | HASL | 11 mil Round | 11 mil Round | 0.69 | 0.46 |
| uBGA | 2 oz | HASL | 11 mil Round | 13 mil Sq, 2 mil Radius | 0.81 | 0.39 |

Methodology to Test Surface Area Ratio Theory

The test vehicle shown in Figure 4 was created to verify if a modified area ratio (Surface Area Ratio) based on the PWB configuration would aid in paste transfer efficiency for smaller components. This vehicle was created in 1 oz and 2 oz copper weight with both HASL and ENIG finishes. Over/under printing scenarios were created to confirm whether or not designing stencil apertures based on this modified *Surface Area Ratio* would reduce or improve solder paste release.

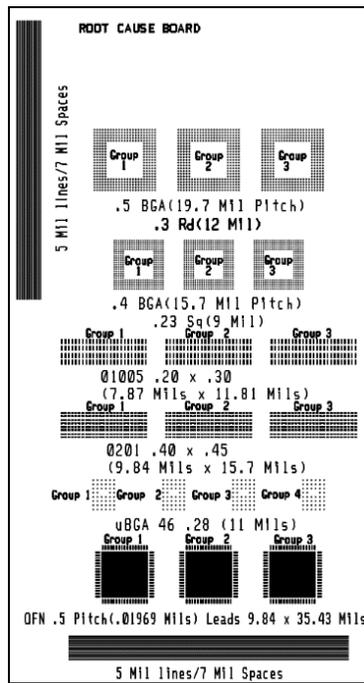


Figure 4 -Test Vehicle

The table below (Table 4) shows the stencil aperture design for each of the component shapes above. Two 4 mil thick stencils were used. One stencil was uncoated and a second stencil was coated with a Fluoro-Polymer Nano Coating (FPN).

Table 4 - Stencil Aperture Sizes

| Component | Group | PWB Pad Size | Stencil Aperture Size |
|-----------|-------|-------------------|--------------------------|
| .5 BGA | 1 | 12 mil Round | 10 mil Sq, 2 mil Radius |
| .5 BGA | 2 | 12 mil Round | 12 mil Round |
| .5 BGA | 3 | 13 mil Round | 14 mil Sq, 2 mil Radius |
| .4 BGA | 1 | 9 mil Round | 7 mil Sq, 2 mil Radius |
| .4 BGA | 2 | 9 mil Round | 9 mil Round |
| .4 BGA | 3 | 9 mil Round | 11 mil Sq, 2 mil Radius |
| 01005 | 1 | 7.9 x 11.8 mils | 5.9 x 9.8 , 2 mil Radius |
| 01005 | 2 | 7.9 x 11.8 mils | 7.9 x 11.8, 2 mil Radius |
| 01005 | 3 | 7.9 x 11.8 mils | 7.9 x 9, 2 mil Radius |
| 0201 | 1 | 15.7 x 9.8 mils | 13.7 x 7.8, 2 mil Radius |
| 0201 | 2 | 15.7 x 9.8 mils | 15.7 x 9.8, 2 mil Radius |
| 0201 | 3 | 15.7 x 9.8 mils | 14.7 x 8.8, 2 mil Radius |
| uBGA | 1 | 11 mil Round | 9 mil Sq, 2 mil Radius |
| uBGA | 2 | 11 mil Round | 11 mil Round |
| uBGA | 3 | 11 mil Round | 13 mil Sq, 2 mil Radius |
| uBGA | 4 | 11 mil Round | 15 mil Sq, 2 mil Radius |
| QFN | 1 | 35.4 x 9.8 Oblong | 55.4 x 9.8, Oblong |
| QFN | 2 | 35.4 x 9.8 Oblong | 35.4 x 9.8, Oblong |
| QFN | 3 | 35.4 x 9.8 Oblong | 65.4 x 7.8, Oblong |

Five boards with 2 oz Copper and HASL finish were printed with a common No-Clean SAC305, Type 4 solder paste and 5 boards were printed using a common Water Soluble SAC305, Type 3 solder paste. In addition, 5 boards were printed with 1 oz ENIG and 1 oz HASL using the No-Clean SAC305 Type 4 paste. All printed solder paste bricks were then measured after print using a production 3D solder paste measurement system to obtain printed volume and transfer efficiency was calculated.

Test Results comparing Area Ratio to Surface Area Ratio

Results were charted showing Transfer Efficiency versus Area Ratio for both types of paste and each board type as well as Transfer Efficiency versus Surface Area Ratio. The results are shown below (Figures 5 and 6).

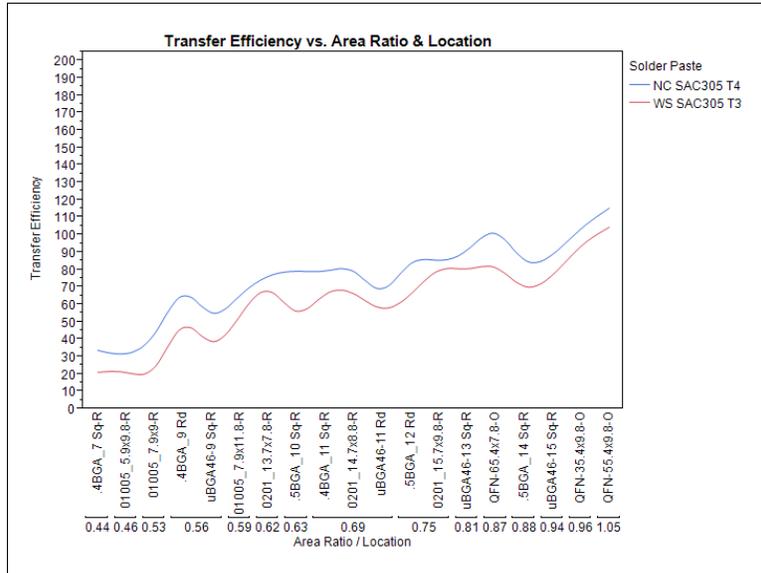


Figure 5 – 2 oz Cu, TE versus Area Ratio and Location by Paste Type

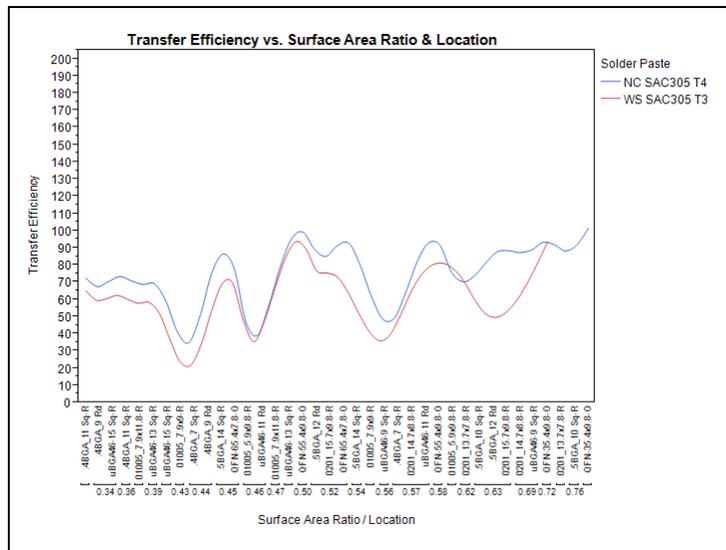


Figure 6 - 2 oz Cu, TE vs Surface Area Ratio and Location by Paste Type

One can see from the graph above (Figure 5) that as the standard area ratio increases, the transfer efficiency also increases in a linear fashion. Also, as expected, transfer efficiency is better when using No Clean, type 4 paste versus Water Soluble, type 3 paste. However, when looking at the chart by Surface Area Ratio (Figure 6), transfer efficiencies do not increase in a linear path. It is easier to see the validity of this modified Surface Area Ratio if one looks at a specific component (Figure 7).

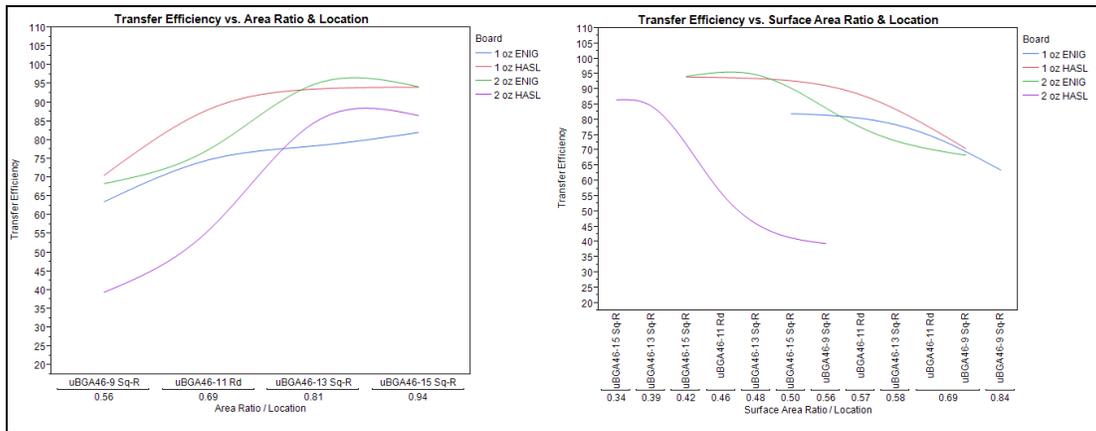


Figure 7 – Transfer Efficiency Vs Area Ratio vs Surface Area Ratio for uBGA46 by Board Type

When looking at the 46 pin uBGA component data, it is easy to see that calculating Surface Area Ratio based on copper weight of the outer layer and the surface finish on the board is not a good method to determine improved transfer efficiency. As the Surface Area Ratio increases, transfer efficiency decreases. Data from other components followed this same trend. This experimental test process establishes that although the copper weight of the outer layers of the board and surface finish do impact transfer efficiency, the area ratio calculation is the best method of predicting transfer efficiency.

Results and Recommendations for Improving Paste Release

By examining this data, the best method to predict improvement in transfer efficiency is to consider area ratio. The data collected also shows that when FPN coatings are used, improved transfer efficiencies can be realized versus uncoated stencils for the same area ratio (Figure 8).

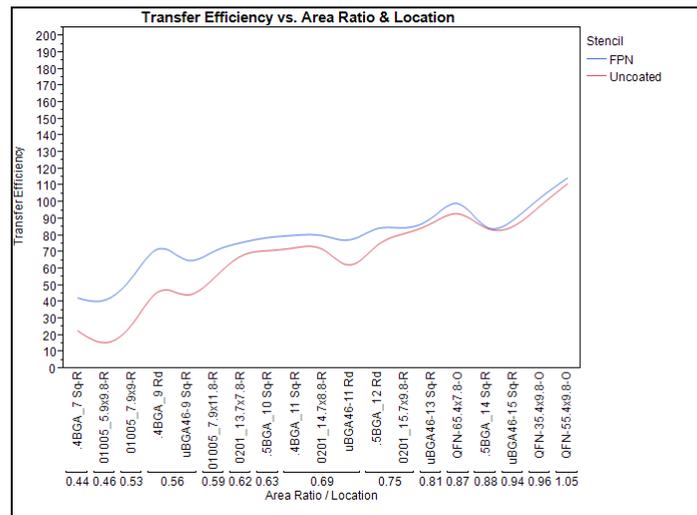


Figure 8 – Transfer Efficiency vs Area Ratio by Stencil Type

It is also worth noting that standard deviations are also reduced using FPN coatings versus uncoated stencils. In Figure 9 below, the standard deviation for area ratios between 0.56 and 0.81 is less on FPN coated stencils than uncoated stencils. Once area ratios increase higher than 0.81, the benefit of FPN coatings to reduce standard deviation no longer exists.

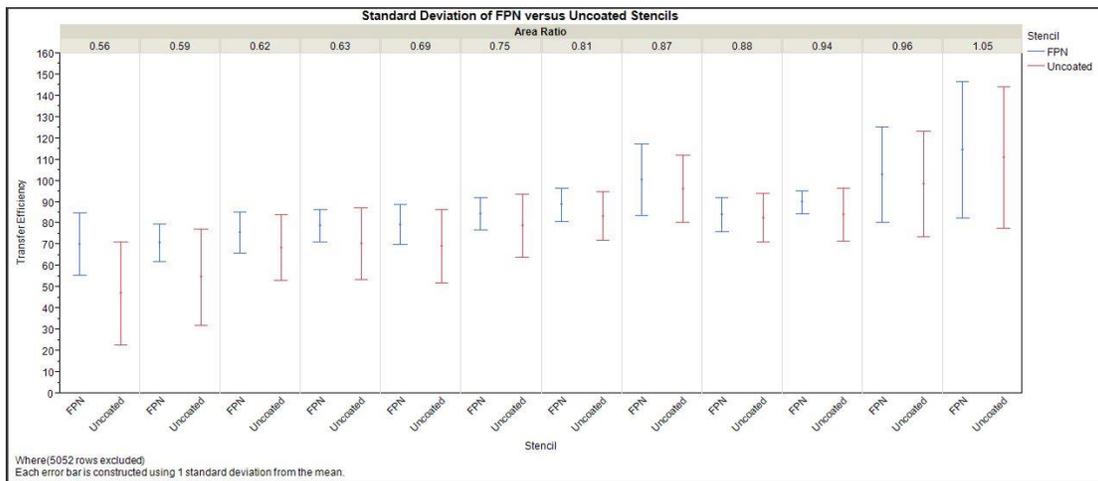


Figure 9 – Transfer Efficiency vs Standard Deviation by Stencil Type

Using the following graph (Figure 10), recommendations can be made as to minimum area ratios used to achieve targeted transfer efficiencies. Again, these recommendations are for 4 mil stencils using 3D SPI equipment and a no-clean paste. It is necessary for manufacturers to consider their specific SPI results versus Area Ratio to determine what minimum transfer efficiency is required to produce acceptable results. It is also necessary for manufacturers to determine what transfer efficiencies are required for small component printing to achieve acceptable solder joints.

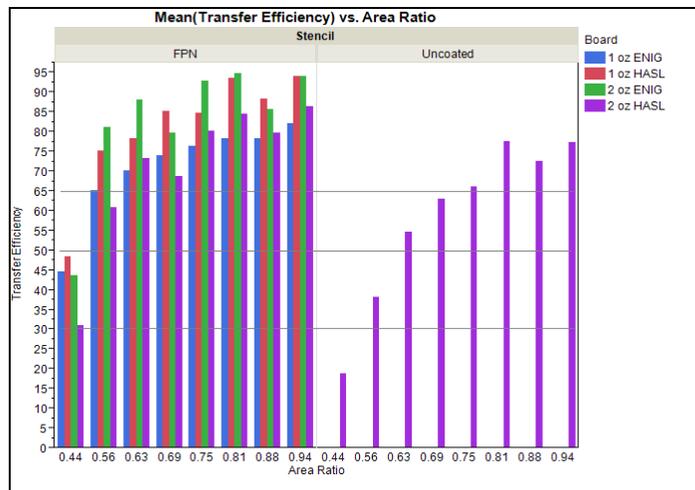


Figure 10 – Transfer Efficiency vs Area Ratio by Board/Finish

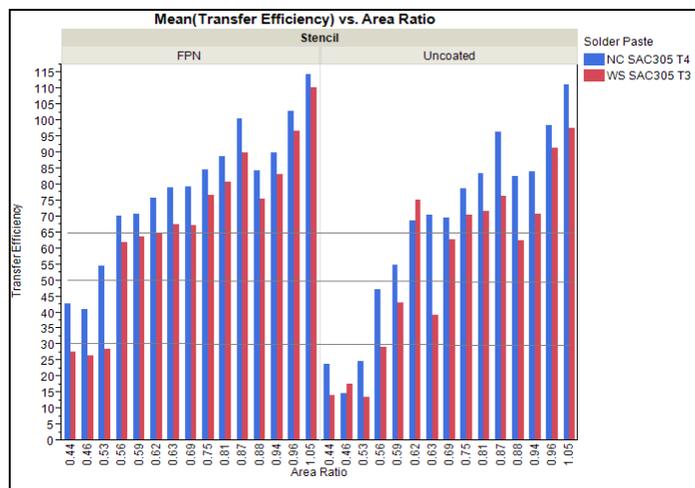


Figure 11 – Transfer Efficiency vs Area Ratio by Stencil and Paste Type

If 50% transfer efficiency is adequate, an uncoated 4 mil stencil can be used according to Figure 9 above. The lowest area ratio recommended is 0.63 which is very close to the current IPC recommendation [2] of 0.66. If a 30% transfer efficiency is acceptable, one could accept down to 0.55 area ratio with an uncoated stencil. An example based on the statements above is that one could expect to see close to 50% transfer efficiency on a 10 mil aperture using a 4 mil stencil. In previous work, Bath [3] showed that a 10 mil aperture in a 0.4mm pitch CSP with an area ratio of 0.63 printed at 56.9% transfer efficiency using an uncoated stencil which coincides with the data in this study.

Again, if 50% transfer efficiency is adequate, an FPN coated stencil can be used down to 0.5 area ratio according to the data in Figure 8 above. Again, in previous work, Bath [3] confirms that a 0.3mm CSP, 8 mil aperture with an area ratio of 0.50 printed at 55.5% transfer efficiency which is in line with the data in this study. If smaller transfer efficiencies are proven to create acceptable solder joints then lower area ratios can be used. Looking at the 0.44 area ratio component above which is the 7mil square with rounded corner aperture, one could expect at least 42% transfer efficiency with the Type 4 No Clean solder paste used in this study (Figure 11).

When performing Root Cause Analysis in situations of inadequate solder paste transfer, solder paste should also be considered. Looking at Figure 11 above, it is clearly seen that paste type and powder size can play a factor in obtaining adequate transfer efficiency. For example, looking at the uncoated stencil data, one could expect to see 50% transfer efficiency with a 0.59 area ratio aperture using a No Clean, Type 4 paste. The same aperture printed with a Water Soluble, Type 3 paste would only provide 43% transfer efficiency. Looking at the FPN stencil data, the 0.53 area ratio component release at 55% transfer efficiency with the No Clean, Type 4 paste whereas the Water Soluble, Type 3 paste releases only 28%.

This data is also dependent on the actual brand of solder paste being used in addition to the paste type and powder size. Solder paste from different manufacturers will give different transfer efficiencies. Again, when performing a root cause analysis for insufficient paste, these factors should be considered.

Solder-Balls (Mid Chip Solder Beads): Stencil Design to Minimize Solder Balls

Solder balls on two pin chips appear after reflow but in many instances can be prevented or greatly reduced by stencil design. When performing Root Cause Analysis on a stencil design to prevent solder balls, one must look at the design of the stencil apertures in relation to the actual part package. In many instances where solder balls are occurring, there is a mismatch in the design of the stencil apertures versus how the component sits on the SMT pads. It is critical at this step that all of the Gerber layers are available as the actual copper outer layers and mask layers will be needed for this process. The first step is to identify the actual dimensions of the part package and this can be done by referring to a chip design guide such as the one below (Figure 12).

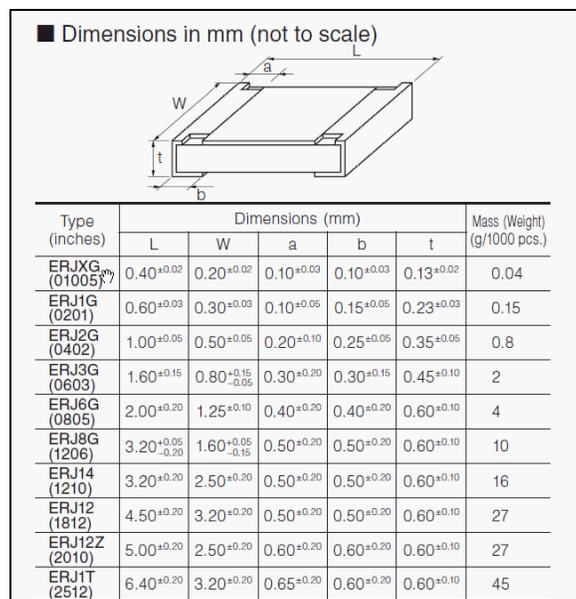


Figure 12 – Chip Design Guide

Once the chip design has been obtained and the size of the package determined, one must overlay the component part outline over the stencil apertures using a Gerber editor. Once this is done, the outside edge of the component should sit very close to the midpoint of the stencil apertures. Through many years and designs, the “U-Shape” aperture has produced the best reduction in Mid Chip Solder Balls (Figure 13). When designing the “U-Shape” aperture, one should pull the aperture toward the inside of the component so that D_t is at the inside edge of the terminal or 2-3 mils inside the terminal edge. Please note that there should be 7.5 mils minimum between the inside edges of the stencil apertures (C_s) for 0201 and larger chip components.

The inverted homeplate (Figure 14) has also shown good ability to reduce solder balls. The same design parameters should be applied to this shape as the “U-Shape”. Both of these designs remove solder paste from the center, inside edge of the component and effectively prevent “squeeze out” during placement that might allow solder balls to develop during reflow. One final consideration is that when applying this design to chip components, the area ratio must be considered. When changing from a rectangle to this “U-Shape” more surface area is being added to the aperture walls. If the area ratio limit (i.e., 0.63) is exceeded, a standard reduction should be made and a rounded square or rectangular aperture should be used.

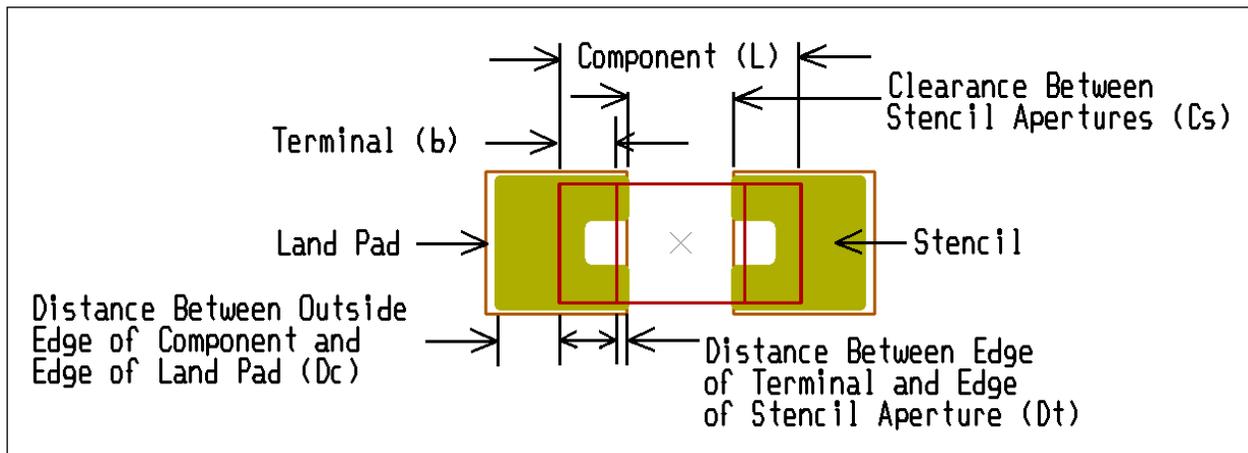


Figure 13 – “U Shape” Aperture Design to Prevent Solder Balls During Reflow

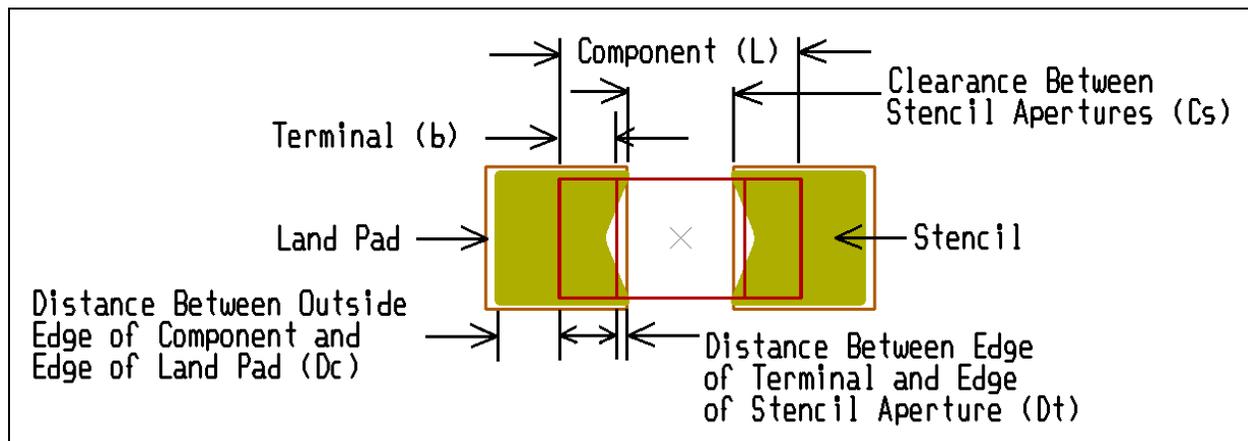


Figure 14 – Inverted Homeplate Aperture Design to Prevent Solder Balls During Reflow

Tombstoning: Improving Tombstoning with Stencil Design

Tombstoning defects on two pin chips may appear after reflow, but in many cases, can be mitigated through stencil design. This process is very similar to performing Root Cause Analysis to prevent solder balls in that one must look at the design of the stencil apertures in relation to the actual part package. Often, when tombstoning is occurring, there is a mismatch in the design of the stencil apertures versus how the component sits on the SMT pads. It is critical at this step that all of the Gerber layers are available as the actual copper outer layers and mask layers will be needed for this process and not just the solder paste layer. The first step is to identify the actual dimensions of the part package by referring to a chip design guide such as the one above (Figure 12).

Once the chip design has been obtained and the size of the package determined, one must overlay the component part outline over the stencil apertures using a Gerber editor. When this is done, the outside edge of the component should sit very close to the midpoint of the stencil apertures. If there is a large area extending beyond the component edge, there is more area to allow one side to melt or become molten before the other side which can cause tombstoning. Again, through many years of design, the “Reverse U-Shape” aperture has produced the best reduction in tombstoning (Figure 15).

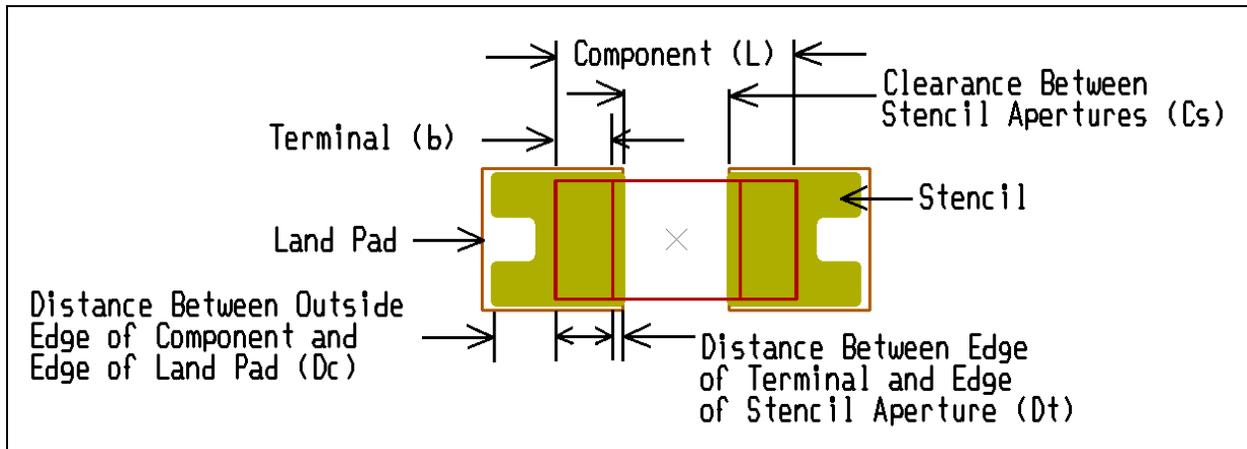


Figure 15 – “Reverse U Shape” Aperture Design to Prevent Tombstoning During Reflow

This design removes solder volume from the back end of the package so that when the paste reflows, it wants to spread or pull toward the outside of the apertures holding the component down flat during reflow. Put in another way, removing this paste on the outside of the component lowers the wetting force of the solder when it becomes liquid and helps prevent the component from tombstoning. When designing the “Reverse U-Shape” aperture, one should pull the aperture toward the inside of the component so that D_t is at the inside edge of the terminal or 2-3 mils inside the terminal edge. Please note that there should be 7.5 mils minimum between the inside edges of the stencil apertures (C_s) for 0201 and larger chip components.

There are a lot of scenarios where the SMT pads on the board are not optimum. Sometimes the pads are shifted too far apart and sometimes pads are too long. In many cases, the solder paste brick needs to be pulled toward the inside of the component removing paste from the outside of the component pads. Again, this places more paste under the part so that when it turns liquid, the paste spreads from under the component to the outside holding the component down.

One final consideration is that when applying this design to chip components, the area ratio must be considered. When changing from a rectangle to this “Reverse U-Shape” more surface area is being added to the aperture walls. For example, a rectangular pad that is 13.8 mils square has an area ratio of 0.7 and the same aperture reduced by one mil per side with the “Reverse U-Shape” has an area ratio of 0.5.

If the area ratio limit (i.e., 0.63) is exceeded, a standard reduction should be made and a rounded square or rectangular aperture must be used.

Bridging at Print: Simple Guidelines to Eliminate Bridging

There is one thing certain, there are no guarantees for good board design. Many times contract manufacturers are expected to successfully assemble components onto boards where design is not optimized. This can be the case on pitch type components such as QFPs, BTCs, TSOPs and many others. Many times the width of the copper SMT pad is larger than it should be and if the stencil is not designed properly, bridging can occur. If bridging at print is occurring, the primary areas to address are aperture width and area ratio. The area ratio will determine what foil thickness should be used if that is in question. Again, through many years and thousands of stencil designs, it has been determined the best design for pitch components is to make the width of the aperture half of the pitch of the component leads. For instance, if the pitch is 15.7 (0.4 mm), the stencil aperture width should be 7.85 mils. Many stencil manufacturers will round up a 15.7 mil (0.4 mm) pitch component and call it 16 mil pitch when calculating the aperture width and will recommend or design the aperture to be 8 mils wide. The same for 19.6 or 19.7 mil pitch (0.5 mm) devices. Many stencil suppliers will make the aperture widths for these apertures 10 mils wide. Typically, the length of these types of components are always kept the same as the length of the copper pads. Very rarely have there been bridging issues at print when this “Half Pitch” rule is followed (Figure 16). The only caveat is if the copper pad is less than half of the pitch, then you would design the stencil aperture the same width as the copper pad.

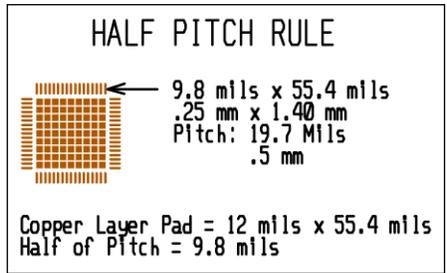


Figure 16 – Half Pitch Rule

After calculating half the pitch to determine the width of the aperture and designing it so that the length is the same as the copper pad, the area ratio can be determined. The stencil designer should then verify the area ratio is higher than the lowest allowable area ratio for the stencil.

Bridging at SMT Reflow: Causes for Bridging After Reflow When it is Not Present After Print

When bridging occurs after reflow but is not present after print, most often it is seen occurring on Gull wing, QFP type devices (Figure 17). Before beginning a root cause analysis process for this type of defect, it is necessary to have a Component Data Sheet (Figure 18) for the actual device being placed.



Figure 17 – Example of QFP Gull wing Lead

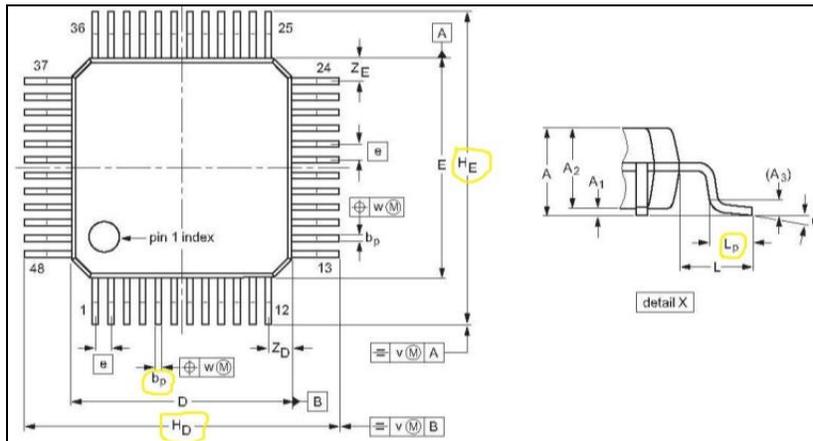


Figure 18 – QFP Data Sheet Example

To identify a solution for this defect, one has to look at the foot dimension, L_p on the component data sheet and compare it to the land pad on the copper layer of the PWB. In most cases when the foot is much shorter than the land pad, bridging can occur. An example of this is shown below (Figure 19).

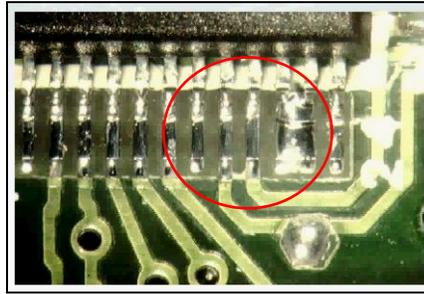


Figure 19 – Example of QFP Bridging

Due to the way the gull wing lead is exposed to the convective heat of the oven, these types of components heat up quickly in reflow. When the length of the Gull wing foot is 25% shorter or more than the length of the land pad of the board, thermal differences allow the foot of the lead to heat faster than the solder paste on the land pad of the board. As this occurs, the solder paste becomes liquidous at the foot first, and paste tends to wet up the lead typically stopping close to the shoulder. At this point, because no more solder can wet up the lead, the liquid solder starts pooling around the foot of the component until the rest of the land pad heats and paste wets to the entire pad. On fine pitch components, this pooling can spill out across the lead and bridge or short to the next lead. A common cause of this phenomenon is when the land pad is designed for a specific component and the component is replaced by another similar component where the foot is too short for the length of the land pad on the PWB.

Reducing the paste volume printed on the land pad is necessary to prevent paste from pooling during reflow and causing bridges or shorts. The process to identify and correct this defect includes determining the length of the foot and comparing it to the length of the copper SMT pad on the PWB. If the foot of the component lead is 25% shorter than the length of the pad, the volume of paste deposited should be reduced 10%. If the length of the lead is 50% shorter than the land pad a 25% volume reduction should be made and finally, if it is 70% shorter, then the volume should be reduced by 40%. In addition to reducing the volume of paste printed on the land pad, it is also necessary to center the new, modified stencil aperture on the component foot. This process involves looking at the component drawing (Figure 18) and identifying the dimension H_E and H_D for the component being analyzed to determine the outer extents of the component feet to create a Gerber layer of the component feet centered according to the drawing. The new stencil apertures created to reflect the reduction in volume should be centered on this pattern as shown below (Figure 20). When the new apertures are used, the reduced paste volume will flow up to the aperture shoulder as it wets to the land pad. The pooling will be eliminated and bridging prevented with this new aperture design.

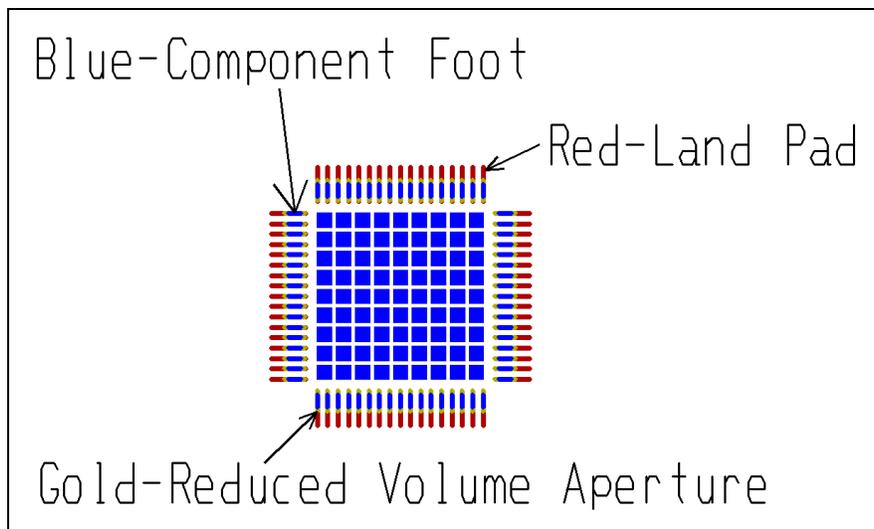


Figure 20 – Example of Reduced Volume Apertures Centered on Component Foot

Insufficient Solder Volume at SMT Reflow: Correlation of Stencil Design to Solder Volume After Reflow for Leadless Devices

In previous work R. Dervaes [4] outlined a method to overcome Lead-less component failures through stencil design that still apply today. With the widespread use of lead-less packages, insufficient solder volume is one SMT defect that is occurring more frequently. This SMT defect is costly, but can be repaired at rework. To prevent this defect, one must compare the leadless package termination size to the PCB land pad. The required ratio of the two is very consistent and adjustments to the solder paste stencil can prevent insufficient solder volume problems at reflow.

To obtain sufficient solder paste volume after reflow and produce acceptable solder joints, the PCB land pad length is ~110% of the leadless termination length (Figure 21). However, inspection and rework of leadless components is extremely difficult when almost 100% of the land pad is underneath the component. For this reason, the majority of leadless land pad designs will lengthen the PCB land pad.

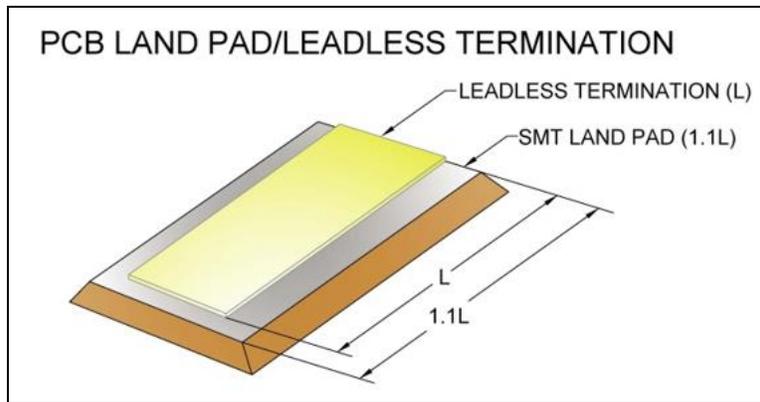
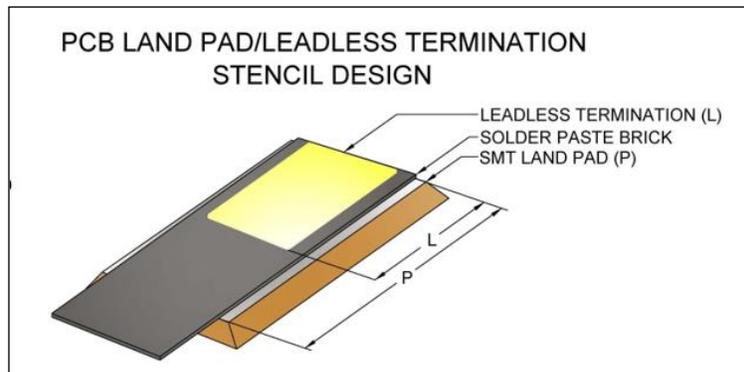


Figure 21 – Optimum Paste Volume for Leadless Termination

While in the reflow oven, the leadless package design tends to obstruct more of the convection air flow and IR, compared to a gull wing style component. Unless the PCB has extremely heavy copper weights, the leadless termination and PCB land pad temperatures will therefore increase fairly uniformly, and be close together at liquidous. This will produce a uniform wetting



of the solder across the surfaces. Increasing the land pad length beyond 110% of the termination length increases the surface area that the solder has to cover. This will limit the formation of acceptable solder fillets, if the solder paste volume is not increased at print.

Figure 22 – Volume Increase Diagram

The volume increase is based on the size difference of the leadless termination and PCB land pad and is applied to the stencil. Referring to Figure 22, the volume increase is calculated as follows:

$$\text{Volume increase (\%)} = 50 * \left(1 - \left(\frac{L}{P}\right)\right)$$

The new stencil apertures created to reflect the reduction in volume should be centered on this pattern as shown in Figure 22.

The additional solder paste volume should always be printed to the “toe” side for leadless components. Extending the solder paste brick further underneath the leadless package should be avoided, due to the bridging potential and increasing the stencil

aperture width should also be avoided. Extending solder paste beyond the SMT land pad, up to 0.040”, is not a problem with leaded or lead-free solders as both coalesce and pull back onto the SMT land pad extremely well.

However, it is extremely rare that an overprint gets even close to 0.040” with leadless components and an overprint to this extent is typically reserved for paste-in-hole applications. The majority of the time the extension is somewhere between 0.005” and 0.010”.

In addition to increasing the stencil aperture size, the stencil foil thickness is also very important. For the majority of leadless components, a 0.005” foil thickness is required. If the foil thickness has to be reduced to accommodate other SMT components, the stencil aperture volume for the leadless components should be increased accordingly. Solder volumes are critical and it does not take much of a volume reduction to start causing yield problems.

Voiding: Design Ideas to Reduce Voiding Through Stencil Design

There are many variables to address when attempting to reduce voids in SMT solder joints and stencil design is one. Ground pads on BTCs such as QFNs are an area of focus and the search to identify the best design to minimize voiding is ongoing. The IPC 7525(B) Stencil Design Guidelines [2] address ground pads for LCC/BTC device and suggests a 20% to 50% reduction in the area and the use of a window pane design. It also suggests not depositing paste directly onto any vias that are located in the ground pad with the idea that liquid solder would seep into the via during reflow causing less than 50% coverage.

Historically, the window pane design has been the most utilized design for ground pads in stencil production. Over the past several years, a five dot pattern has been used along with many other designs in the attempt to reduce solder voids. Lentz studied four different designs [5] to determine if voiding could be reduced based on the stencil design below (Figure 23).

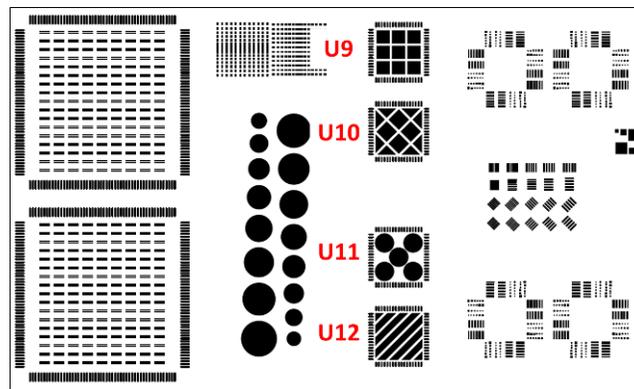


Figure 23 – Voiding Stencil Design

A standard window pane was used for U9, a diagonally rotated window pane was used for U10, five dot pattern used for U11 and a diagonal line design was used for U12. The specifics of the stencil design are listed below (Table 5). All designs targeted a 65% paste coverage or a 35% area reduction.

Table 5 – Stencil Design For Voiding

| Location | Aperture Shape | Aperture Size in mils (mm) | Spacing in mils (mm) | Paste Coverage Area (%) |
|----------|----------------|----------------------------|----------------------|-------------------------|
| U9 | Square | 88 (2.24) | 20 (0.51) | 65.3 |
| U10 | Diamond | 99 (2.51) | 20 (0.51) | 65.3 |
| U11 | Circle | 132 (3.35) | 8 (0.20) | 63.9 |
| U12 | Stripe | 40 (1.02) | 20 (0.51) | 65.0 |

Three different water soluble pastes and two different no clean pastes were printed, dummy parts were then placed and the boards reflowed. Each of the four locations were then placed in X-Ray, images taken (Figure 23) and void area percentages were measured. The results are shown in the graph below (Figure 25).

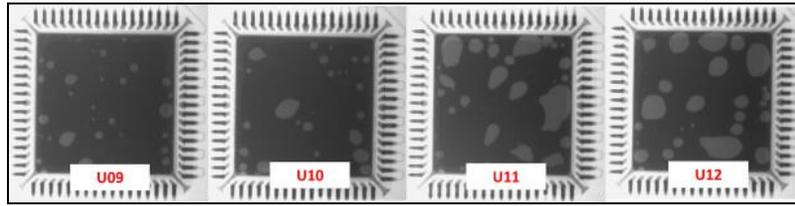


Figure 24- X-Ray Images of Voiding by Stencil Design

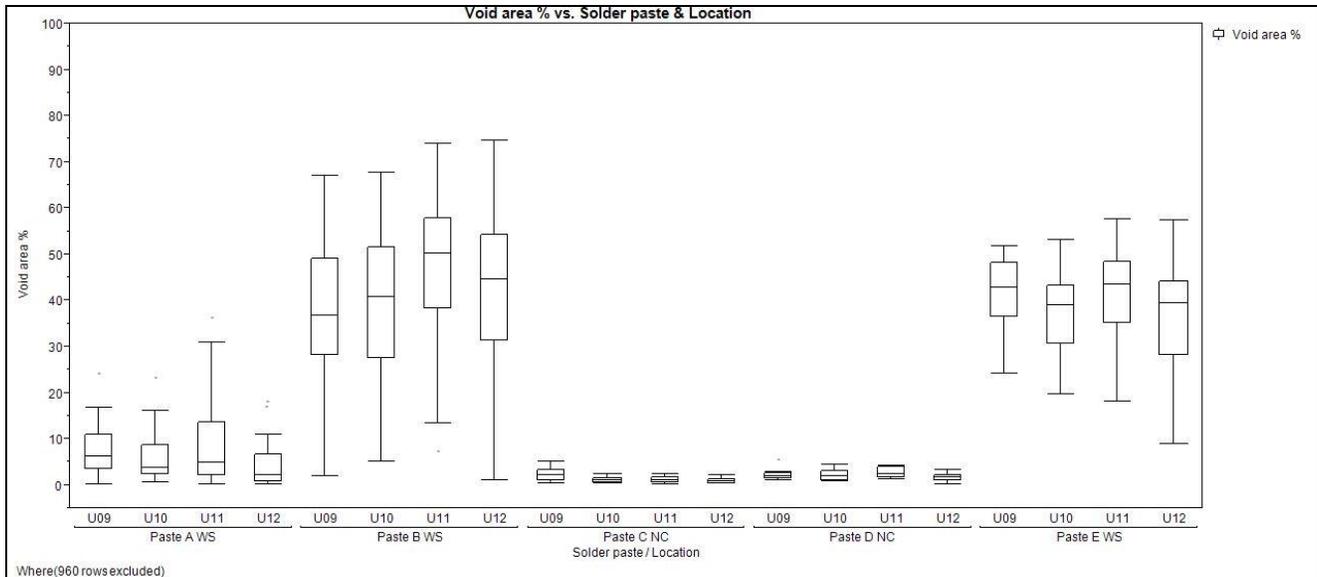


Figure 25 – Void Area Percent by Solder Paste Type and Location

Next, the data was compared to see if voiding percentage was significantly different using Tukey-Kramer HSD in the image below (Figure 26). When examining the Tukey-Kramer data, water soluble paste A, water soluble paste E and no clean paste D all showed no statistical difference in void percentage between different ground pad designs. However, water soluble paste B showed that the ground pad design for U11 had a statistically higher percentage of voiding than the other three designs. No clean paste C showed that U09 had a statistically higher percentage of voiding than the other three designs. One can see by the results of this testing these specific designs do not significantly reduce voiding. It also appears the specific paste can have an influence on voiding percentage for these specific designs.

There is much work still to do in identifying the best stencil design to minimize voiding on ground pads of these bottom terminated devices. Area coverage, pattern opening designs as well as the venting pattern in many shapes and combinations all need to be studied in order to determine the best pattern for void reduction. Until this work is done, a common design currently yielding good results for BTCs is a 5 dot pattern or window pane pattern with 50% volume coverage of the ground on the PWB.

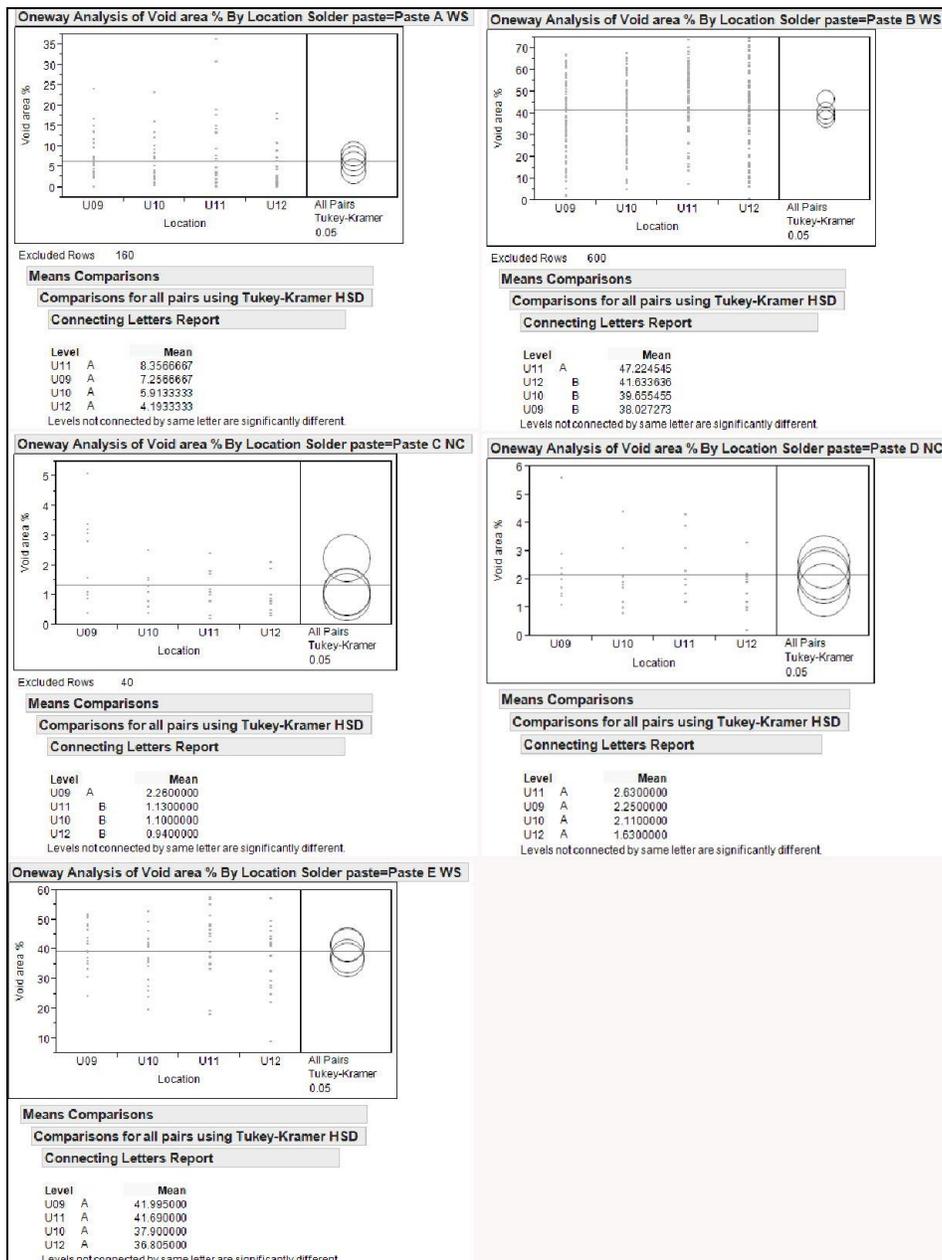


Figure 26 – Tukey-Kramer HSD Data on Paste Vs Void Percentage by Location

Conclusions

Identifying specific “universal” defects in the print process is critical in the effort to improve first pass yields, minimize cost, minimize assembly time and in turn to improve reliability. These “universal” defects including poor solder paste release, solder balls, tombstoning, bridging at print, bridging after reflow, insufficient solder after reflow and voiding on bottom terminated devices can all be addressed with stencil design. In many cases these defects can be greatly reduced by addressing the root cause of the specific issues.

When addressing insufficient paste at print, it has been determined it is critical to identify minimum transfer efficiencies required for acceptable solder joints and then determine minimum area ratios necessary on stencil apertures to achieve those transfer efficiencies. Solder ball issues can best be overcome using a “U-Shape” or “Inverted Homeplate” aperture and tombstoning can be improved using a “Reverse U-Shape” aperture. The “Half Pitch Rule” is a valid and widely accepted method for eliminating bridging at print and when bridging is occurring after reflow on gull wing devices such as QFPs, it is critical to compare the size of the PWB land pad to the size of the foot of the actual component lead. Finally, voiding on ground pads of BTCs are critical and there is much work left to do to identify the best stencil design to minimize voiding percentages on these types of devices. Currently, however, the standard window pane and five dot pattern remain accepted designs.

Future Work

Further investigation into ground pad designs for bottom terminated devices will be presented to identify patterns that can minimize void percentages.

References

- [1] R. Dervaes, “SMT Assembly Challenges and Proven Solutions for Improving Yields”, Proceedings of IPC Apex Expo, 2015.
- [2] IPC, “IPC-7525B 2011-October Stencil Design Guidelines”.
- [3] J. Bath, T. Lentz, G. Smith, “An Investigation into the Use of Nano-Coated Stencils to Improve Solder Paste Printing with Small Stencil Aperture Area Ratios”, Proceedings of IPC Apex Expo, 2016.
- [4] R. Dervaes, “Improving SMT Yields – Leadless Components”. Internal Company Report.
- [5] T. Lentz, “Fill the Void”, SMTA International 2016.