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Implementing Robust Bead Probe Test Processes into Standard Pb-Free Assembly

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Abstract
Increasing system integration and component densities continue to significantly reduce the opportunity to access nets using standard test points. Over time the size of test points has been drastically reduced (as small as 0.5 mm in diameter) but current product design parameters have created space and access limitations that remove even the option for these test points. Many high speed signal lines have now been restricted to inner layers only. Where surface traces are still available for access, bead probe technology is an option that reduces test point space requirements as well as their effects on high speed nets and distributes mechanical loading away from BGA footprints enabling test access and reducing the risk of mechanical defects associated with the concentration of ICT spring forces under BGA devices.

Building on Celestica's previous work characterizing contact resistance associated with Pr-free compatible surface finishes and process chemistry; this paper will describe experimentation to define a robust process window for the implementation of bead probe and similar bump technology that is compatible with standard Pb-free assembly processes. Test Vehicle assembly process, test methods and "Design of Experiments" will be described. Bead Probe formation and deformation under use will also be presented along with selected results.

Key words: Structural Test, In-Circuit Test, Bead Probe, Screen Printing

Introduction
Electronic circuit boards have traditionally needed to be tested during manufacturing to catch structural defects and to ensure the functionality. In-Circuit Test (ICT) has become an industry wide standard that generated its own technical community and industry standard equipment sets. These external probe based tests require a dispersed access to the electrical networks on the assembly. The most common way to provide access for this test is through test points but placing them on the board has always been a compromise to Designers and Layout staff who must sacrifice space and sometimes performance to provide this access. Fixture suppliers and other industry experts regularly publish optimization techniques for standard ICT probe technology. There are multiple conference sessions and workshops dedicated to this topic every year. Crisp et al [1] have recently published on a wide range of process and equipment factors that effect test yield.

As designs have become more complex, the impact of space and high speed circuits cause test points to be a larger compromise. The high speed networks are much more sensitive to trace impedance effects. Test points (TP) and VIAs (used as TP) not only take up valuable space on the board surface, but can cause impedance, and even electromagnetic interference (EMI) problems on high speed paths that degrades the overall system performance.
Component pad spacing has reduced below 4 mils and PCB trace widths are also of similar size. Adding a 30mil diameter test point - or even a 19mil test point becomes almost impossible.
Factors that have reduced the number of TPs include:

- Increased number of layers which may not touch or be near top/bottom of PCB
- Ground planes limiting top/bottom side access
- Blind VIAs - not touching top or bottom, but buried within layers
- Back Drilled VIAs - physically removing the metal VIA to reduce trace inductance of a full top/bottom VIA
- Circuit impedance sensitivity has increased reluctance to incorporate anything (like a TP) that may load down the trace

Test engineers and test product suppliers have responded with many technologies to provide virtual test points or access through internal networks - one example is Boundary Scan cells and advanced uses of BScan chains. However the need for some test points continues, even on high speed networks. Options for the layout team remain few and adding solder to surface traces has been explored by a number of companies and equipment makers. The Bead Probe technology (BPT) utilized in this work was developed by a major test platform supplier and is intended to address this industry problem and provide for easy integration into their widely adopted In-Circuit platforms. The technology uses the conventional In-Circuit

Test approach to probe exposed traces on the surface of printed circuit boards. The solder beads are screen printed directly onto the exposed traces and become viable probing surfaces after the printed circuit boards are reflowed.
The equipment supplier who developed Bead Probe technology (BPT) provides a handbook which is reasonably comprehensive on the test and layout aspects. This paper should add to this handbook by evaluating the process aspects of the technology in the context of standardized Pb-free assembly for medium and high thermal mass products that would normally be associated with the military, aerospace, industrial and medical sectors of the industry. The intent is to produce a standard methodology for implementing BPT into SMT assembly programs currently using screen printing stencils fabricated from 100 and 125 micron sheet stock. The results are applicable to other thicknesses where printing capability has been established for the individual solder paste volumes. The goal of the project is to define a set of parameters that when utilised to convert or implement the test technology will be universally implementable in assembly manufacturing or impose trivial impact on process flows or machinery installations.

Experimental Design
Evaluations of process materials to determine their interaction with ICT have been conducted in the past. McMahon et al. [2] have demonstrated a test vehicle & ICT fixture combination designed specifically for this purpose. In this current work those test vehicle and fixture designs have been updated and modified to provide equivalent contact resistance information for the bead probe approach to ICT access. This modified design is intended to provide data which will facilitate optimization of the bead probe process and provide relevant comparisons to standard ICT probe processes utilizing current Pb-free process materials. The experiment includes input variables related to product design, fixture design and process design. The single response variable is contact resistance; it is evaluated at a variety of intervals after assembly to evaluate the change in response after storage and under repetitive test. Resistance thresholds relevant to ICT test requirements for particular components have been identified in the previous work. Specifically, five (5), ten (10) and forty-two (42) ohms of resistance are the consensus for low value resistor measurement limit, contact default limit, digital test default limit [2]. However for the current experimental response and for comparisons to existing data where relatively few measurements exceed these levels, a 1 ohm limit is also used.

Table 1: : PWB and ICT Fixture Factor Levels.

Board Factors													
Solder mask defined ovals (SMD) All combinations	Width (mils)	13 mil				14 mil				15 mil			
	Length (mils)	15	20	25	30	15	20	25	30	15	20	25	30
Traces in Solder mask ovals (NSMD) All combinations	Trace width (mils)	6				7				8			
	Length (mils)	15	20	25	30	15	20	25	30	15	20	25	30
Test Fixture / Probe Factors													
Spring Force		High				Standard				Low			
Probe Series, (size)		100 series				75 series				50 series			
Probe Contact		Flat face								Waffle Face			

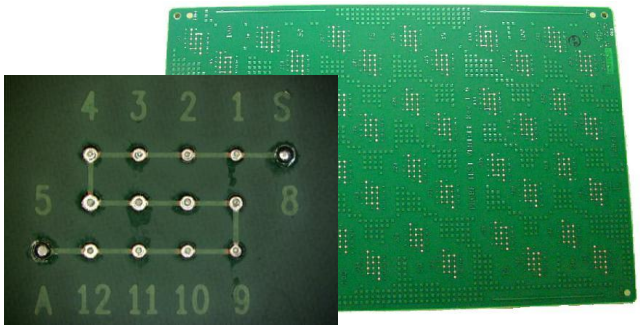

Figure 1: Test Vehicle Configuration. – Previous Version

Test Vehicle Design
The test vehicle for this experimentation is a modification of a previous assembly, exhibited in Figure 1. There are 48 replications of the etch pattern (Figure 2) arranged in 12 staggered rows. In this bead probe experiment the active patterns are reduced to 36 because bead probes were not available in Series 39 configuration at the time of the study. Traditional 0.030 inch diameter solder pads labeled “S” and “A” are included at each end of the individual etches to enable 4 wire measurement of the contact resistance. These pads displayed in Figure 2 are contacted by standard ICT probes after solder has been

reflowed to facilitate comparisons with previous experiments. Typical SMD and NSMD targets like those exhibited in Figure 3 are located in alternate columns of the etch design and probe series are distributed in multiple rows. The probe styles displayed in Figure 4 are also distributed over the surface of the board. This dispersion of factor levels is intended to reduce any location effect but as with many hardware factors included in experiment design, complete randomness is not achievable. In this case we must consider that the factors are distributed but not completely random. Each individual PWB yields 432 individual resistance measurements at every test.

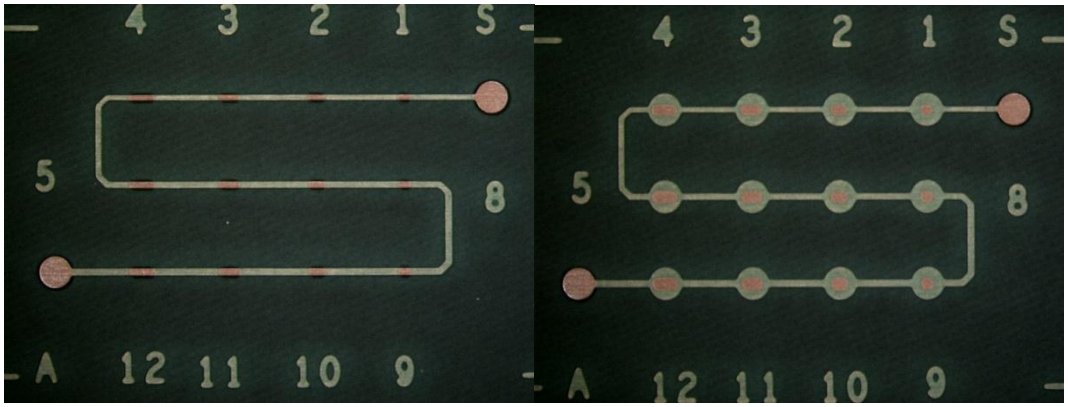

Figure 2: Surface Copper & SMO designs for NSMD and SMD Bead Probe Targets.

The original plan for the experiment was to evaluate nominal trace widths of 0.004, 0.005 and 0.006 inches. Upon receipt of the PWBs we measured surface copper and solder mask opening (SMO) dimensions and discovered that the as manufactured trace dimensions were much closer to 0.006, 0.007 and 0.008 inches. SMO width dimensions were originally intended to be copper width plus 0.006 but again the "as manufactured" was copper plus 0.007 inches. The as manufactured factor levels associated with the TV and fixture designs are displayed in Table 1. BPT is adaptable to either signal traces or expansive copper areas where either power or ground circuitry exists on the surface. For this reason both solder mask defined (SMD) and Non-solder mask defined (NSMD) targets have been included in the experiment. The size and configuration of the wettable copper area may have a significant effect on the solder volume requirements.

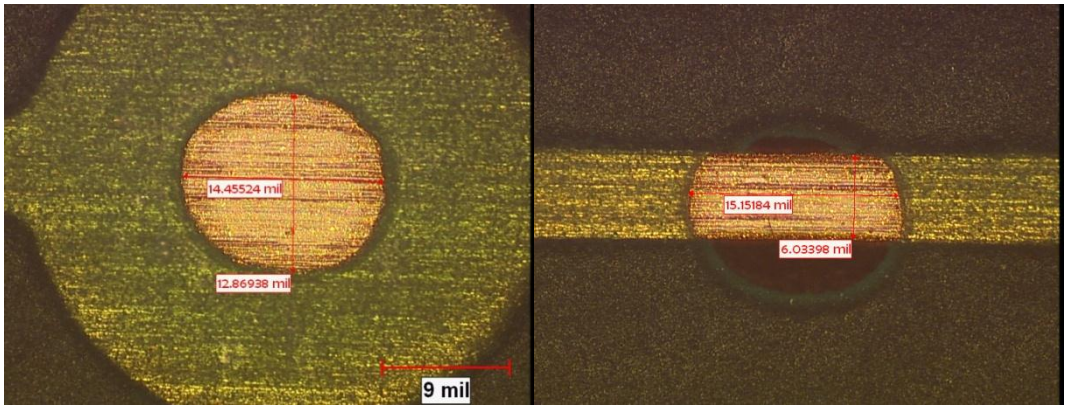

Figure 3: Individual examples of Copper & SMO configurations

Test Fixture Design

The ICT fixture is a standard vacuum operated single sided clam shell fixture. The probes series are arranged by in multiple repeating rows to distribute individual levels over the test vehicle area. Probe styles are distributed by individual etch patterns. Figure 5 displays the standard configuration, a single pattern of 12 measurement positions has only one series and style combined with standard probes for the reference positions. Finally the three levels of spring force are distributed over the fixture. The combined result is that each individual resistance measurement is assigned a combination of both target and fixture attributes and those combinations are distrusted as widely as possible over the available test positions.

Figure 4: Bead Probe Styles – Flat & Waffle

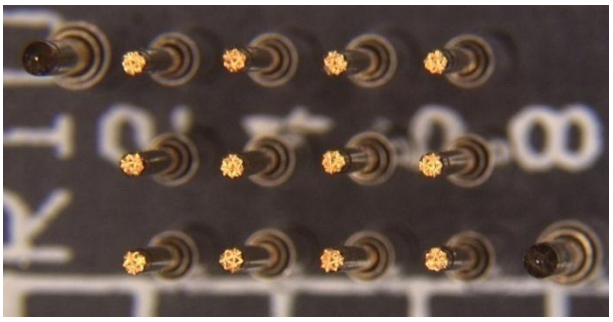

Figure 5: ICT fixture Probe Configuration

Resistance Measurement

Resistance distributions are highly skewed. Typically 95% or more of the measurements will be below 300 milliohms and the threshold of consequence for the experimental response will be 1 Ohm. Therefore the required resistance resolution is in the milliohm range necessitating 4-wire measurements of all probes in the experiment for greater accuracy and repeatability. The "S" and "A" bus wiring was assigned to separate probes while the "I" and "B" bus were wired to the same probe. The latter probe is the one where the resistance measurement will be made. The reason we use a separate "A" bus probe is to eliminate the probe and contact resistance of the source probe. This approach takes the source probe and any etch resistance completely out of the resulting measurement. The "S" and "A" pads are clearly identified in the surface copper at each end of the individual etch patterns in the test vehicle design as seen in Figure 2.

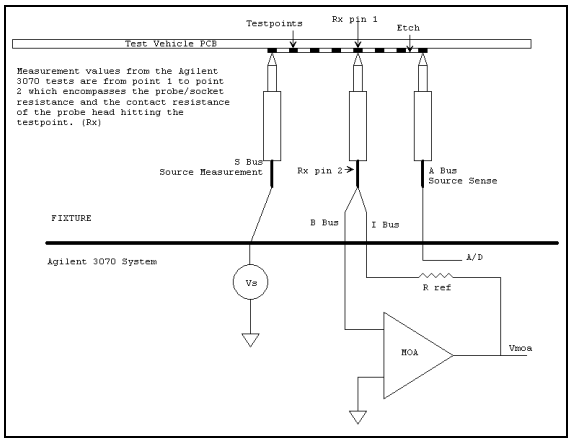

Figure 6: Four Wire Resistance Measurement

Stencil Design

Multiple stencil aperture sizes were calculated for both SMD and NSMD targets to create two levels of solder volume for each of SMD target sizes and two levels of solder volume for each of the NSMD target sizes within each stencil. There is some overlap in the dimensions resulting in 6 apertures labeled "L-A" through "L-F" for low volume and "H-A" though "H-F" for high volume. In both cases the progression is from smallest to largest aperture. The distribution of apertures in the stencil design for a single row of etch patterns is displayed in Figure 7. This pattern was repeated for every row of etch patterns in the test vehicle. When combined with the two different foil thicknesses of 0.004 and 0.005 inches there are 4 solder volumes for each of the target sizes.

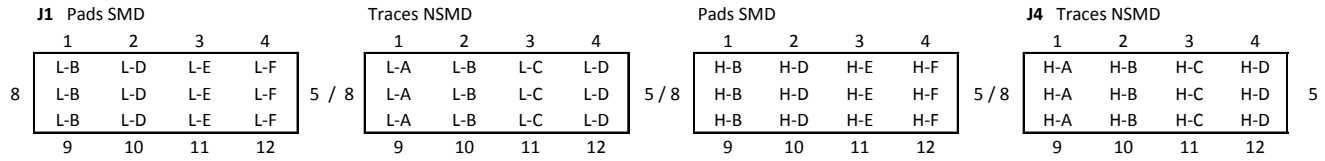

Figure 7: Stencil Aperture Mapping

Assembly Process

Test vehicles constructed using a standard high volume, phenolic cured filled epoxy FR4 resin system were processed in a production environment using standard Pb-free capable surface mount assembly (SMT) equipment at the Celestica Toronto facility. Solder Paste was printed onto each assembly using standard production parameters and equipment. The solder paste was a current generation, Type 3 powder, with 89 wt% metal load of SAC305 alloy, blended into Pb-Free capable flux vehicle. The laser cut stencil foils were either 0.004 or 0.005 inches thick. The assembly with paste deposits then reflow soldered in a 12 zone high thermal capacity reflow oven using a thermal profile suitable for medium thermal mass product typical for the military, aerospace, and industrial sectors of the industry. Each assembly was subsequently inverted and reflowed a second time to liquefy the flux residue surrounding each solder deposit and allow it to flow to the worst possible configuration for probe contact. This is an equivalent process to that experienced by bead probe contact targets located on the bottom side of a double sided SMT assembly. The SMT thermal excursion profile utilized for this project is approximately 175 seconds from ambient to reflow at 217℃ and is typical for medium complexity medium thermal mass products. The time versus temperature plot used to produce the solder targets is displayed in Figure 8.

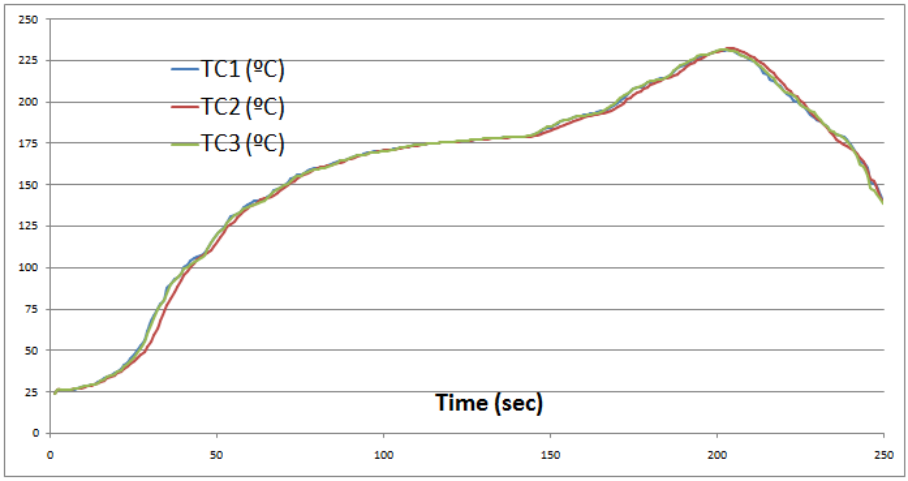

Figure 8: SMT Thermal Profile

Testing

The original intent was to measure ICT contact resistance at T_0 and at 120 day intervals until threshold values were exceeded in a significant portion of the sample size. This methodology was adapted during the experiment to include combinations of impact cycles using the ICT fixture and room temperature storage. The expectation prior to this initial test was that bead probe targets would produce resistance values similar to standard probe types at initial test but might suffer from degradation from two sources. First, that oxidation after initial test would produce a non-conductive surface layer that would increase resistance. Second, that successive strikes from the probes would produce decreasing amounts of deformation in the solder and therefore have lower opportunity to break up the oxide layer. The following methodology was established to enable comparisons based on storage and solder deformation.

All boards were tested within 24 hours of SMT assembly using an ICT program with a single vacuum cycle (TEST1) before resistance measurement. At either 129 or 130 days after SMT assembly all boards were tested using an ICT program with 5 vacuum cycles (TEST5) before resistance measurement. In the following 22 days TEST5 was repeated on decreasing subsets of boards created by removing 4 boards, two from each stencil lot until the last group had experienced a total of 41 vacuum cycles. All boards were returned to room temperature storage after this testing was complete. At 247 days after SMT assembly all boards were measured using the TEST1 method.

Results: Initial Test - Day 1

There were no events recorded at any of the threshold levels during the resistance measurement data from the initial TEST1 which was performed within 24 hours of SMT reflow. All of the data (100%) was below 1 ohm. The mean value was 26.9

milliohms, the median value was 17.6 milliohms, and the highest recorded contact resistance was 581 milliohms. As expected the significant difference between median and mean value speaks to the highly skewed nature of the distribution.

Results: Days 129 to 152

There are no single cycle results available at 129 days after reflow. However we can make some observations from the first 5 vacuum cycle tests which were conducted on the 129th and 130th day. This resistance measurement of all 30 boards which includes all levels of all factors recorded 3200 PPM above 1 ohm and 700 PPM above 5 ohm. These results are displayed in Table 2 as 6 cycle results. Over the next 22 days decreasing sample sizes were subjected to repeated test resulting in lots that had accumulated up to 41 vacuum cycles. Table 2 documents the variation in results as the number of boards is reduced and the number of contact strikes increases. The clear trend is an increase in both 5 ohm and 1 ohm yield with cycle count. Note that the number of test cycles includes the T_0 test.

Table 2: 5 Ohm & 1 Ohm - Day 129 to 152

Multi Vacuum Cycle -TEST5 contact - 5 Ohm Capability									
Test Cycles	6	11	16	21	26	31	36	41	All
< 5 Ohm	0.999300	0.999300	0.999100	0.998800	0.998700	0.998400	1.000000	1.000000	0.999100
Total Test (N)	12960	11232	9504	7776	6912	4320	1728	864	55296

Multi Vacuum Cycle TEST5 contact - 1 Ohm Capability									
Test Cycles	6	11	16	21	26	31	36	41	All
< 1 Ohm	0.996800	0.997000	0.996500	0.997200	0.995700	0.995600	0.996500	0.998800	0.996600
Total Test (N)	12960	11232	9504	7776	6912	4320	1728	864	55296

Results: Final Test - Day 247

The T1, single vacuum cycle results at 247 days represent a variety of conditions. Every assembly was T_0 tested and T_{247} tested using the TEST1 method but in the period between 129 and 152 days they received between 5 and 40 additional cycles. The 5 ohm yield from this test was 0.996065 or 3935 PPM greater than 5 ohm. The contact resistance 1 ohm yield data for all levels of all factors at T_{247} displayed in Table 3 exhibits significantly higher portions that exceed the 1 Ohm threshold. The maximum is 24900 PPM the minimum is 6900 PPM and the grand average across all lots is 17000 PPM. These results highlight the expected degradation due to oxidation and repeated compression of the solder if there is no optimization of the process.

Table 3: 1 Ohm – Day 247

Final day 247 TEST1 contact - 1 Ohm Capability									
Test Cycles	7	12	17	22	27	32	37	42	All
< 1 Ohm	0.978600	0.975100	0.984400	0.982600	0.978600	0.989000	0.987300	0.993100	0.982900
Total Test (N)	1728	1728	1728	1728	1728	1728	1728	864	12960

Analysis & Optimization

Clearly not all of the factor levels operate well over the storage and service conditions imposed by this experiment. Our initial approach to optimization was to generate models using the logistic regression techniques [1] employed during our previous work on standard probes. These techniques fail to converge to a numerical solution primarily because there are multiple factors that are not discretely defined in the data. Because there are multiple sizes of targets and multiple apertures for each target and multiple stencil thicknesses there is considerable overlap in some portions of the data

Figure 9: Flat and Waffle Compression 42 Vacuum Cycles - Oblique Views

Additionally, the two probe styles interact very differently with the solder Figure 9 and may produce very different capability windows in other factors. The logistic regression approach does not accommodate these types of issues. Our solution was to

use factor mapping techniques to find all of the combinations of factors that are not capable and define a process window that is easily implementable and provides a robust solution.
The initial factor maps were prepared using data from the final TEST1 conducted on day 247. However, these maps were then duplicated against all data collected on days 129 through 247. The total experimental data space is 68256 measurements, of which 23700 data points below 1 ohm were discovered to be easily separable by factor and level. Put in more basic terms there were 864 board / fixture / stencil combinations under test. Over 247 days of room temperature storage and multiple levels of probe impact, 150 of these combinations had never produced a resistance measurement greater than 1 ohm. While it is not possible to generate relative factor strengths using this technique, two categories of factors are evident.

1. Factors which have little impact
   Ex: Probe size, Target size, Target Type
2. Factors which are impactful when interacting with other significant factors.
   Ex: Probe Spring Force, Probe Type, Solder volume,

Solder volume was not in the list of factors predetermined for this DOE but exists as a calculated surrogate for the various combinations of stencil foil thickness and aperture size.
Several different factor maps provided consistent 1 ohm contact resistance capability. The simplest combination only required control of two primary factors.

Observations:

- There are several data and design issues that must be resolved before BPT can be implemented into functional product. Test point locations must be identified in the CAD files to allow for transposition to the data files for fixture construction, stencil fabrication, etc. BP locations must account for the probe keep out which will now be larger than the target. This is the opposite case to standard probes.
- Probe targets for signal traces must be located where line spacing and solder mask registration will not interact to expose more than one signal. Solder mask registration capability varies with PWB supplier and product configuration.
- Flat and Waffle probe faces act very differently with solder beads. This difference produces very different capability factor maps.
- Not all solder volume / probe target combinations are viable after room temperature storage.
- Not all solder volume / probe target combinations are viable after repeated fixture cycling.
- When comparing all data contact yield increases with increasing vacuum cycles
- When comparing all data contact yield deceases with increasing storage time.
- Increasing Probe Spring Force is usually the first action taken when probe contact becomes an issue. These experimental results did identify capable factor maps that included only standard and high spring forces but other combinations were which included all three spring forces were equally capable of achieving 1 ohm performance.

Conclusions

The experimental results demonstrate that Bead Probe technology when combined with the process and implementation approach developed here provides a viable option to removing traditional test points while still providing access. Furthermore, this implementation of BPT does not necessitate increased probe spring forces to match standard probe contact resistance performance.

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