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GENERALIZATIONS ABOUT COMPONENT FLATNESS AT ELEVATED TEMPERATURE

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ABSTRACT:
An examination was made of a database of collected component warpage information in the hopes of finding a simple correlation between a physical attribute of the components and the warpage measured at reflow temperatures. This would allow companies to by-pass actual experimentation, at least for a first pass approximation of the expected warpage. The measured flatness information was compared to various component outer and inner dimensions. In specific instances some correlations have been discerned, but no over-arching generalization can be made.

INTRODUCTION:
The flatness of boards and components is an important topic. This study deals only with components. This is not to imply that the study of the flatness of boards is not important, especially for thinner boards and boards of newer, "greener" materials where not as much data has been amassed. Failure to have completely flat components and circuit boards can lead to opens, shorts, head on pillow[1], weakened solder joints and stressed solder joints[2].

Component manufacturers have complete access to all the physical parameters and chemical information of the materials that go into their components. This allows them to carry out detailed parametric calculations[3] and even construct full-fledged FEA models which can be compared against experimental data[4-6].

The list of things that can affect component warpage is quite extensive. One study[3] mentioned: time dependent viscoelastic properties, curing profile, cooling rate, CTE mismatch between mold compound and substrate, chemical shrinkage, substrate thickness, Tg and Young's Modulus. In their particular case they found that a 20% higher CTE resulted in an additional 260 micron deviation from flatness. Another pair of studies[4,5] mentioned die size, die thickness, mold cap thickness, substrate thickness, substrate copper ratio, green vs. non-green substrates, mold compound (shrinkage), die attach material and stress relaxation. They found die size to be very significant but a change in die thickness from 0.1 to 0.075 mm had little effect. They also found that the mold compound had less effect once the temperature rose above the Tg of the material but then the copper ratio was more significant. A fourth study examined flip chip BGAs[6]. They concentrated on the physical makeup of the component and examined: substrate, underfill, die, thermal interface material (TIM) and the heat spreader. Smaller, thicker die were better, heat spreaders with high Young's Modulus and high CTE were better. Smaller package size was better. Heat spreaders that made contact along all four sides were better than those that only made contact on the four corners.

OEMs have examined boards, components and the manufacturing process[1,7] to see how one can alleviate, if not eliminate, the issues that arise from a lack of flatness throughout and after the manufacturing process. Without going into great detail, solder paste printing (amount and alignment), placement (alignment and pressure) and the reflow process have all been found to affect flatness of the final assembly.

As mentioned in the first paragraph, the problems do not stop at the end of the manufacturing line. Zhou and Lu have shown that "the net warpage change from the solder solidification temperature extremes of an accelerated thermal cycling test is related to the solder joint crack length."[2] This is a very significant finding.

And finally, NEC was just granted a US patent on a method to predict warp in electronic components and PCBs. They are using an "extension" of Timoshenko plate theory to develop an algorithm to predict wrap in multilayer structures. Inputs include: Young's Modulus, coefficient of thermal expansion (CTE), Poisson's ratio and layer dimensions. They claim it can even calculate warpage for printed circuit packs. Their Japanese patent was issued in 2007 and their US patent in 2013.[8]

All actual measurements were made by the second and fourth authors of this paper.

METHOD:
All measurements were collected with an Akrometrix PS400 system outfitted with a bottom infrared heating system. A 100 line per inch diffraction grating was used. Components were either LGAs, QFNs, CSPs or BGAs, the former two types without solder balls. Samples are usually delivered to the lab in sealed moisture barrier bags, but not always. The solder ball components were either received from the manufacturer without any solder balls applied or they were removed in the lab by carefully using a # 4 wood chisel. The components were then spray painted with a very thin layer of a high temperature white paint in an exhausted enclosure for safety

purposes. The painted surfaces were allowed to dry at room temperature for about ten minutes and then the parts were baked at 125°C for 4 hours. The JEDEC specification JESD22B112, "High Temperature Package Warpage Measurement Methodology"[9], requires a minimum of 3 samples. However, for the collected data in this paper, generally a set of ten components were heated at one time and then this was repeated with a second set of ten more components. The components were placed bottom side up (the surface that would normally be attached to the circuit board facing up) on a 11 cm x 11 cm piece of glass supported in the shadow moiré equipment by two thin metal rails.

Since all components are destined for lead free soldering processes, a reflow profile with a maximum temperature of 260°C was always used. The profile was a straight heating ramp profile with a gradient of 1C°/sec. This results in a longer profile than would be used in manufacturing, but to obtain a faster profile would have required retrofitting the equipment with convection heaters. Pictures of the Moiré pattern were captured at multiple temperature s during each run for every set of components.

RESULTS:

Over the course of the last few years more than 200 sets of components have been examined using the shadow moiré technique. **Figure 1** shows the histogram of the distribution of all the maximum deviations from flatness observed. All but two values of maximum deviation are below 100 microns and 74% are below 50 microns. In almost every case the maximum value was found at the maximum temperature of the reflow profile. **Figure 2** is a plot of the distribution of standard deviations for the maximum deviations from flatness at the highest temperatures used for the reflow profiles. All but four sets of measurements had standard deviations of less than 15 microns. This is very similar to the observation of Zhou and Lu who found their standard deviations to be less than 20 microns.

Of the two hundred and fifty-six different sets of components examined, 156 exhibited convex behaviour, 98 concave deformation, 5 complex (neither concave or convex) and two where this information was not recorded.

Figure 3 shows the warpage per millimeter of the diagonal length of the part plotted as function of the component thickness. All parts were between 0.4 and 1.3 mm in thickness with the greatest number being between 0.6 and 0.9 mm. There may be a slight trend toward larger deviations from flatness for thinner components, however, this perception may just be colored by the smaller number of thicker components. Component types include single dies, multiple dies, stacked dies and daisy chain components.

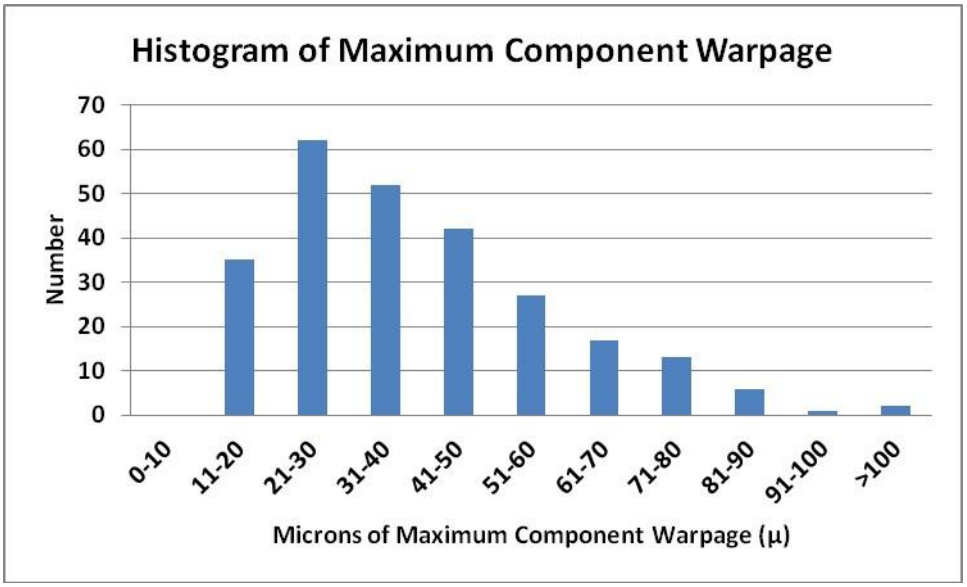

Figure 1. Histrogram of Maximum Deviation from Flatness

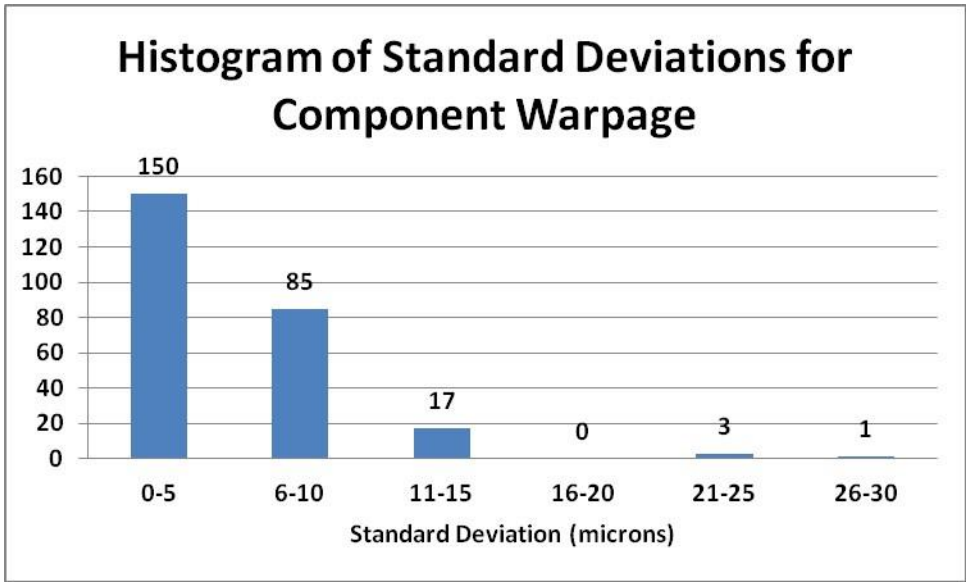

Figure 2. Standard Deviations of all the Maximum Deviations from Flatness Recorded

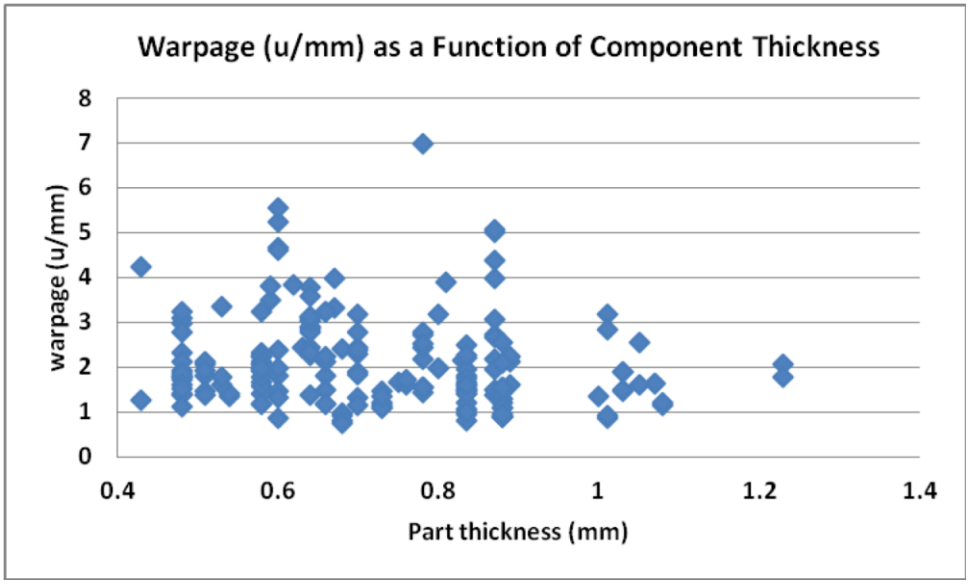

Figure 3. Warpage as Function of Component Thickness

However, for a subset of the most recent components (digital only), where there is only one die present, a clearer trend can be observed. See **Figure 4.** As one might expect, there is a correlation between package thickness and the amount of deviation from flatness.

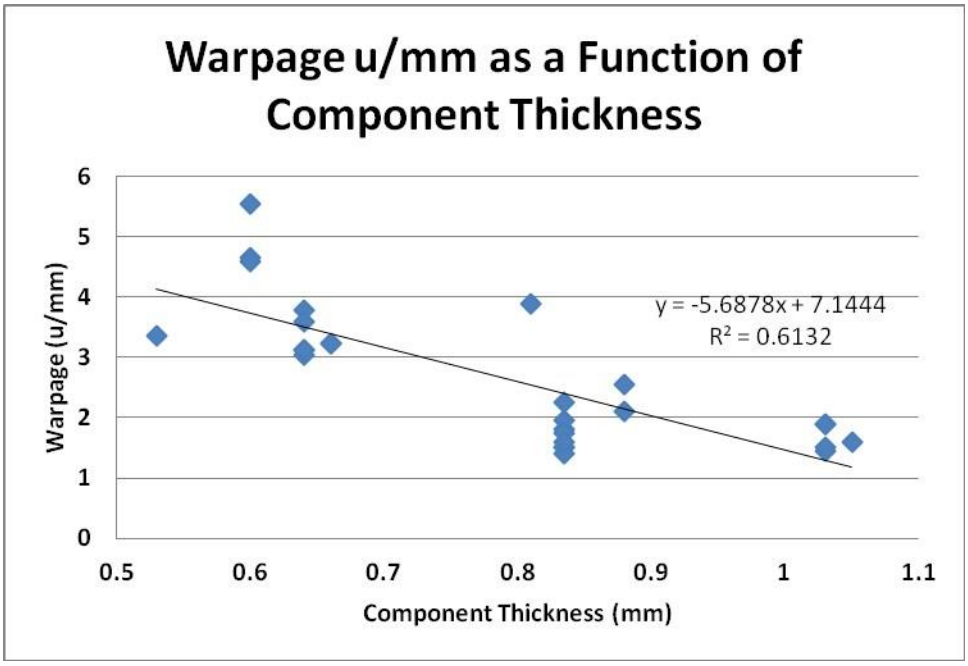

Figure 4. Warpage of Digital Components only as a Function of Component Thickness

Another way of looking at the flatness data is in terms of the volume of the ICs inside the components. The stiffness of the silicon will most certainly have an effect on the component behavior. **Figure 5** holds 74 data points where data is available about the ICs. There does seem to be an increase in possible change in flatness once the IC volume drops below about 15 cubic millimeters.

Another way of parsing the data is by company. However, only in two cases was there enough data points to look for trends.

Company A – 31 data points, 13 different components, information on 4 IC dimensions. **Figure 6** shows a weak trend for IC volume. **Figure 7** shows that there is the hint of increased warpage with thinner components. If one then looks at substrate thickness, all the components with almost double substrate thickness have higher warpage and it is close to showing a linear increase with component thickness. See **Figure 8**.

Company B – 123 data points, **Figure 9** shows no apparent correlation between component thickness and warpage. **Figure 10** does show some correlation between total IC volume and warpage. And this is certainly more evident when only those components with a single stack of three die are considered, as shown in **Figure 11**

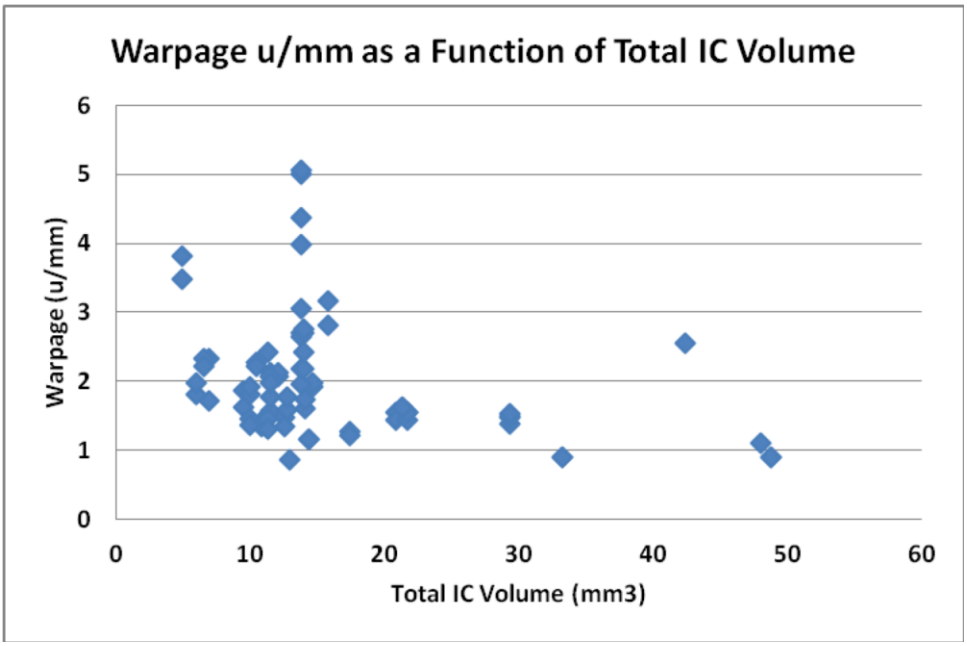

Figure 5 Flatness Deviation as a Function of Total IC Volume

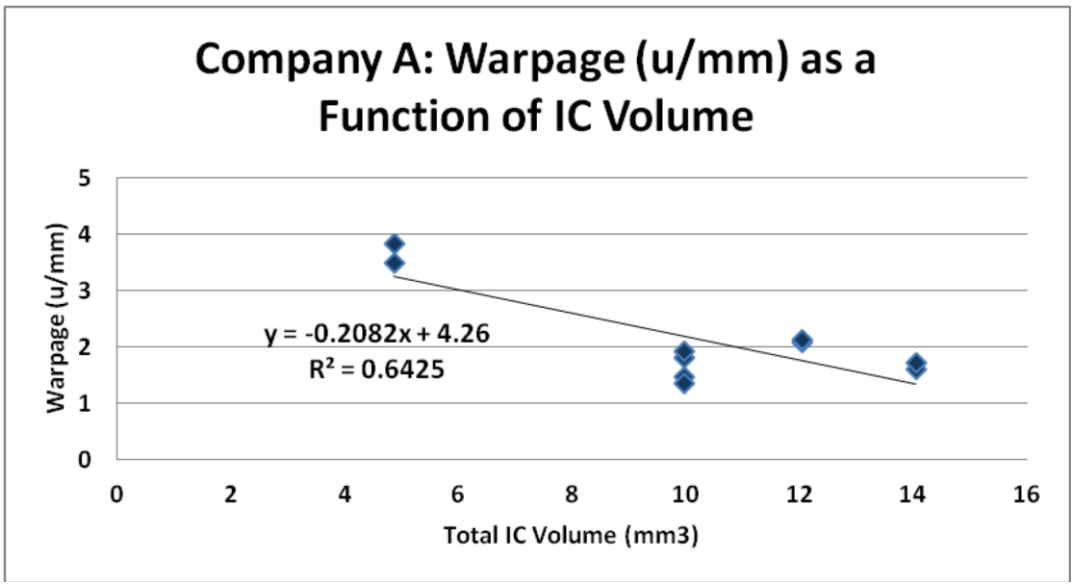

Figure 6 Company A: Warpage as a Function of Total IC Volume

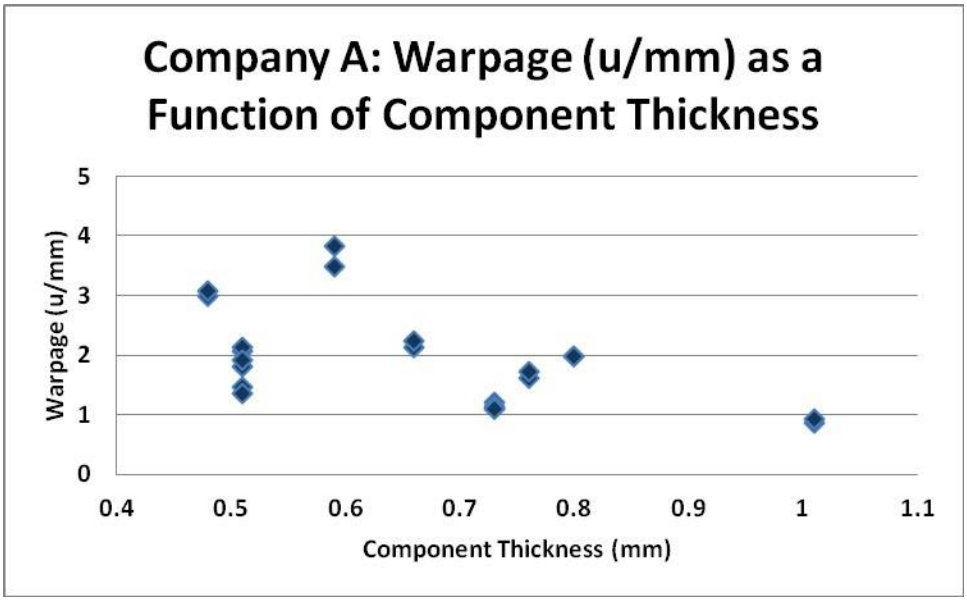

Figure 7 Company A: Warpage as a Function of Component Thickness

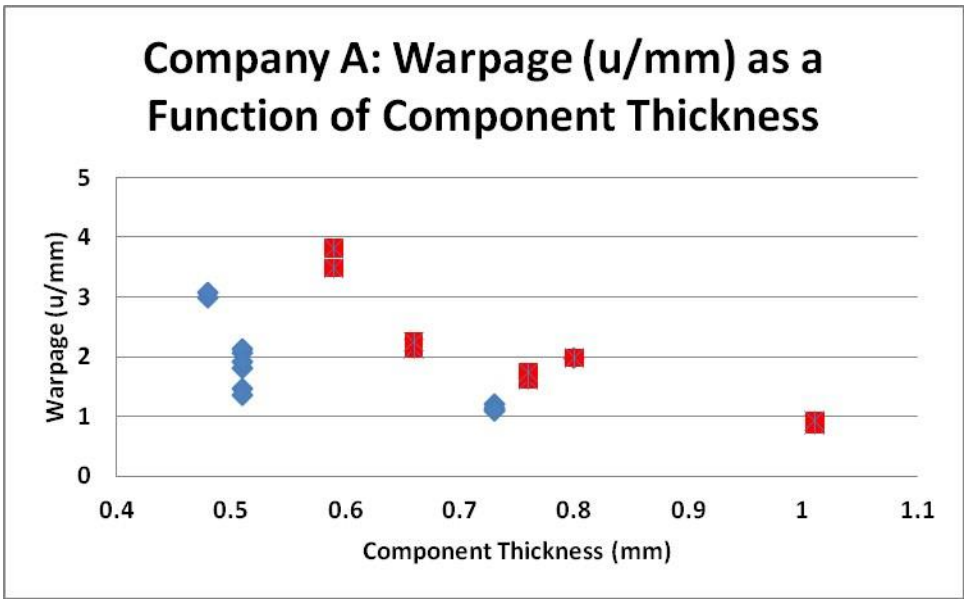

Figure 8 Company A: Warpage as a Function of Component Thickness, Highlighting Data Points of Components with Thicker Substrates

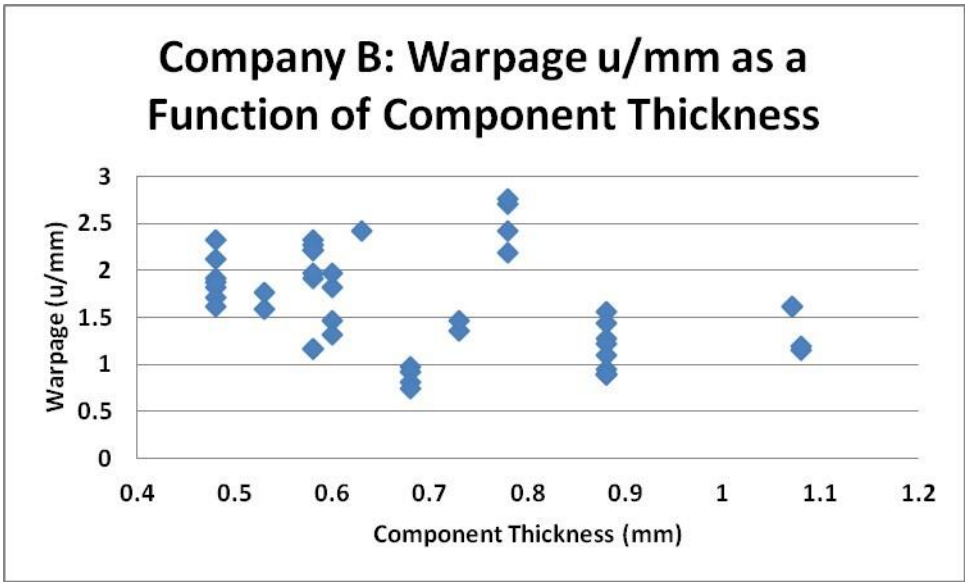

Figure 9 Company B: Warpage as a Function of Component Thickness

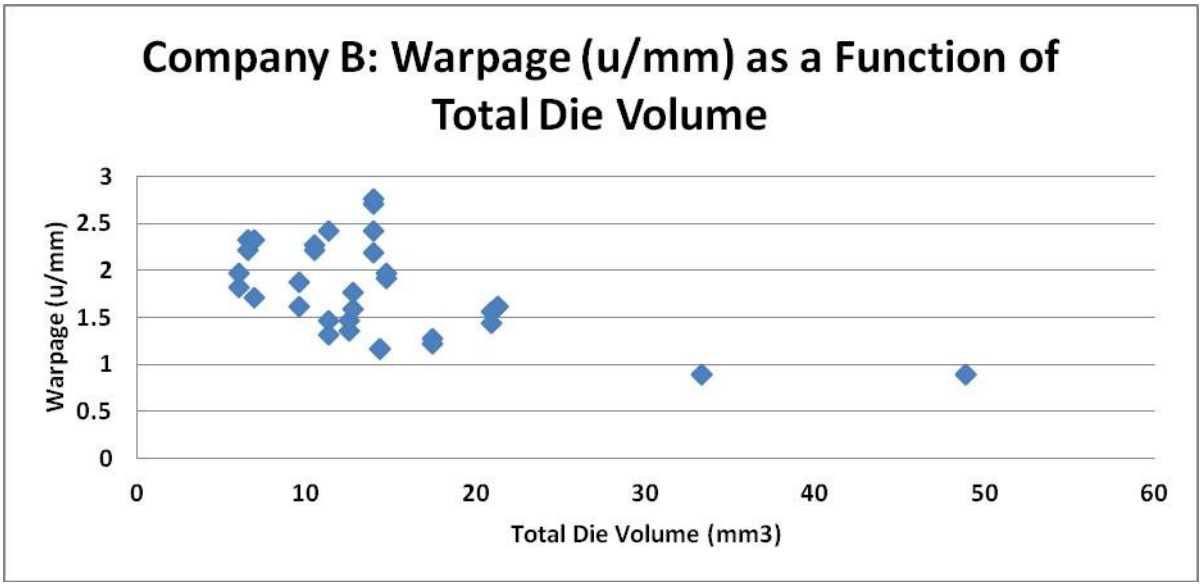

Figure 10 Company B: Component Warpage as a Function of Total Die Volume

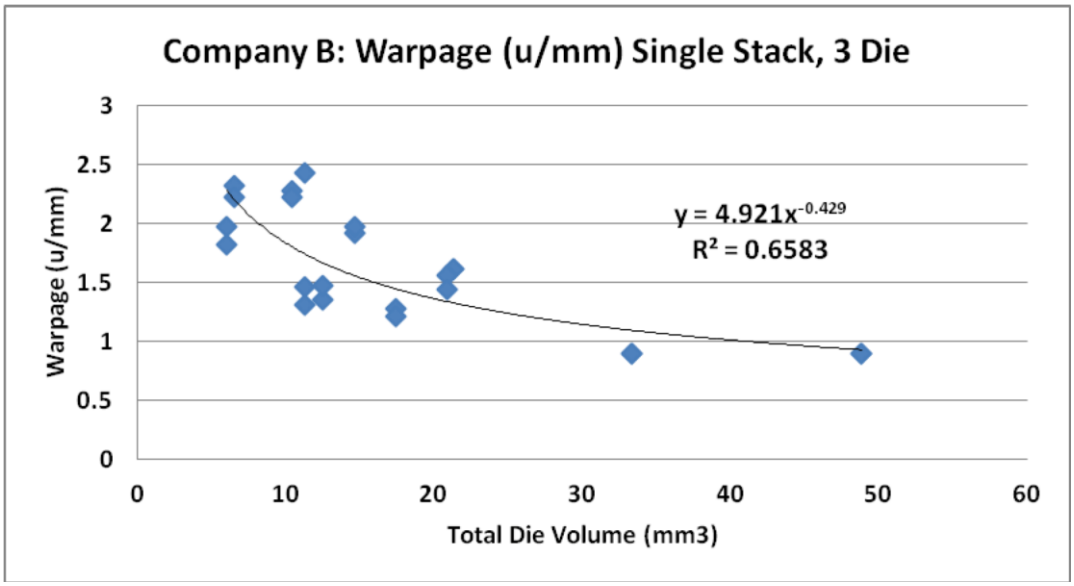

Figure 11 Company B :Warpage Components with only One Stack of 3 Die

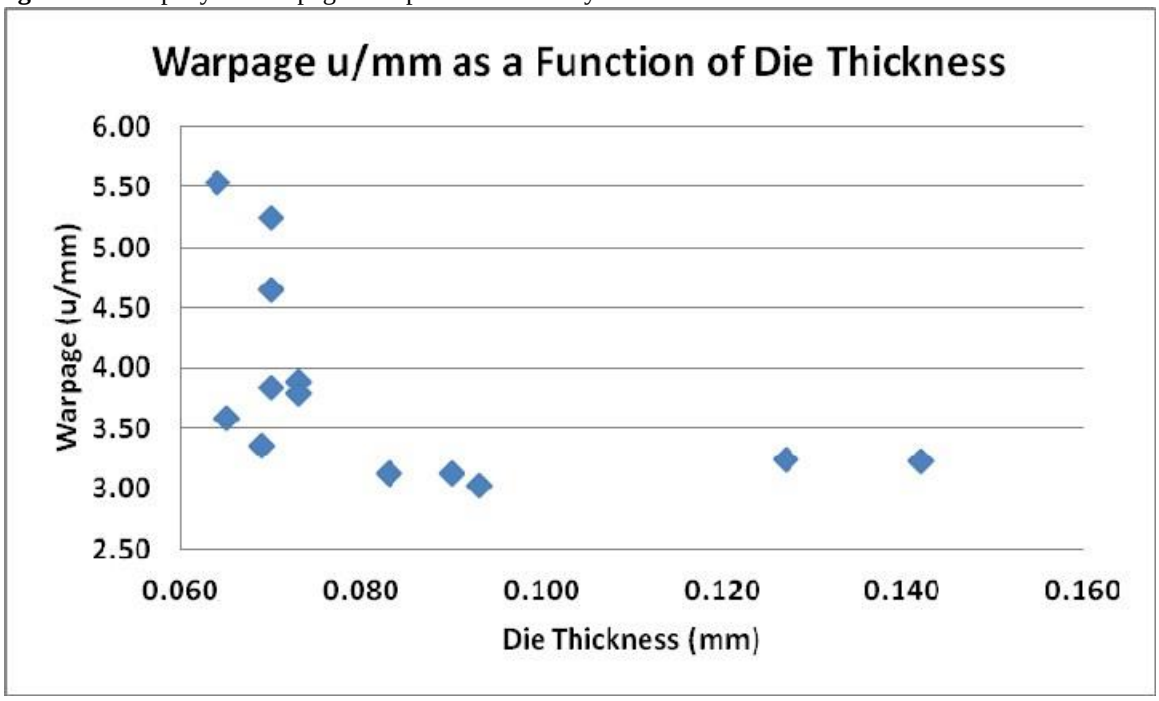

Figure12.

Unrelated to the present work, a series of components from various suppliers were cross-sectioned to determine the size of the ICs inside the components. This information was subsequently cross-referenced with the Thermoiré database and it was found that several had been measured for warpage. **Figure 12** shows the results of this cross- referencing. Here the points are for the warpage of recent components with only one die. The plot clearly shows that significant warpage occurs once the silicon reaches a thickness of 0.7 mm or thinner.

CONCLUSIONS:

In this paper an examination has been made of over 250 different components that have been examined using shadow moiré. There is no one attribute that provides a perfectly linear, exponential or polynomial correlation with the warpage observed for all plastic encapsulated components examined. For various subsets of the components tested, correlations have been possible with respect to component thickness, substrate thickness, total volume of the ICs in the component or IC die thickness when there was only one die. There were factors that could not be taken into consideration because of lack of data. Some of these were: packaging house or houses used by each component manufacturer, particular epoxy used for each component and curing conditions for each epoxy. It is expected that the type of epoxy would be the most important of these three mentioned.

Certainly component thickness and even more so IC volume are important considerations when examining for component flatness. But, as the scrutiny given to the data presented here shows, neither dimension tells the whole story regarding the warpage of components.

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